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DC-Link Capacitor Voltage Imbalance Compensation Method Based Injecting Harmonic Voltage for Cascaded Multi-Module Neutral Point Clamped Inverter

Kyoung-Pil Kang [1], Younghoon Cho [1,*], Ho-Sung Kim [2] and Ju-won Baek [2]

[1] Department of Electrical Engineering, Konkuk University, Seoul 05029, Korea; kkpsp@konkuk.ac.kr
[2] Industry Application Research Laboratory, KERI, Changwon 123456, Korea; khsgt@keri.re.kr (H.-S.K.); juwonbeak@keri.re.kr (J.-w.B.)
* Correspondence: yhcho98@konkuk.ac.kr; Tel.: +82-10-6207-0431

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Abstract: In a three-level (NPC) converter, the voltage imbalance problem in the DC-link capacitors is major issue. This paper proposes the DC-link capacitor voltage imbalance compensation method, where a common offset voltage is injected for a multi-module NPC inverter. The offset voltage consists of a harmonic voltage and a voltage difference between the upper and lower capacitors. The proposed method does not require any hardware modification, so that it is easily implemented. In order to show the effectiveness of the proposed balancing method, theoretical analysis is provided to balance the voltages, and both the simulations and the experiments were carried out to show that the voltage difference of the DC-link was decreased by the proposed method.

Keywords: multi-module NPC inverter; DC-link capacitor voltage balance; offset voltage injection

1. Introduction

In DC distribution systems, multi-level topologies have been considered because of the electrical characteristics of high voltage (HV) or medium voltage (MV) applications [1–9]. Three-level neutral-point-clamped (NPC) inverters have been widely used in MV and HV applications. Compared with two-level inverter systems, three-level NPC inverters have some advantages. NPC inverters have less harmonic component on output current. In addition, NPC inverters can use low level switches because of the dv/dt value on switching devices during switching operation, which is half of the two-level inverter. Therefore, NPC inverters have lower voltage stress than two-level inverters. However, NPC inverters have a major drawback associated with the neutral-point voltage. This problem is the voltage imbalance between the upper and lower capacitor voltage of the DC-link. This voltage imbalance is considered a system imperfection, which is caused by the difference in hardware components or switching operations of the NPC inverter [10,11]. Many strategies have been proposed to solve the capacitor voltage imbalance problem, and these strategies have achieved successful results [12–25].

In References [12,13], the hardware approach with an additional balancing circuit is proposed. This method can achieve voltage balance between the upper and lower capacitor but there is a problem with an increase in cost and system loss caused by the additional circuit. Several modulation techniques for single-phase three-level NPC inverters have been presented in References [14–21]. Among these modulation techniques, the carrier-based pulse width modulation (CB-PWM) method has been widely used due to its simplicity of appliance. In Reference [14], synthesizing the offset voltage method with zero-sequence component into a reference voltage was presented. The zero-sequence component

was calculated at every switching period based on the DC-link capacitor voltage and grid current. Another offset voltage injection method is presented in Reference [15]; in this method, the offset voltage with a distribution factor was injected into a modulation signal. However, these balancing controls are difficult to adapt because these controls require hard calculations for predicting line current and avoiding nonlinearity of the injection signal.

A method for injecting the offset voltage signal, which is composed of the second harmonic signal and capacitor voltage error, into the reference signal of the single-phase three-level NPC inverter for balancing the DC-link capacitor voltage has been studied in Reference [25]. To summarize [25], it is a method to increase or decrease the switching state by synthesizing the ON/OFF signal of the switching leg of the single-phase NPC inverter, operating according to the reference signal with the second harmonic signal. In addition, the limit value of the offset voltage by DC-link voltage error was analyzed. Although a previous study has the merit of its method being simple to implement because it does not require complicated calculations and additional hardware configuration, it can only compensate the DC-link capacitor voltage error in a narrow region due to a limitation of the injecting signal [25].

In this paper, the method proposed in [25] was further extended and detailed to adapt to cascaded multi-level inverters. The main concept of this paper is adding the DC-link capacitor voltage error signals of each NPC module into one phase reference signal for balancing each DC-link capacitor voltage error. This paper is organized as follows: In Section 2, an analysis of the offset voltage injection method for the NPC inverter with second harmonic signal injection is provided. In Section 3, a DC-link capacitor voltage balancing method is provided for a multi-module NPC inverter. In Sections 4 and 5, a 3-kW prototype model is fabricated to verify the effectiveness of the proposed method. Simulations and experiments were carried out under forced DC-link capacitor voltage imbalance conditions. Then, the results of simulations and experiments are discussed. Finally, Section 6 concludes this paper.

2. DC-Link Capacitor Voltage Balancing Control with Harmonic Component Injection

In this section, the possibility of multi-module NPC inverters with the second harmonic voltage injection method was analyzed [25]. The offset voltage injection method is a useful way to reduce the neutral-point voltage difference, and this method has the advantage of easy implementation.

The main concept of Reference [25] was to adjust the ON/OFF states of each inverter's switching legs by synthesizing a phase voltage reference and offset voltage which composed of second harmonics or the half-wave of second-harmonics and the DC-link capacitor voltage error. The synthesized pole voltage for legs of an NPC inverter can be describes as follows [25].

$$\begin{cases} v_{A0} = 0.5v_g + v^*_{offset} & (1) \\ v_{B0} = -0.5v_g + v^*_{offset}. & (2) \end{cases}$$

At this time, since the injection voltage, v_{offset}*, does not affect the phase voltage reference, v_{g}*, of the entire inverter system, it is widely used because the DC-link capacitor voltage balancing can be achieved by an appropriate selection of the offset voltage. In Reference [25], the offset voltage was selected which consists of a second harmonic component and a DC-link capacitor voltage difference. When the offset voltage is selected as described above, the individual pole voltage reference changes, as shown in Figure 1, by the offset voltage to reduce the DC-link voltage error.

However, this offset voltage injection method limits the value of the offset voltage level by the voltage difference between the upper capacitor and the lower capacitor of NPC inverter module. This limitation is caused by the DC-link capacitor voltage error. If the synthesized pole voltage exceeds the limitation, the PWM linearity could be broken.

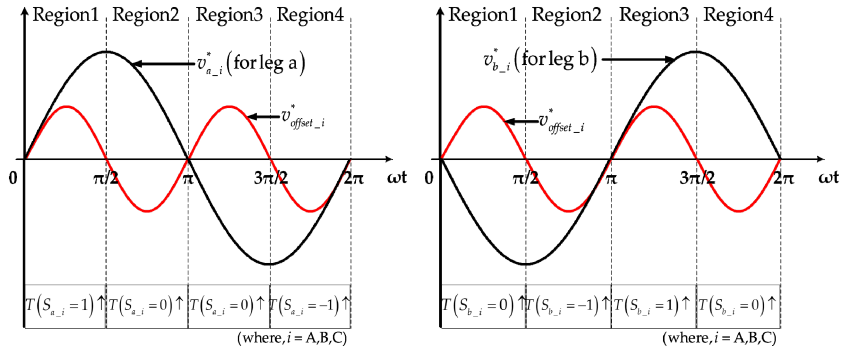


Figure 1. Waveforms pole voltage reference. Voltage, v_g*; offset voltage, v_{offset}*.

To maintain PWM linearity, the offset voltage can be calculated by differentiating the pole voltage reference v_{A0}* and v_{B0}*, which is described in Equations (3) and (4).

$$\begin{cases} v^*_{A0} = \frac{1}{2}v^*_g + K\sin(2\omega t) & (3) \\ v^*_{B0} = -\frac{1}{2}v^*_g + K\sin(2\omega t). & (4) \end{cases}$$

where ω, m and K are the fundamental electrical angular frequency of the grid voltage v_g, modulation index, and the injection gain of the second harmonic voltage, respectively.

For the pole voltage v_{A0}*, the results of the differential can be obtained as follows.

$$\frac{dv^*_A}{d\omega t} = \frac{1}{2}mv_c\cos(\omega t) + 2K\cos(2\omega t). \quad (5)$$

$$\omega t = \begin{cases} \pi - \text{acos}\left(\left(m - \sqrt{(32K^2 + m^2)}\right)/8K\right) & (6) \\ \pi + \text{acos}\left(\left(m + \sqrt{(32K^2 + m^2)}\right)/8K\right) & (7) \\ \pi + \text{acos}\left(\left(m - \sqrt{(32K^2 + m^2)}\right)/8K\right) & (8) \\ \pi - \text{acos}\left(\left(m + \sqrt{(32K^2 + m^2)}\right)/8K\right) & (9) \end{cases}$$

Among these four roots, the maximum value and the minimum value exists as follows.

$$\begin{aligned} \omega t_{\min} &= \pi + \text{acos}\left(\left(m + \sqrt{(32K^2 + m^2)}\right)/8K\right) \\ \omega t_{\max} &= \pi - \text{acos}\left(\left(m + \sqrt{(32K^2 + m^2)}\right)/8K\right) \end{aligned} \quad (10)$$

Equations (7) and (8) determine the limiting region of the offset voltage. If these equations are multiple roots, the PWM linearity could not maintained. Consequently, the DC-link capacitor voltage balancing control would be a failure.

3. DC-Link Capacitor Voltage Balancing Method for a Multi-Module NPC Inverter

In the case of a multi-module NPC inverter, three-level NPC inverters are cascaded to correspond to HV applications. In this case, the inverter input voltage also increased by 3N + 2 depending on the number of cascaded NPC modules N, so that an input voltage closer to the sinusoidal waveform could be formed. However, when the NPC circuit was cascaded as shown in Figure 2, the problem of a capacitor voltage error occurring in the separated DC-link capacitor occurred, which is the main disadvantage of the NPC structure. In Figure 2, the additional resistive load R_{add} could be attached

to the upper side capacitor or the lower side capacitor of DC-link for forcing the DC-link capacitor voltage imbalance.

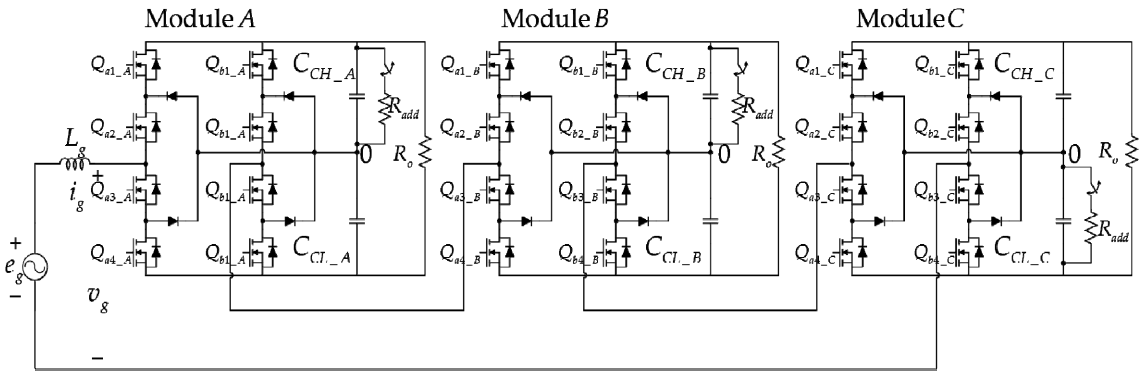


Figure 2. Single-phase three-level neutral-point-clamped (NPC) converter with additional switch circuit on the upper capacitor.

In order to solve this problem, the offset voltage injection method analyzed in Section 2 was applied to the multi-level NPC inverter circuit. The proposed DC-link capacitor voltage balancing control is as follows. First, the phase voltage reference, v_g*, of each NPC inverter module was generated on the basis of the first module of the cascaded NPC inverter. Then, the pole voltage reference, v_{A0_j}* and v_{B0_j}* (where j = A, B, C), for the individual modules were generated using the phase voltage reference v_g* and the DC-link capacitor voltage error of each module, respectively. Finally, the synthesized pole voltage references were compared with the phase-shifted carrier signal, v_{carr_A}, v_{carr_B} and v_{carr_C}, in accordance with the order each module was to perform the switching operation.

For maintaining PWM linearity of each module, the differential of each pole voltage reference was calculated. The results of calculation can be denoted as Equations (11)–(22).

$$\omega t_A = \begin{cases} \pi - \operatorname{acos}\left(\left(m_A - \sqrt{(32K_A^2 + m_A^2)}\right)/8K_A\right) & (11) \\ \pi + \operatorname{acos}\left(\left(m_A + \sqrt{(32K_A^2 + m_A^2)}\right)/8K_A\right) & (12) \\ \pi + \operatorname{acos}\left(\left(m_A - \sqrt{(32K_A^2 + m_A^2)}\right)/8K_A\right) & (13) \\ \pi - \operatorname{acos}\left(\left(m_A + \sqrt{(32K_A^2 + m_A^2)}\right)/8K_A\right) & (14) \end{cases}$$

$$\omega t_B = \begin{cases} \pi - \operatorname{acos}\left(\left(m_B - \sqrt{(32K_B^2 + m_B^2)}\right)/8K_B\right) & (15) \\ \pi + \operatorname{acos}\left(\left(m_B + \sqrt{(32K_B^2 + m_B^2)}\right)/8K_B\right) & (16) \\ \pi + \operatorname{acos}\left(\left(m_B - \sqrt{(32K_B^2 + m_B^2)}\right)/8K_B\right) & (17) \\ \pi - \operatorname{acos}\left(\left(m_B + \sqrt{(32K_B^2 + m_B^2)}\right)/8K_B\right) & (18) \end{cases}$$

$$\omega t_C = \begin{cases} \pi - \text{acos}\left(\left(m_C - \sqrt{(32K_C^2 + m_C^2)}\right)/8K_C\right) & (19) \\ \pi + \text{acos}\left(\left(m_C + \sqrt{(32K_C^2 + m_C^2)}\right)/8K_C\right) & (20) \\ \pi + \text{acos}\left(\left(m_C - \sqrt{(32K_C^2 + m_C^2)}\right)/8K_C\right) & (21) \\ \pi - \text{acos}\left(\left(m_C + \sqrt{(32K_C^2 + m_C^2)}\right)/8K_C\right) & (22) \end{cases}$$

At this time, maximum and minimum values that can be injected to each module are as follows.

$$\begin{aligned} \omega t_{\text{min\_}A} &= \pi + \text{acos}\left(\left(m_A + \sqrt{(32K_A^2 + m_A^2)}\right)/8K_A\right) \\ \omega t_{\text{max\_}A} &= \pi - \text{acos}\left(\left(m_A + \sqrt{(32K_A^2 + m_A^2)}\right)/8K_A\right) \end{aligned} \quad (23)$$

$$\begin{aligned} \omega t_{\text{min\_}B} &= \pi + \text{acos}\left(\left(m_B + \sqrt{(32K_B^2 + m_B^2)}\right)/8K_B\right) \\ \omega t_{\text{max\_}B} &= \pi - \text{acos}\left(\left(m_B + \sqrt{(32K_B^2 + m_B^2)}\right)/8K_B\right) \end{aligned} \quad (24)$$

$$\begin{aligned} \omega t_{\text{min\_}C} &= \pi + \text{acos}\left(\left(m_C + \sqrt{(32K_C^2 + m_C^2)}\right)/8K_C\right) \\ \omega t_{\text{max\_}C} &= \pi - \text{acos}\left(\left(m_C + \sqrt{(32K_C^2 + m_C^2)}\right)/8K_C\right) \end{aligned} \quad (25)$$

Figure 3 shows a multi-level NPC inverter control block diagram with the offset voltage generator for the DC-link capacitor voltage balancing control. In the proposed DC-link capacitor voltage balancing method, only one controller for DC-link voltage and input current was used and the balancing operation was performed by the capacitor voltage error of each module, so the implementation was simple and the responsibility of the control was guaranteed.

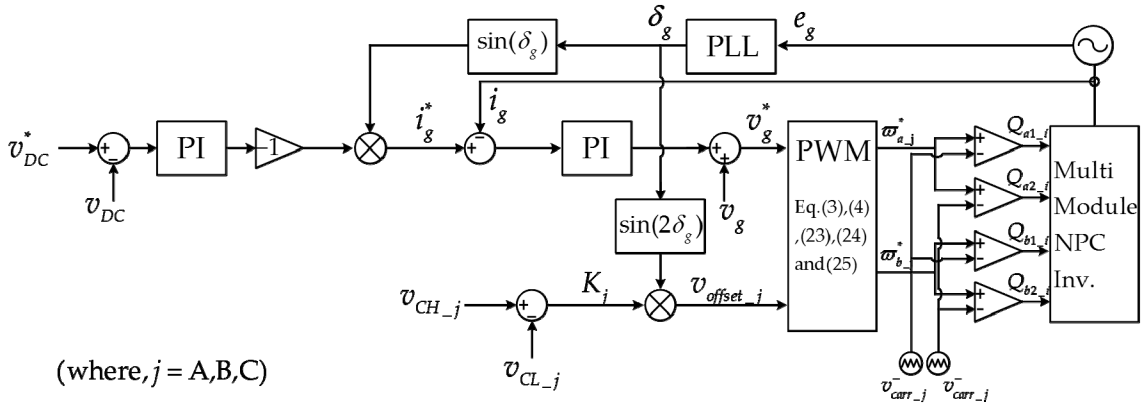


Figure 3. Proposed multi-level NPC inverter control block with offset voltage generator.

4. Simulations and Simulation Results

In order to verify the DC-link capacitor voltage balancing method for multi-module NPC inverters, a 3-kW simulation model has been configured by using PSIM. The simulation consists of three-level NPC modules cascaded in series as shown in Figure 4. In order to force the DC-link capacitor voltage imbalance of each module, the additional resistive load has been connected to capacitors C_{CH_A}, C_{CH_B}, and C_{CL_C}, respectively. The control and the hardware specifications of each NPC inverter module are as follows.

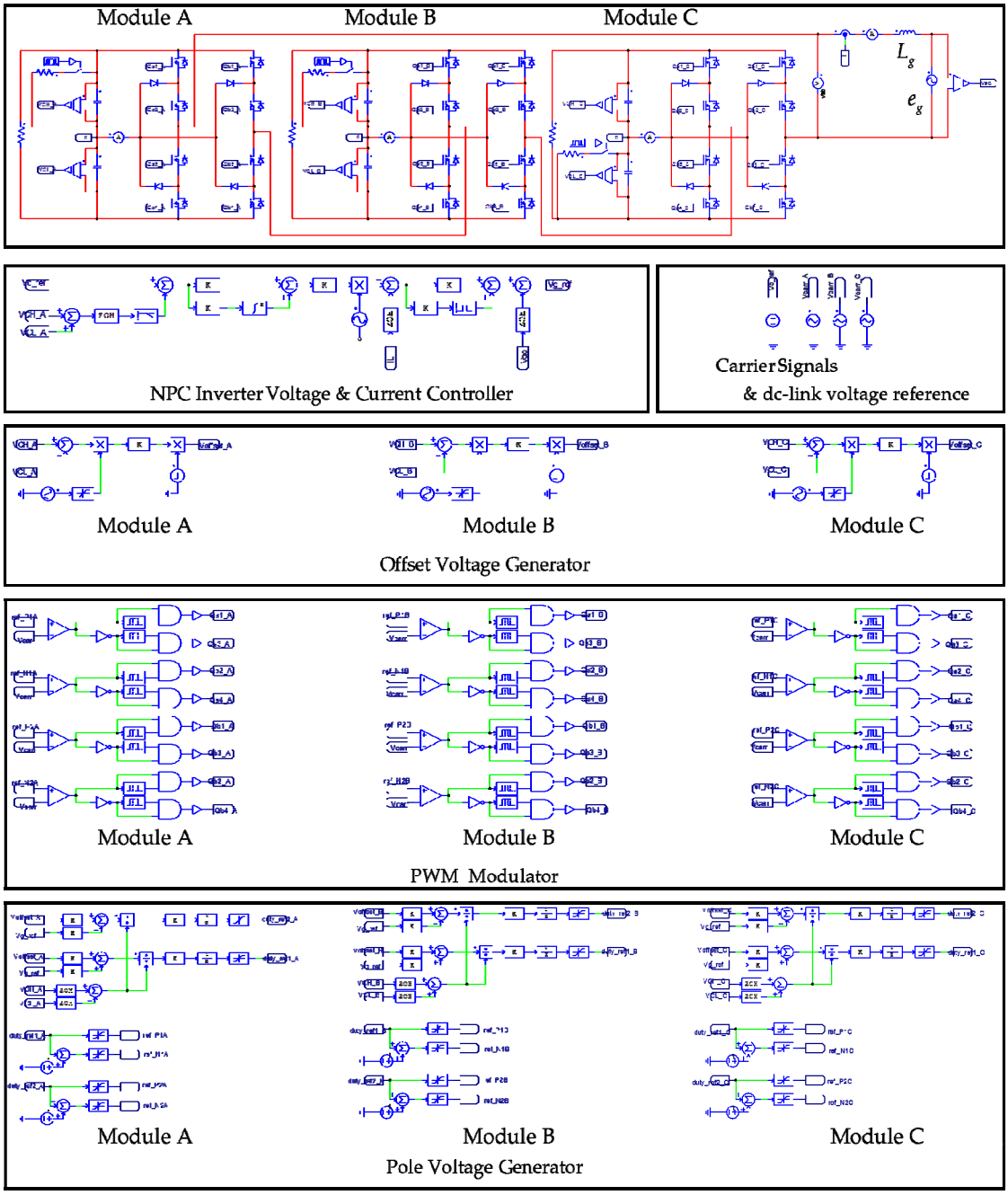


Figure 4. Proposed multi-level NPC inverter control block with offset voltage generator.

The controller configured to control the multi-module inverter consists of a current controller in the inner loop and a DC-link voltage controller in the outer loop. The current controller used the proportional-resonant (PR) controller with an excellent control performance for the AC input power, and the proportional-integral (PI) controller was used for the DC-link voltage controller. In addition, an offset voltage generator composed of the capacitor voltage errors of each DC-link capacitor and second harmonic of the grid-side frequency was configured to decrease the voltage errors of each NPC module.

The control process of the DC-link capacitor of the multi-module inverter is as follows. First, the phase voltage reference, v_g*, of the NPC inverter module was generated based on the DC-link voltage of the first module of the multi-module NPC inverter. At this time, the offset voltage generator made the injection voltage, v_{offset_j}* (where, j = A, B, C), through the DC-link capacitor voltage error of

each NPC module. Then, the phase voltage reference of the inverter module, v_g*, and the injection voltage of each module were synthesized to generate a new pole voltage reference, v_{a0_j}* and v_{b0_j}* (where, j = A, B, C), for operating the respective module legs. The pole voltage references were compared with the carrier signals, v_{carr_A}, v_{carr_B}, and v_{carr_C}, respectively. Those phases of each carrier signal were delayed by 60 degrees, thereby determining ON/OFF states of the respective module switches. If there were no voltage differences between each DC-link capacitor, the multi-module NPC inverter was controlled so that each DC-link voltage was $1/3\ v_{dc}$ according to phase voltage reference v_g*. On the other hand, if there were capacitor voltage errors in the NPC module, an offset voltage, v_{offset_j}*, was synthesized with the phase voltage reference v_g* to reduce the DC-link capacitor voltage imbalance.

The parameters for the proposed balancing control were obtained as follows. The DC-link capacitor voltage of each module which is represented as v_{CH_j} and v_{CL_j} (where, j = A, B, C), and input current, i_g, were measured with a voltage and current sensor, respectively. The phase angle of grid-side, δ_g, was obtained through the PLL block. At this time, the obtained phase angle was used to generate the phase voltage reference for the NPC inverter, v_g*, and the second harmonic was used for DC-link capacitor voltage balancing.

In order to intuitively see the proposed method of each NPC module, an imbalanced condition was forcibly created by using the additional resistive load which connected to each capacitor. The additional resistive load was connected at t = 0.02 s using a switch, and the switch reopened at t = 0.04 s to create a DC-link capacitor voltage imbalance. At this time, the generated voltage differences are −56.5 V in module A, −49.1 V in module B, and 64.5 V in module C, respectively.

The simulation results of the DC-link voltage control of a multi-module NPC inverter are shown in Figure 5. From the simulation results, it can be seen that the DC-link voltage of each module is controlled to 300 V for the input voltage of 471 V in the root-mean-square value (RMS), and it can be confirmed that the input voltage of the module is level 11. However, from the viewpoint of the DC-link capacitors of each module, it can be seen that the voltage error between the upper capacitor and the lower capacitor increased with time. In this case, it was difficult to supply stable power to each load, as it could cause instability of the inverter. So, DC-link capacitor voltage balancing control is required.

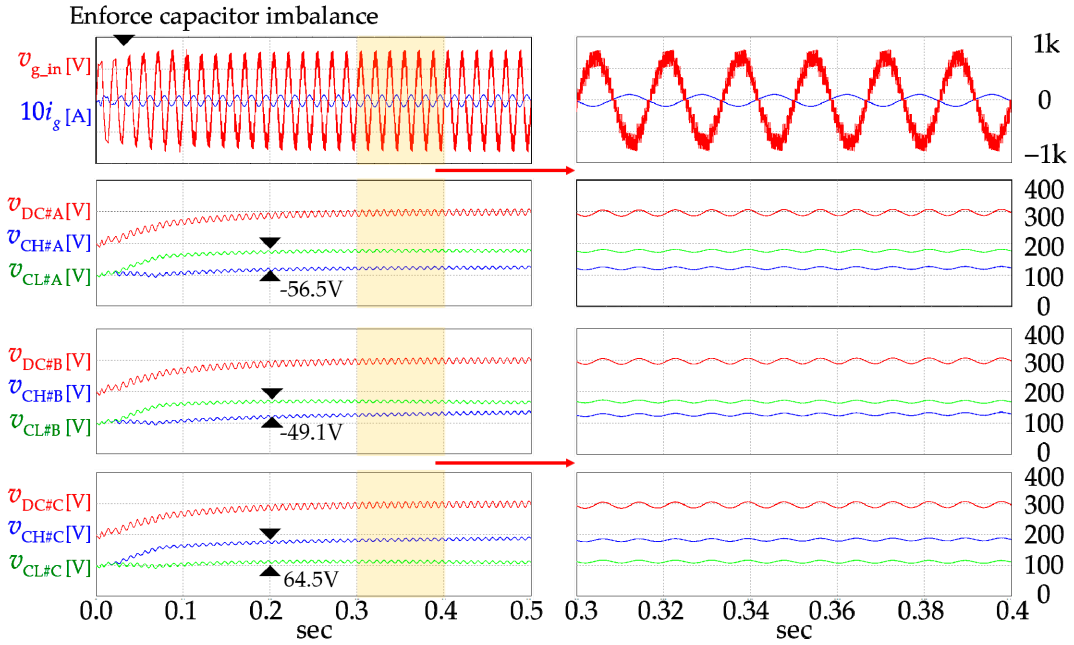


Figure 5. DC-link voltage control of multi-module NPC inverter without voltage balancing control.

Figure 6 shows the simulation results that adopted proposed DC-link capacitor voltage balancing control of a multi-module NPC inverter. As shown in Figure 6, DC-link capacitor voltage balancing

control is adopted at t = 0.2 s. Even when the proposed method was applied, it can be confirmed that the DC-link voltages of each module were controlled to 300 V and had level 11 voltage waveform, the same as in the simulation result of Figure 5. In addition, each capacitor voltage, v_{CH_j} and v_{CL_j} (where j = A, B, C), reached a balanced point at t = 0.5 s. The capacitor voltage differences of each module were reduced from −56.5 V to −2.47 V in module A, −49.1 V to −0.02 V in module B, and 64.5 V to 5.48 V in module C, respectively.

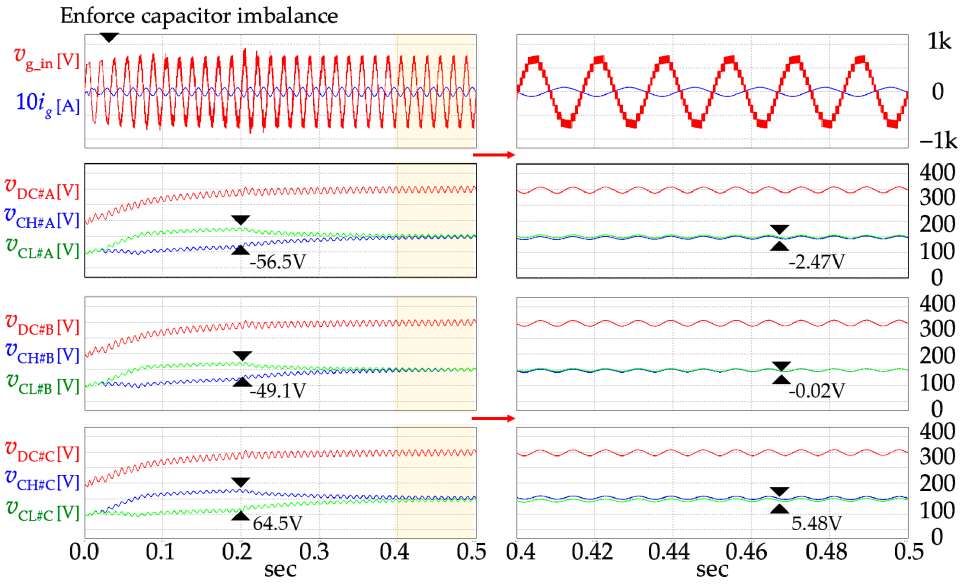


Figure 6. DC-link voltage control of multi-module NPC inverter with voltage balancing control.

5. Experiments and Experimental Results

The performance of DC-link capacitor voltage balancing control of a multi-module NPC inverter which was verified by simulation was tested through the experiments. Figure 7 shows the hardware configuration of the NPC inverter with cascaded three modules which were used in the experiment. Each NPC inverter module consists of two half bridges and two series capacitors. In addition, 3-kW loads were connected to each module.

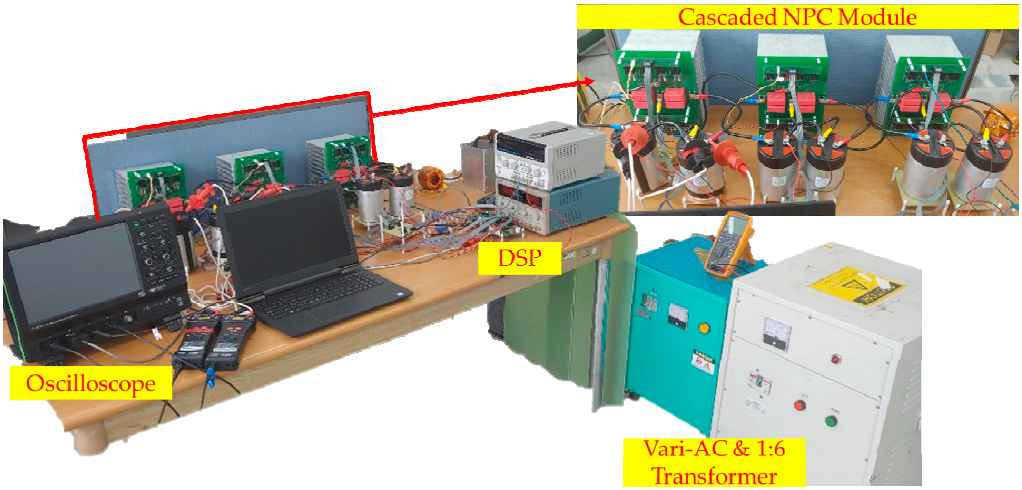


Figure 7. Hardware configuration for cascaded multi-module NPC inverter.

In the experiments, all parameters of the NPC inverter module were composed with the same specifications as the simulation. The power source for the inverter module used a vari-AC connected to a 1:6 transformer to generate 943 VAC. The specifications of the elements constituting each NPC module

are shown in Table 1. All power switching devices and clamping diodes of the NPC module used silicon-carbide. These power devices are Cree's SiC MOSFET C2M0080120D. SiC based power switches can increase the switching frequency more than Si-based power semiconductors, and consequently they could reduce the size of the magnetic components configured in the system. In addition, since the heat capacity of the SiC-based power device is larger than that of the Si-based power device, there was the advantage of the system heat radiation design being convenient. The DC-link capacitors of each module, C_{CH_j} and C_{CL_j} (where, j = A, B, C), used AVX's film capacitor, FFLI-6Q0149K, and the capacitance of FFLI-6Q0149K was 250 μF. In addition, the input filter inductance, Lg, was 14 mH. The digital control board was used to control the NPC module and to process the measured variables. For these controllers, a board made in-laboratory, based on Texas Instrument's TMS320F28335 chipset was used. In order to measure the DC-link capacitor voltages and input current, a differential probe and a current probe were used. For each probe of the DC-link capacitor, PINTEK's high voltage differential probe DP-50 was used. In addition, for measuring input current, Lecroy's current probe CP150 was used.

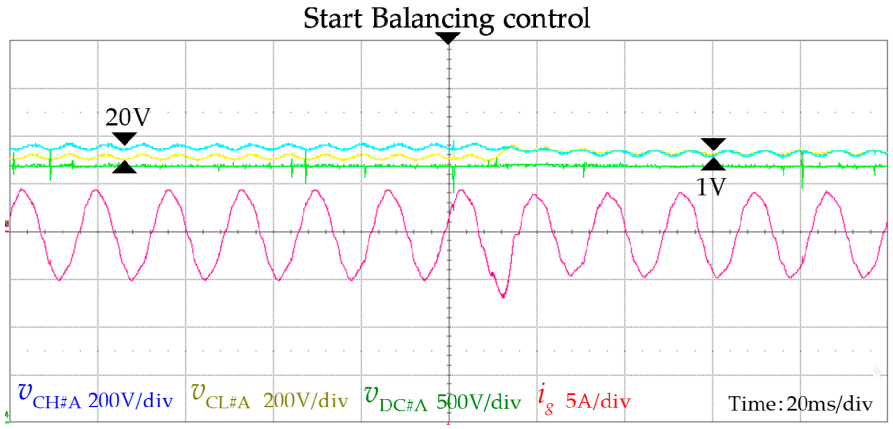
Table 1. Parameter specifications of the NPC inverter.

Parameter	Value	Quantity
Switches	1.2 kV/60 A	24
Clamped Diodes	1.2 kV/33 A	12
Filter Inductor	14 mH	1
Capacitors	250 μF	6

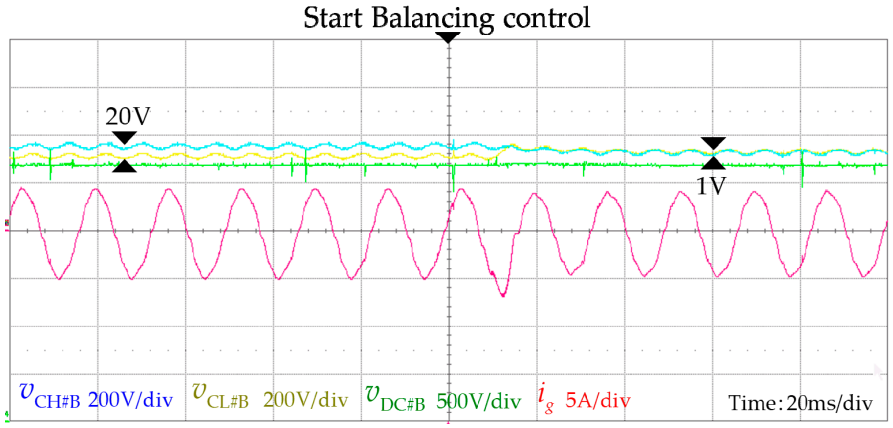
By using the experimental set up above, the experiment for DC-link capacitor voltage balancing control was performed in the following order. First, the input voltage connected to the series-connected NPC inverter module was increased to 943 V in RMS value. At this time, the NPC inverter module controlled the DC-link voltage to 300 V (total 900 V) based on the module A. Then, an additional resistive load which attached to the capacitor of each module was connected to the module to force each module's DC-link capacitor voltage imbalance. At this time, the forced DC-link capacitor voltage difference should not have exceeded the voltage rating of the DC-link capacitor. Finally, after applying the proposed balancing control, the DC-link capacitor imbalance of each module and the input current distortion was continuously observed.

The experimental results of the proposed DC-link capacitor voltage balancing control are shown in Figure 8. Figure 8a–c show the results of applying the proposed method with the imbalance of individual capacitors forced by attaching an additional resistive load to each module. In Figure 8a, there was a capacitor voltage difference of about 20 V between the upper capacitor and the lower capacitor due to the operation of an additional load which connected to the upper capacitor of module A. At this point, the upper capacitor voltage was about 341.7 V and the lower capacitor voltage was about 319.8 V. When the proposed method was applied, the DC-link capacitor voltage difference was reduced to 95% from 20 V to 1 V within about 40 ms. At the start of the balancing control, the input current was slightly distorted, but as the capacitor voltage reached the balancing point, the input current recovered a sinusoidal waveform. In the other modules B and C, the DC-link capacitor voltage was kept constant about 300 V as the DC-link voltage reference, and the capacitor voltages of modules B and C were also maintained constant. In Figure 8b, there were capacitor voltage differences of about 22 V in module A, and 15 V in module B, respectively. In this case, when the proposed balancing control was applied, the DC-link capacitor voltages of each modules were reduced about 95% (100 V to 10 V) in module A, and 87% (15 V to 2 V) in module B. The DC-link voltage of module C was also maintained constant as the above test. Figure 8c shows the results of the proposed balancing method when the voltage imbalance condition has been forced on all modules by using an additional load. As in above experiments, the DC-link voltage differences were reduced about 90% (20 V to 1 V) in module A, and 87% (15 V to 2 V) in module B, and 95% (20 V to 1 V). In case of input current, the input

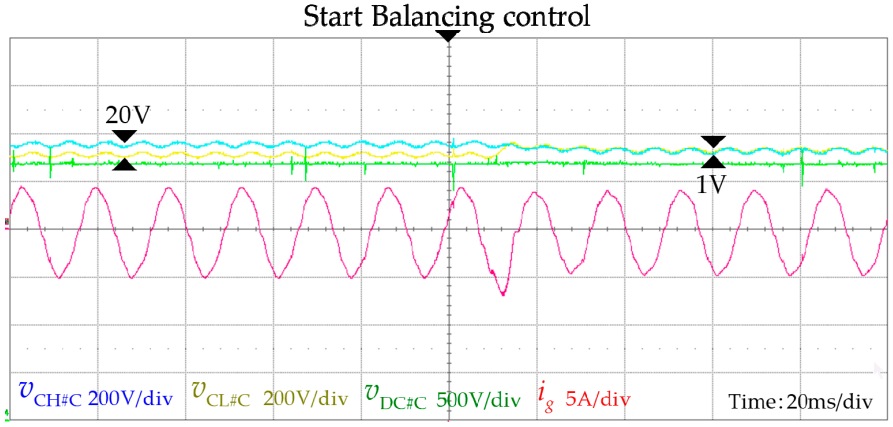
current distortion was small in Figure 8a. However, if the capacitor voltage imbalance condition occurs in each module, the input current distortion tends to increase in the balancing process. This is because the phase voltage reference of each module changes individually due to the injected offset voltage for balancing the capacitor voltage.



(**a**)



(**b**)



(**c**)

Figure 8. Experimental results of multi-level NPC inverter with proposed capacitor voltage balancing method: (**a**) capacitor voltage imbalance condition in module A; (**b**) capacitor voltage imbalance condition in module B; and (**c**) capacitor voltage imbalance condition in module C.

From the simulation and experimental results, the proposed method can compensate the DC-link capacitor voltage imbalance for the multi-level NPC inverter. The proposed method can compensate the DC-link capacitor voltage error in the same manner as that applied in a single-phase three-level NPC module. However, as the number of NPC modules increase, the input current distortion also increases. This is because the distorted input currents, which occurs during the capacitor voltage balancing of module B and module C are added to the distorted current for module A.

6. Conclusions

This paper described the DC-link capacitor voltage error compensation method for multi-module NPC inverters. The proposed compensation method is based on the offset voltage injection technique, and the offset voltage consisted of the capacitor voltage error of each NPC module and double-frequency of the grid.

The proposed method does not require complex calculations and additional hardware setup for DC-link capacitor voltage compensation. It is, therefore, more convenient and intuitive to implement than other offset voltage injection methods. However, the disadvantage of the proposed method that it can be controlled only within the limited injection voltage range. This limitation is related to the maximum and minimum values of the pole voltage which synthesized the phase voltage reference and the offset voltage. If the injection voltage exceeds this limit, the proposed DC-link capacitor voltage compensation method does not guarantee the operation of the NPC inverter module.

Simulations and experiments were performed by using a 3-kW NPC inverter module. In addition, based on simulations and experimental results, the validity and feasibility of the proposed balancing control for the multi-module NPC inverter is verified. The proposed method for multi-module capacitor voltage balancing can be adopted for other topologies that have separated DC-link capacitors like T-type topology.

Author Contributions: K.-P.K. implemented the system and performed the experiments. Y.C. managed the paper. H.-S.K. and J.-w.B. assisted the idea development and the paper writing.

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