

Article

# Transformerless High Step-Up DC-DC Converters with Switched-Capacitor Network

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**Abstract:** High-voltage gain conversion is necessary for several applications, especially for low voltage renewable source applications. In order to achieve a high-voltage gain, the presented paper proposes a class of transformerless DC-DC converters based on three switched-capacitor networks. The proposed converters have the following characteristics: reduced voltage stress on the capacitors and power devices; obtained high voltage gain with small duty cycle; and reduced conduction losses in the power switches. To verify the operation principle of the proposed converters, the detailed analysis in different conditions of the proposed converters and a comparison considering existing topologies are also discussed in the paper. Moreover, the parameter selection and controller design for the converters are determined. Finally, to reconfirm the theoretical analysis, both the simulation and experimental results taken from a 400 W prototype operating at 60 kHz are given.

**Keywords:** transformer-less topology; high-voltage gain; switched-capacitor; two-switch; boost converter

## 1. Introduction

Nowadays, we are facing global surface temperature, the energy crisis and environmental pollution problems. Hence, the use of renewable energy applications is imperatively developed as the most-effective solution. Among various renewable energy sources, photovoltaic (PV) cell, fuel cell (FC) stacks and wind energy have been considered to generate power, as presented in [1]. However, the output of PV, FC cells or wind energy is typically an unregulated, low-level DC voltage and has some drawbacks in [2,3]. Thus, a high step-up voltage gain DC-DC converter is needed to boost to a regulated higher DC voltage bus (200 V or 400 V). Furthermore, the demand for a high boost DC-DC converter has been developed rapidly and popularly. Many high boost DC-DC converters have widely developed and evaluated to find a high-voltage gain in both isolated and non-isolated structures. For the isolated structure, a high-frequency (HF) transformer is added to provide the galvanic isolation between the input and the output with DC/AC and AC/DC power conversions. The isolated DC-DC converters are one of those kinds of converters in which the high voltage gain of the converter can be achieved by adjusting the transformer's ratio [4–9]. Nevertheless, the isolated DC-DC converters have some disadvantages: a high turn ratio is required for high voltage gain applications, which causes more conduction loss of the transformer; the leakage inductance of HF transformer produces voltage spikes across the semiconductor devices; and the snubber circuit is required to reduce the spike and recycle the energy.

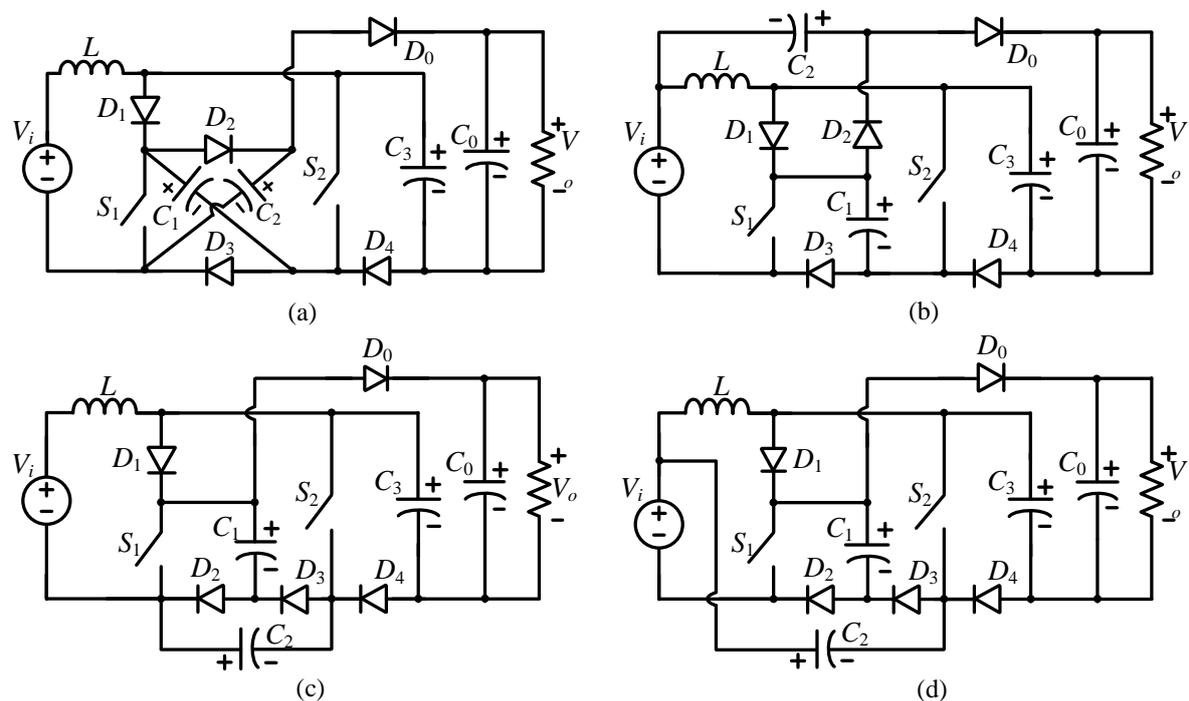
For non-isolated structures, the conventional boost DC-DC converter including two semiconductors (one switch and one diode), one inductor and one capacitor is commonly provided to convert a low voltage source into a high DC-bus voltage with simple circuit and low cost. In practice, the voltage gain of the conventional boost converter is limited by the parasitic components. In order to improve the boost ability, the conventional DC-DC converters based on coupled inductor were proposed in [10–13], however, the leakage problem of the coupled inductor will be caused negative impact for converters. On the other hand, without coupled-inductor structures, the conventional DC-DC converters can be connected in series, but it is very complicated due to the number of switches and control units. For example, the cascade Cockcroft-Walton voltage multiplier was applied to a non-isolated DC-DC converter in [14]. Up to now, many step-up DC-DC converters have proposed to achieve high voltage ratios without isolated transformers or couple inductors. Among these high step-up converters, the quadratic boost converter was proposed in [15] to get high voltage with wide rate of changes using the minimum number of switches. Moreover, some other techniques for high step-up conversions are developed such as interleaved technique [16], voltage multiplier cells [17], switched-inductor cells [18], switched-capacitor cells [19–21] or a hybrid of them. The boost ability of transformer-less DC-DC converters in [14–21] is limited because the duty cycle  $D$  is varied within a wide range of 0 to 1. When a high boost voltage ability is necessary, the large value of  $D$  is reached to 1, this result leads to high conduction loss on the power switches.

In order to provide the boost ability and reduce the duty cycle of the switches in the range of 0 to 0.5, the transformer-less DC-DC converter with Z-source network, which combines two capacitors and two inductors connected in an X-shape, has been presented in [22]. However, the Z-source DC-DC converter operates with discontinuous input current. To improve the input current profile, a converter with switched-boost topology has been introduced in [23], hereby an inductor and capacitor were changed by one more active switch and one more diode. Nevertheless, the output voltage gain of the switched-boost converter is not higher than that of the Z-source converter ( $G = 1/(1 - 2D)$ ). In [24], a 3-Z network boost converter with three Z-networks has been proposed to get a high step-up voltage. Nevertheless, a large number of passive components in the Z-network leads to an increase in the size, weight, cost and loss of the converter. According to the advantage of switched-capacitor technique, the DC-DC converter with switched-capacitor-based technique have been proposed in [25–28]. These DC-DC converters can reduce the voltage stress of the capacitors and semiconductors. However, the improvement in the high voltage gain is not very remarkable and may be still not enough for many industrial applications, which come forward a challenge for developing DC-DC converters with even higher voltage gains. In order to further achieve the high voltage gain, a combination of two switched-capacitor cells and energy storage cell has been proposed in [29]. Moreover, a combination of the switched-capacitor cells and switched-inductor cells has been proposed in [30,31]. They still have drawbacks such as a high number of inductors leads to increase the volume, size, cost and reduces the efficiency.

In this paper, a class of high step-up DC-DC converters with three switched-capacitor-networks is proposed and thus named three switched-capacitor-network converters (3-SCNCs). The proposed 3-SCNCs can achieve high gain at low values of the duty cycle and reduce voltage stresses across the capacitors and power devices. Thus, the power switches with low drain-source on-resistance and devices with low nominal voltage can be used in the proposed 3-SCNCs, which in turn reduces the conduction and switching losses. In the next section, the operating principle of the proposed 3-SCNCs in continuous conduction mode (CCM) is given. In Section 3, the proposed converters in both discontinuous conduction mode (DCM) boundary and parasitic components analysis will be accomplished. Section 4 compares the proposed converters with other high voltage gain converters. It is followed by the parameter's selection of the converters in Section 5. In Section 6, the simulation and experimental results with closed-loop controller will be conducted to evaluate the theoretical analysis. Finally, conclusions are given in Section 7.

## 2. Derivation of Proposed 3-SCNCs in CCM

The switched-capacitor-network based converter can provide high voltage gain. By keeping this goal, the basic idea of this paper is to regenerate step-up DC voltage using an inductor and switched-capacitor network during on-state of the switches. The circuit diagram of the proposed 3-SCNCs are depicted in Figure 1. As shown in Figure 1, four proposed converters have the same as several components which contain two power switches ( $S_1, S_2$ ), three switched-capacitor networks  $D_n-C_n$  ( $n = 1-3$ ), one boost inductor, one additional diode, and a pair of output diode-capacitor. To simplify the process of theoretical analysis, the following assumptions were made: an inductor current is continuous, all devices are without the effects of parasitic components, the voltage ripple of capacitors are ignored.



**Figure 1.** Proposed DC–DC converters with three switched-capacitor networks (3-SCNCs): (a) Type 1, (b) Type 2, (c) Type 3 and (d) Type 4.

### 2.1. Operating Principle of the Proposed 3-SCNC Type 1

Figure 2 introduces the key waveforms of the proposed 3-SCNC type 1, where  $D$  and  $T$  are the duty cycle and the switching period. Based on the waveforms, two main operating states are defined at every switching period.

Stage 1- $[t_0-t_1]$ , Figure 3a]:  $S_1$  and  $S_2$  are turned on at  $D \cdot T$ . The inductor is charged by the input DC source and the  $C_1$  capacitor, the  $C_2$  and  $C_3$  capacitors are discharged. The  $D_1, D_2, D_3$  and  $D_4$  diodes are reverse-biased when the  $D_0$  diode is forward-biased. The following equation is written:

$$\begin{cases} L \frac{di_L}{dt} = V_i + V_{C1} \\ V_o = V_{C1} + V_{C2} + V_{C3}. \end{cases} \quad (1)$$

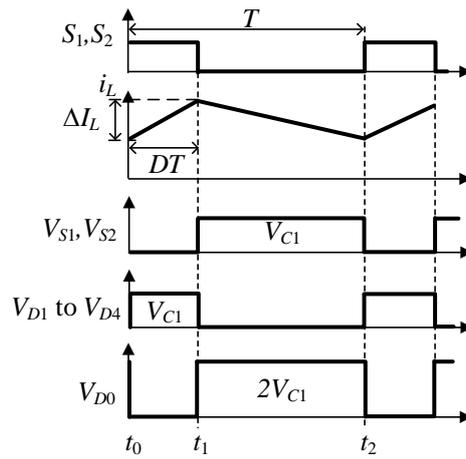


Figure 2. PWM control method for the proposed 3-SCNC type 1 in CCM.

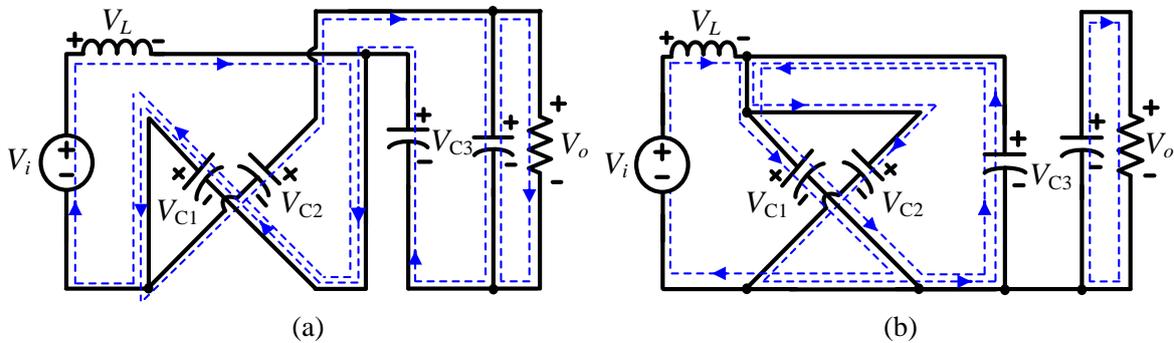


Figure 3. Equivalent circuits of the proposed 3-SCNC type 1. (a) State 1, (b) State 2.

Stage 2- $[t_1-t_2]$ , Figure 3b]:  $S_1$  and  $S_2$  are turned off at the same time  $(1 - D) \cdot T$ ; the  $D_1, D_2, D_3,$  and  $D_4$  diodes are reverse-biased while the  $D_0$  diode is forward-biased. We have

$$\begin{cases} L \frac{di_L}{dt} = V_i - V_{C1} \\ V_{C1} = V_{C2} = V_{C3}. \end{cases} \quad (2)$$

According to the volt-second balance law of the inductor in one switching period, (1) to (2) yield the following equation:

$$V_{C1} = V_{C2} = V_{C3} = \frac{V_i}{1 - 2D'} \quad (3)$$

By substituting (3) to (1), the voltage gain of the proposed 3-SCNC type 1 in the CCM is derived

$$G_{CCM} = \frac{V_o}{V_i} = \frac{3}{1 - 2D'}. \quad (4)$$

### 2.2. Operating Principle of the Proposed 3-SCNC Type 2

Compared to 3-SCNC type 1, the proposed 3-SCNC type 2 has lower voltage stress across capacitor  $C_2$ , as seen in Figure 1b. It can be created by changing the connection of capacitor  $C_2$  to DC-source. According to the PWM method in Figure 2, the equivalent circuit of the proposed 3-SCNC type 2 in CCM operation can be divided into two states, as shown in Figure 4.

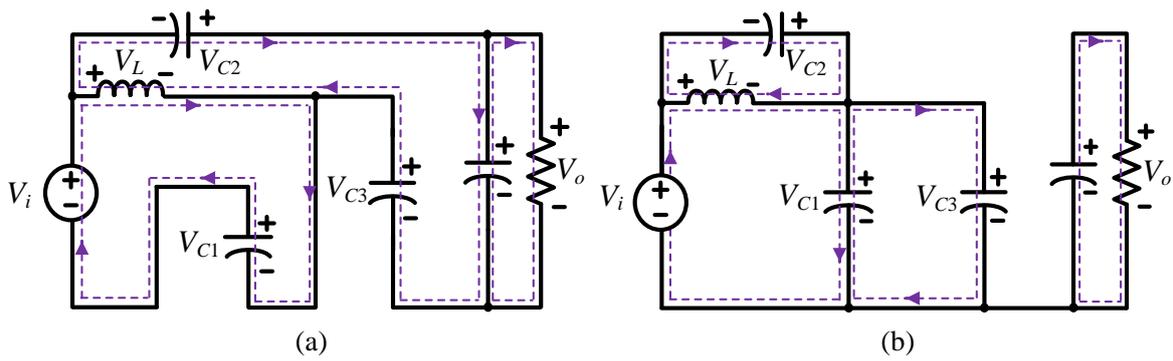


Figure 4. Equivalent circuits of the proposed 3-SCNC type 2. (a) State 1, (b) State 2.

When  $S_1$  and  $S_2$  are turned on, the equations are obtained

$$\begin{cases} L \frac{di_L}{dt} = V_i + V_{C1} \\ V_o = V_i + V_{C1} + V_{C2} + V_{C3}, \end{cases} \quad (5)$$

When  $S_1$  and  $S_2$  are turned off. The extra equations are given

$$\begin{cases} L \frac{di_L}{dt} = -V_{C2} \\ V_{C1} = V_{C3} = V_i + V_{C2}, \end{cases} \quad (6)$$

By applying volt-second balance for the inductor, the voltage of capacitors can be expressed

$$\begin{cases} V_{C1} = V_{C3} = \frac{V_i}{1-2D} \\ V_{C2} = \frac{2DV_i}{1-2D}, \end{cases} \quad (7)$$

By combining (5) and (7), the voltage gain of proposed 3-SCNC type 2 is obtained

$$G_{CCM} = \frac{V_o}{V_i} = \frac{3}{1-2D}. \quad (8)$$

### 2.3. Operating Principle of the Proposed 3-SCNC Type 3

Moreover, the CCM analysis of the proposed 3-SCNC type 3 is also considered with PWM method in Figure 2. The equivalent circuits are shown in Figure 5.

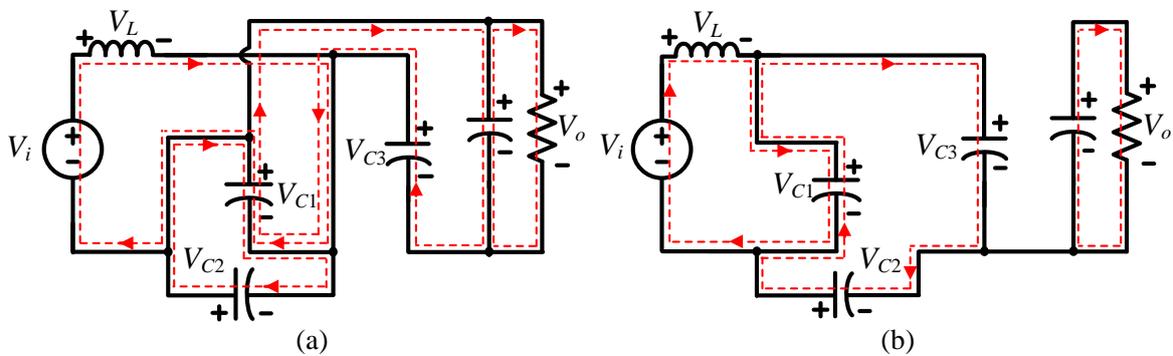


Figure 5. Equivalent circuits of the proposed 3-SCNC type 3. (a) State 1, (b) State 2.

When switches  $S_1$  and  $S_2$  are turned on, the following equations are given

$$\begin{cases} L \frac{di_L}{dt} = V_i + V_{C1} \\ V_o = V_{C1} + V_{C3} = V_{C2} + V_{C3}, \end{cases} \quad (9)$$

When  $S_1$  and  $S_2$  are off. The above equations can be rewritten

$$\begin{cases} L \frac{di_L}{dt} = V_i - V_{C1} \\ V_{C3} = V_{C1} + V_{C2}, \end{cases} \quad (10)$$

At steady state, based on the volt-second relationship of  $L$ , the voltage of capacitors and voltage gain are calculated as

$$\begin{cases} V_{C1} = V_{C2} = \frac{V_{C3}}{2} = \frac{V_i}{1-2D} \\ G_{CCM} = \frac{V_o}{V_i} = \frac{3}{1-2D}, \end{cases} \quad (11)$$

#### 2.4. Operating Principle of 3-SCNC Type 4

Similarly, the proposed 3-SCNC type 4 is also analyzed with two states. The equivalent circuit during state 1 is shown in Figure 6.

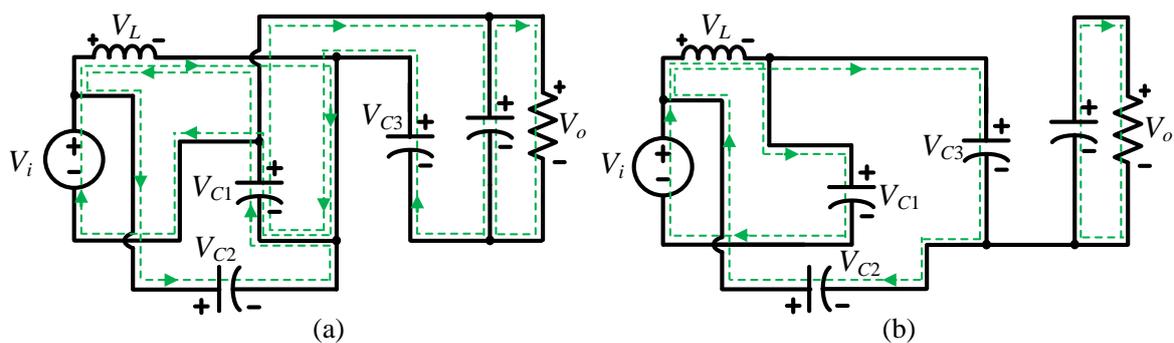


Figure 6. Equivalent circuits of the proposed 3-SCNC type 4. (a) State 1, (b) State 2.

The voltage across the inductor  $L$  and output voltage are given by

$$\begin{cases} L \frac{di_L}{dt} = V_{C2} = V_i + V_{C1} \\ V_o = V_{C1} + V_{C3}, \end{cases} \quad (12)$$

When  $S_1$  and  $S_2$  are turned off. The above equations can be rewritten

$$\begin{cases} L \frac{di_L}{dt} = V_i - V_{C1} \\ V_{C3} = V_{C1} + V_{C2} - V_i, \end{cases} \quad (13)$$

According to the volt-second balance law, from (12) to (13), we have

$$\begin{cases} V_{C1} = \frac{V_i}{1-2D} \\ V_{C2} = \frac{(2-2D)V_i}{1-2D} \\ V_{C3} = \frac{2V_i}{1-2D}, \end{cases} \quad (14)$$

The voltage gain can be obtained as

$$G_{CCM} = \frac{V_o}{V_i} = \frac{3}{1-2D}. \quad (15)$$

### 3. DCM Boundary Condition and Influence of Parasitic Components Analysis

To simplify the analysis process of the proposed 3-SCNCs under different operation conditions, one of the proposed converters, the 3-SCNC type 1 is considered as an example. It is analyzed in detail in DCM operation and a voltage gain analysis with parasitic components is presented. Moreover, the other proposed 3-SCNC's analyses can be determined with the same method.

#### 3.1. DCM Derivation

For the DCM analysis, the key waveforms of the proposed 3-SCNCs in DCM are presented in Figure 7. The voltage across inductor can be written as

$$v_L = \begin{cases} V_i + V_{C1}, & (t_0 - t_1) \\ V_i - V_{C1}, & (t_1 - t_2) \\ 0, & (t_2 - t_3). \end{cases} \quad (16)$$

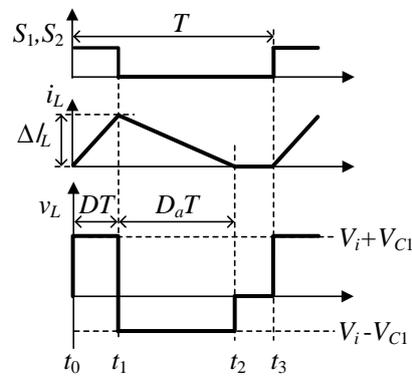


Figure 7. Operating waveform of the proposed 3-SCNCs in DCM.

According to Figure 3a and (1), the peak to peak current ripple of the inductor is calculated

$$\Delta I_L = \frac{V_i + V_{C1}}{L} DT, \quad (17)$$

The average inductor current is the input current and can be determined

$$\bar{I}_L = \bar{I}_{in} = \frac{P_o}{V_i} = \frac{V_o^2}{RV_i}, \quad (18)$$

Based on the condition of DCM as

$$\bar{I}_L < \Delta I_L / 2, \quad (19)$$

Substituting (17) and (18) into (19), we have the results in

$$K < K_{crit}(D), \quad (20)$$

where  $K$  is a normalized coefficient to define the operation mode of the converter, and  $K = 9L/(2RT)$ ,  $K_{crit} = D(1 - D)(1 - 2D)$ .

Referring to Figure 7, the average value of inductor current is determined as follows

$$\bar{I}_L = \frac{V_i + V_{C1}}{2L} D \cdot (D + D_a) \cdot T, \quad (21)$$

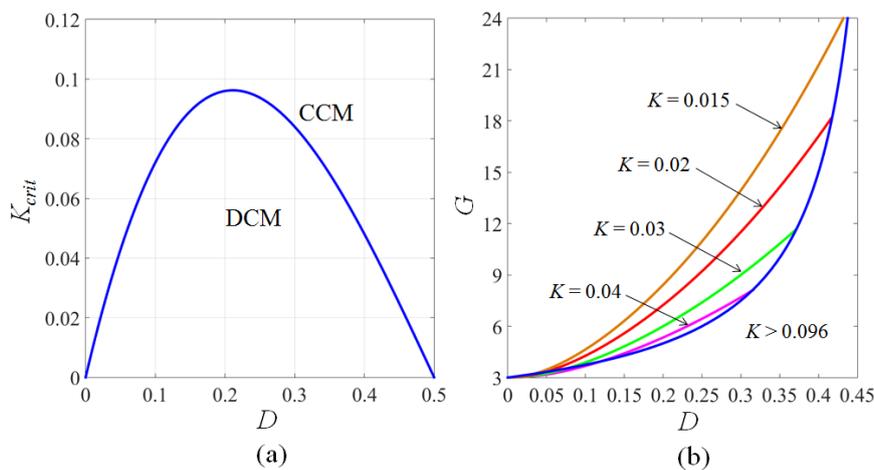
Apply the volt-second balance law of inductor to (16),  $D_a$  can be written as

$$D_a = \frac{D(V_i + V_{C1})}{V_{C1} - V_i}, \tag{22}$$

In terms of (18), (21) and (22), the output voltage gain in DCM is derived as

$$G = \frac{3(D^2 + 2K + \sqrt{D^4 + 12KD^2 + 4K^2})}{4K}, \tag{23}$$

Figure 8a shows the plots of CCM/DCM boundary curve. Then, one can define the operation mode of the proposed 3-SCNC type 1 in CCM when  $K > K_{crit}$ ; otherwise the converter considers with DCM operation. Furthermore, the voltage gains of the proposed 3-SCNC type 1 in DCM are different when the values of duty cycle  $D$  and coefficient  $K$  are changed. Figure 8b shows the voltage gain in DCM with several colored curves with different  $D$  and  $K$ . When  $K < 0.096$ , the converter expresses in CCM and the voltage gain is increased as  $K$  decreases.



**Figure 8.** Operating plot of the proposed 3-SCNC type 1: (a) CCM/DCM boundary condition. (b) Voltage gain with different  $K$ .

### 3.2. Voltage Gain Considering Parasitic Components

To simplify the parasitic verification, the winding resistor of the inductor, the ESR of the capacitors, the conduction resistor of the switches and the diode forward voltage are denoted by  $r_L, r_C, r_S,$  and  $V_D,$  respectively. The equivalent circuit in the conduction interval of each case are shown in Figure 9. Applying the charge-second balance principle to the capacitors, we obtain

$$\begin{cases} i_{C0\_on} = \frac{1-D}{D}I_o \\ i_{C1\_on} = -\frac{1+D}{D(1-2D)}I_o \\ i_{C2\_on} = i_{C3\_on} = \frac{-I_o}{D} \end{cases} \quad \text{and} \quad \begin{cases} i_{C0\_off} = -I_o \\ i_{C1\_off} = \frac{1+D}{(1-D)(1-2D)}I_o \\ i_{C2\_off} = i_{C3\_off} = \frac{I_o}{(1-D)} \end{cases}, \tag{24}$$

In the duration time  $(1 - D)T$ , the capacitors  $C_2$  and  $C_3$  voltage are determined

$$V_{C2} = V_{C3} = V_{C1} + \frac{3DI_o r_C}{(1 - D)(1 - 2D)}, \tag{25}$$

The inductor current can be written

$$I_L = \frac{3V_o}{(1 - 2D)R'}, \tag{26}$$

According to the voltage-second balance on the inductor, we have

$$D[V_i - I_L r_L + i_{C1on}(2r_s + r_c) + V_{C1}] + (1 - D)[V_i - I_L r_L - 2V_D - V_{C1} - i_{C1off} r_c] = 0, \quad (27)$$

Substituting (24)–(26) into (27), the output voltage can be rewritten

$$V_o = \frac{D(1 - D)(1 - 2D)[3V_i - (7 - 8D)V_D]}{D(1 - D)(1 - 2D)^2 + 9D(1 - D)\frac{r_c}{R} + 3(1 - 2D + 3D^2)\frac{r_c}{R} + 2(1 + D)^2(1 - D)\frac{r_s}{R}}, \quad (28)$$

It can be seen that the voltage gain is defeneded on the parasitic parameters. Assuming that  $r_L = 10r_c = 6r_s, k_L = r_L/R$  and  $V_D = 0.01V_i$ . Figure 10 validates the relationship between the gain versus duty cycle when the resistance of the components is increased.

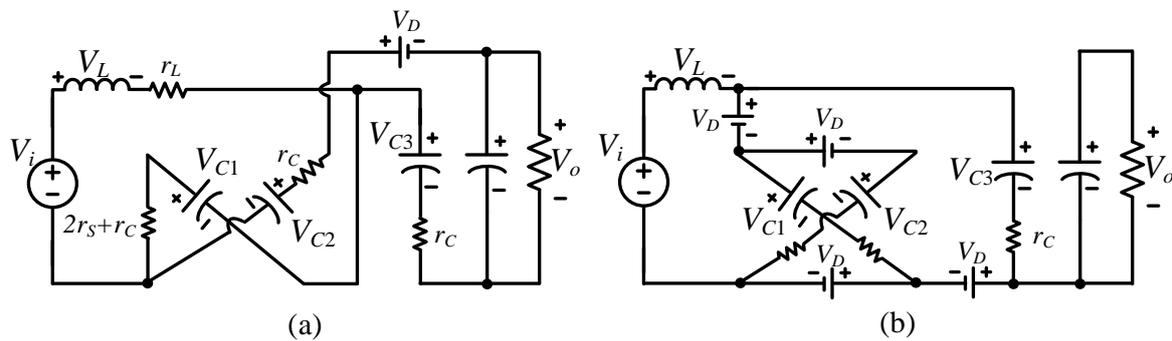


Figure 9. Simplified circuit for parasitic components. (a) State 1, (b) State 2.

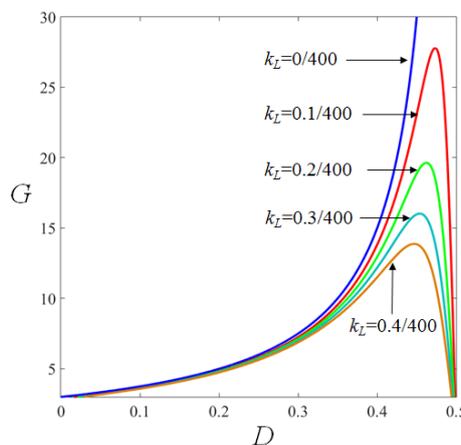


Figure 10. The relationship between the resistance ratio  $r_L/R$  and the voltage gain ratio  $G$ .

Where  $V_{S1}/V_i$  and  $V_{S2}/V_i$  are the drain-source voltage stresses of  $S_1$  and  $S_2$ , respectively.  $V_{Dx}/V_i$  is the voltage stress of diodes ( $x$  is the number of diodes) and  $V_{Cy}/V_i$  is the voltage stress of capacitors ( $y$  is the number of capacitors).

#### 4. Comparison with Other High Step-Up Transformer-Less DC-DC Converter

##### 4.1. Voltage Gain

Currently, research literature is often focused on extending the boost ratio with higher efficiency, decreasing component count, consequently size, weight, losses and minimizing the stresses of component. In order to evaluate the characteristics of the proposed 3-SCNCs, the comparison between the proposed 3-SCNCs and other high step-up transformer-less DC-DC converters are summarized in

Table 1. For better insight, the comparison of voltage gain versus duty cycle is plotted as shown in Figure 11a. It can be noticed that the proposed 3-SCNCs requires the lowest duty cycle for the same voltage gain than that of DIESC-SC [21], 3-ZNC [24], IESC-SC [29], and SL/SC-ANC [30]. When the duty cycle is higher than 0.25, the voltage gain of the proposed 3-SCNCs is lower than SL/SC-SBC [31]. However, the SL/SC-SBC [31] uses two more components.

Table 1. Comparison between the proposed 3-SCNCs and other high boost DC–DC converters.

	3-ZNC [24]	DIESC-SC [21]	IESC-SC [29]	SL/SC-ANC [30]	SC/SL-SBC [31]	3-SCNC Type 1	3-SCNC Type 2	3-SCNC Type 3	3-SCNC Type 4
Ind.	4	2	3	3	2			1	
Cap.	2	5	6	3	3			4	
Di./Sw.	9/1	4/1	5/2	6/2	7/2			5/2	
Total	16	12	16	14	14			12	
$V_{S1}/V_i V_{S2}/V_i$	$G$	$1/(1-D)$	$\frac{1/(1-D)}{1/(1-D)^2}$	$\frac{1/(1-D)}{(1+D)/(1-D)}$	$\frac{2D/(1-3D)}{G/2}$	$G/3$	$G/3$	$\frac{G/3}{2G/3}$	$\frac{G/3}{2G/3}$
$V_{Dx}/V_i$	$\frac{D/(1-D), 1}{(1+D)(1-D)}$ $\frac{2DG/(1+D)}{G}$	$1/(1-D)$	$\frac{1/(1-D)}{1/(1-D)^2}$	$\frac{1}{(2+D)/(1-D)}$ $\frac{D/(1-D)}{D/(1-D)}$	$\frac{G/2}{2D/(1-3D)}$	$\frac{G/3}{2G/3}$	$\frac{G/3}{2G/3}$	$\frac{G/3}{2G/3}$	$\frac{G/3}{2G/3}$
$V_{Cy}/V_i$	$\frac{(1-D)/(1+D)}{G}$	$\frac{1/(1-D)}{D(1-D)}$	$\frac{1/(1-D)}{D/(1-D)^2}$	$\frac{1/(1-D)}{(1+D)/(1-D)}$	$\frac{2D/(1-3D)}{G/2}$	$G/3$	$\frac{G/3}{2DG/3}$	$\frac{G/3}{2G/3}$	$\frac{G/3}{(2-2D)G/3}$ $\frac{2G/3}{2G/3}$
$G$	$\left(\frac{1+D}{1-D}\right)^2$	$\frac{2+D}{1-D}$	$\frac{2+D}{(1-D)^2}$	$\frac{3+3D}{1-D}$	$\frac{2-2D}{1-3D}$	$\frac{3}{1-2D}$	$\frac{3}{1-2D}$	$\frac{3}{1-2D}$	$\frac{3}{1-2D}$
$\Delta I_m$	High	High	High	High	High	Low	High	Low	High

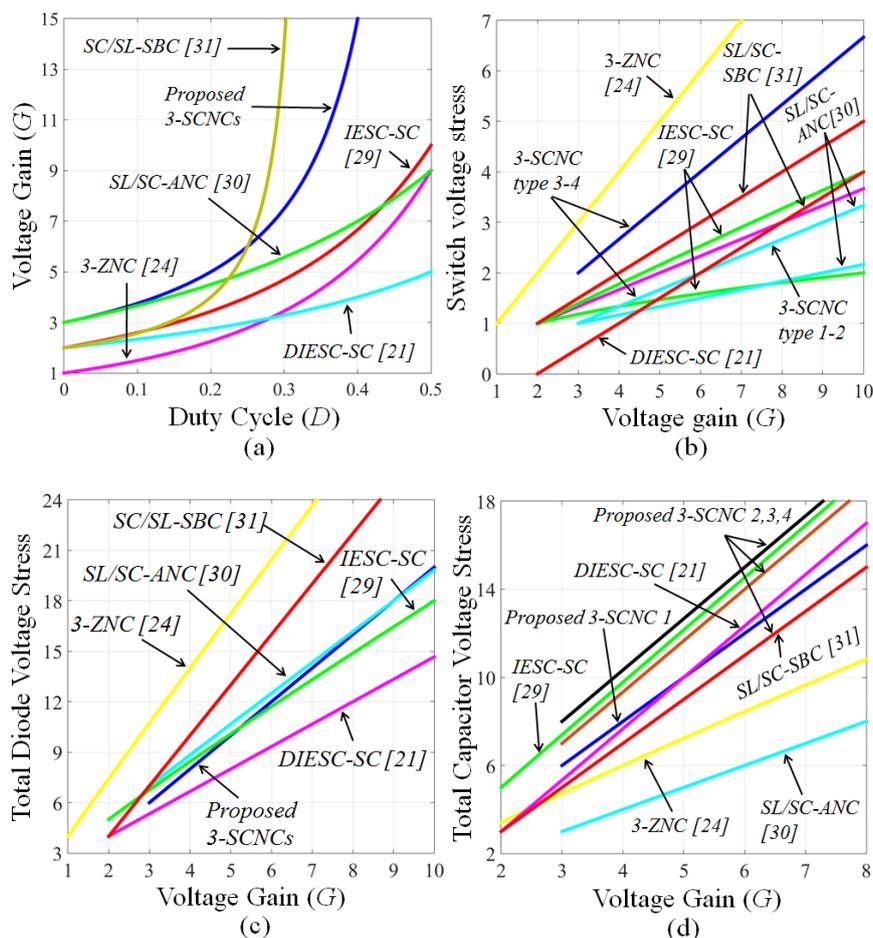


Figure 11. Comparison of (a) Voltage gain, (b) Voltage stress of switch, (c) Voltage stress of diode, (d) Voltage stress of capacitor.

#### 4.2. The Number of Components

Compared to DIESC-SC [21] and 3-ZNC [24], the proposed 3-SCNCs use one more active switch, but reduce a large number of inductors and diodes. In addition, the total number of components used at the proposed 3-SCNCs and DIESC-SC [21] is the same, which is 12. Nevertheless, the proposed 3-SCNCs use one less inductor and capacitor. Compared with the IESC-SC [29], proposed 3-SCNCs have two less inductors, and two less capacitors. The proposed 3-SCNCs contain one more capacitor than the SL/SC-ANC [30] and SC/SL-SBC [31]. However, it has two less inductors, one less diode and one less inductor, two less diodes than that of SL/SC-ANC [30], SC/SL-SBC [31], respectively. Therefore, the size, cost, and weight of the proposed 3-SCNCs are lower than those of other converters.

#### 4.3. Comparison of Stresses and Input Current Ripple

The comparison of the switch voltage stress in these nine converters is shown in Figure 11b. It can be seen that the proposed 3-SCNC type 1, 2 have lower voltage stress than the DIESC-SC [21], 3-ZNC [24], and SL/SC-SBC [26]. Besides, to produce the same output voltage gain, the proposed 3-SCNCs produce a lower switching voltage stress of the diodes than the 3-ZNC [24], SL/SC-ANC [30] and SL/SC-SBC [31], but higher than that of the DIESC-SC [21], IESC-SC [29]. From Figure 11d, it can be observed that the proposed 3-SCNC type 2 has lower capacitors voltage stress than the proposed 3-SCNC 1, 3, 4, DIESC-SC [21], IESC-SC [29], and equal SL/SC-SBC [31]. Moreover, the capacitor voltage stress of the proposed 3-SCNC type 2 has lower than DIESC-SC [21] and IESC-SC [29].

As presented in Table 1, the input current ripple comparison is also discussed. The input current ripple of the DIESC-SC [21], 3-ZNC [24], IESC-SC [29], SL/SC-ANC [30], SL/SC-SBC [31], the proposed 3-SCNC type 2 and 4 are very high. This is because the capacitor, diode or switch is directly connected to DC input voltage. Moreover, in the proposed 3-SCNC type 1 and 3, the inductor is directly connected to the DC input voltage. Thus, the input current ripple of them is low.

### 5. Component Selections

#### 5.1. Inductance Selection

The proposed 3-SCNC type 1 is considered as an example to design the inductor. The inductance is selected by using the current ripple of the inductor in the interval time  $DT$ . From (1) and  $\Delta I_L \leq x\%I_L$ , the required inductance in the CCM can be derived

$$L = \frac{2D(1-D)(1-2D)R}{9x\%f_s} \quad (29)$$

#### 5.2. Capacitance Selection

The capacitors are selected with the rated voltage as presented in Table 1. Moreover, the value of capacitance is designed based on the capacitor voltage ripple. From (24), we have:

$$\left| C_1 \frac{\Delta V_{C1}}{DT} \right| = \frac{1+D}{D(1-2D)} I_o, \quad (30)$$

If the peak-to-peak capacitor voltage ripple is limited by  $y_1\%$ , the rated capacitance of capacitors  $C_1$ ,  $C_2$ , and  $C_3$  can be derived.

$$C_{1,2,3} = \frac{3(1+D)}{y_1\%(1-2D)f_s R'} \quad (31)$$

Similarly, from (24) we have

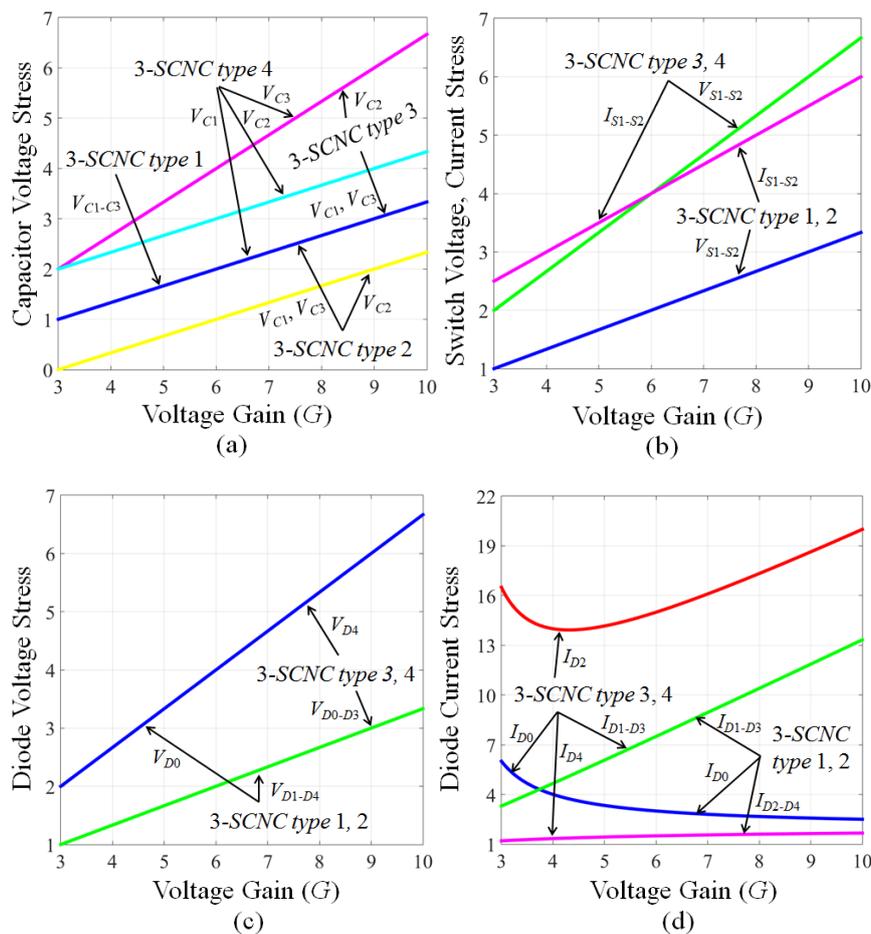
$$\left| C_0 \frac{\Delta V_o}{DT} \right| = \frac{1-D}{D} I_o, \quad (32)$$

The capacitance of  $C_0$  should be calculated as

$$C_0 = \frac{3(1 + D)}{y_0 \% f_s R'} \quad (33)$$

### 5.3. Semiconductor Devices Selection

The voltage and current stresses of the proposed 3-SCNCs are the main constraint in the selection of switches and diodes to maintain them operating in their safe condition, as shown in Table 2. Moreover, the voltage and current stress comparison of the proposed 3-SCNCs for semiconductor device has been shown in Figure 12. Compared to the proposed 3-SCNC type 3-4, the proposed 3-SCNC type 1-2 has lower voltage stress of switches and capacitors.



**Figure 12.** Voltage and current stresses comparison of the proposed 3-SCNCs. (a) Voltage stress of capacitor, (b) Voltage and current stress of switch, (c) Voltage stress of diode, (d) Current stress of diode.

**Table 2.** Voltage and current stresses of the proposed 3-SCNCs.

	Type 1	Type 2	Type 3	Type 4
$V_{C1}/V_i$	$G/3$	$G/3$	$G/3$	$G/3$
$V_{C2}/V_i$	$G/3$	$2DG/3$	$2G/3$	$(2 - 2D)/(1 - 2D)$
$V_{C3}/V_i$	$G/3$	$G/3$	$G/3$	$2G/3$
$V_{S1}/V_i$	$G/3$	$G/3$	$G/3$	$G/3$
$V_{S2}/V_i$	$G/3$	$G/3$	$2G/3$	$2G/3$
$V_{D0}/V_i$	$2G/3$	$2G/3$	$G/3$	$G/3$
$V_{D1}/V_i$	$G/3$	$G/3$	$G/3$	$G/3$
$V_{D2}/V_i$	$G/3$	$G/3$	$G/3$	$G/3$
$V_{D3}/V_i$	$G/3$	$G/3$	$G/3$	$G/3$
$V_{D4}/V_i$	$G/3$	$G/3$	$2G/3$	$2G/3$
$I_{S1}/I_o$	$(1+D)/D(1 - 2D)$	$(1+D)/D(1 - 2D)$	$(1+D)/D(1 - 2D)$	$(1+D)/D(1 - 2D)$
$I_{S2}/I_o$	$(1+D)/D(1 - 2D)$	$(1+D)/D(1 - 2D)$	$(1+D)/D(1 - 2D)$	$(1+D)/D(1 - 2D)$
$I_{D0}/I_o$	$1/D$	$1/D$	$1/D$	$1/D$
$I_{D1}/I_o$	$(2 - D)/(1 - D)(1 - 2D)$			
$I_{D2}/I_o$	$1/(1 - D)$	$1/(1 - D)$	$(2 - D)/D(1 - 2D)$	$(2 - D)/(1 - D)(1 - 2D)$
$I_{D3}/I_o$	$(2 - D)/(1 - D)(1 - 2D)$	$(2 - D)/(1 - D)(1 - 2D)$	$(2 - D)/(1 - D)(1 - 2D)$	$(2 - D)/D(1 - 2D)$
$I_{D4}/I_o$	$1/(1 - D)$	$1/(1 - D)$	$1/(1 - D)$	$1/(1 - D)$

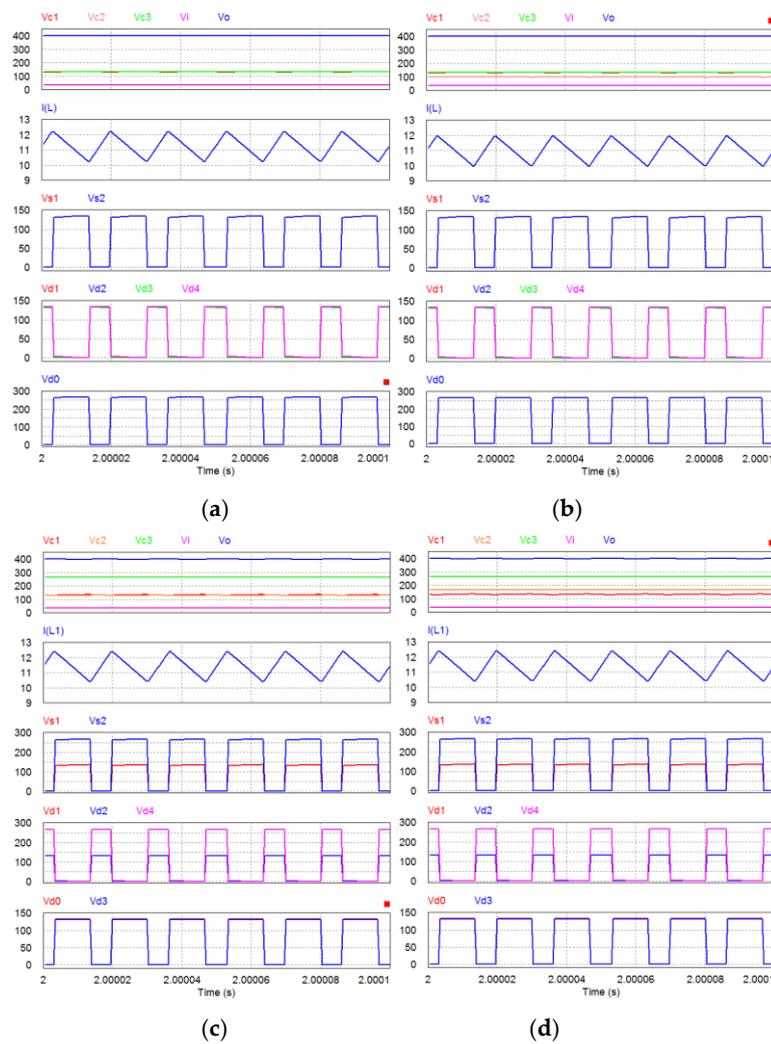
## 6. Simulation and Experiment Discussion

### 6.1. Simulation Results

The proposed 3-SCNCs are verified by using PSIM 9.1 simulation when the input voltage and output voltage are set up 36 V and 400 V, respectively. The switching frequency is 60 kHz, and the load power is 400 W. The simulation parameters of the converters are selected as Table 3. In Figure 13, the simulation results of the proposed 3-SCNCs are shown. The voltage stress across capacitors, diodes and MOSFETs are fit well with the theoretical analysis in Table 2.

**Table 3.** Parameters of the proposed 3-SCNCs.

Parameter	Values	
Input DC source	36 V–72 V	
Output voltage	400 V	
Output power	400 W	
Inductor	0.5 mH	
Capacitors	$C_1, C_2, C_3$	7.5 $\mu$ F/350 V
	$C_0$	45 $\mu$ F/450 V
Switching frequency	60 kHz	



**Figure 13.** Simulation results of the proposed 3-SCNCs with  $V_i = 36$  V. (a–d) From top to bottom: capacitors  $C_1$ – $C_2$ – $C_3$  voltage, output voltage, input voltage, inductor current, voltage stress of switches  $S_1$ – $S_2$ , and voltage stress of diodes  $D_0$  to  $D_4$ .

### 6.2. Experimental Results

In order to verify the experimental performance of the 3-SCNCs, the laboratory prototype for proposed 3-SCNC type 1 was constructed. The main experimental parameters are selected in Table 3. Film capacitors were selected, two power switches of IRFP4668PbF MOSFETs for their low ON-resistance and four STPS60SM200C Schottky diodes were used, one more FF60UP30DN diode was used for output diode  $D_0$ . While the setting parameters are applied, the converter was fed by the CHROMA 62012P-100-50 DC power supply. To maintain the output voltage at 400 V, a simple PI output voltage loop is controlled by a DSP TMS320F28335, as shown in Figure 14. Figure 15 shows the voltage waveforms of two power switches  $S_1$ – $S_2$ , diodes  $D_0$ – $D_4$ , capacitors  $C_1$ – $C_3$ , and the current waveforms of the inductor at  $P_o = 330$  W,  $V_i = 72$  V and  $V_i = 36$  V. The measured values of capacitor voltage are 133.3 V each, the output voltage is 400 V. In Figure 15e,f, it is easy to see that the voltage stress of power switches  $S_1$ – $S_2$  and diodes  $D_1$ – $D_4$  are approximately the capacitor voltage. In order to verify the DCM theoretical study in Section 3.1, the experiment parameters of the proposed 3-SCNC type 1 are  $D = 0.3$ ,  $k = 0.02$ ,  $V_i = 36$  V,  $L = 0.4$  mH. The power load is decreased to 30 W in experiment. As shown in Figure 16, the capacitor  $C_1$ ,  $C_2$ , and  $C_3$  are 134 V and 133 V. Compared to the waveforms in Figure 15 for CCM, the proposed 3-SCNC type 1 in DCM has a higher boost factor.

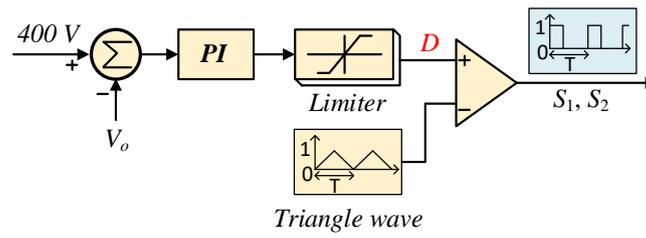


Figure 14. PI voltage controller for the proposed 3-SCNCs.

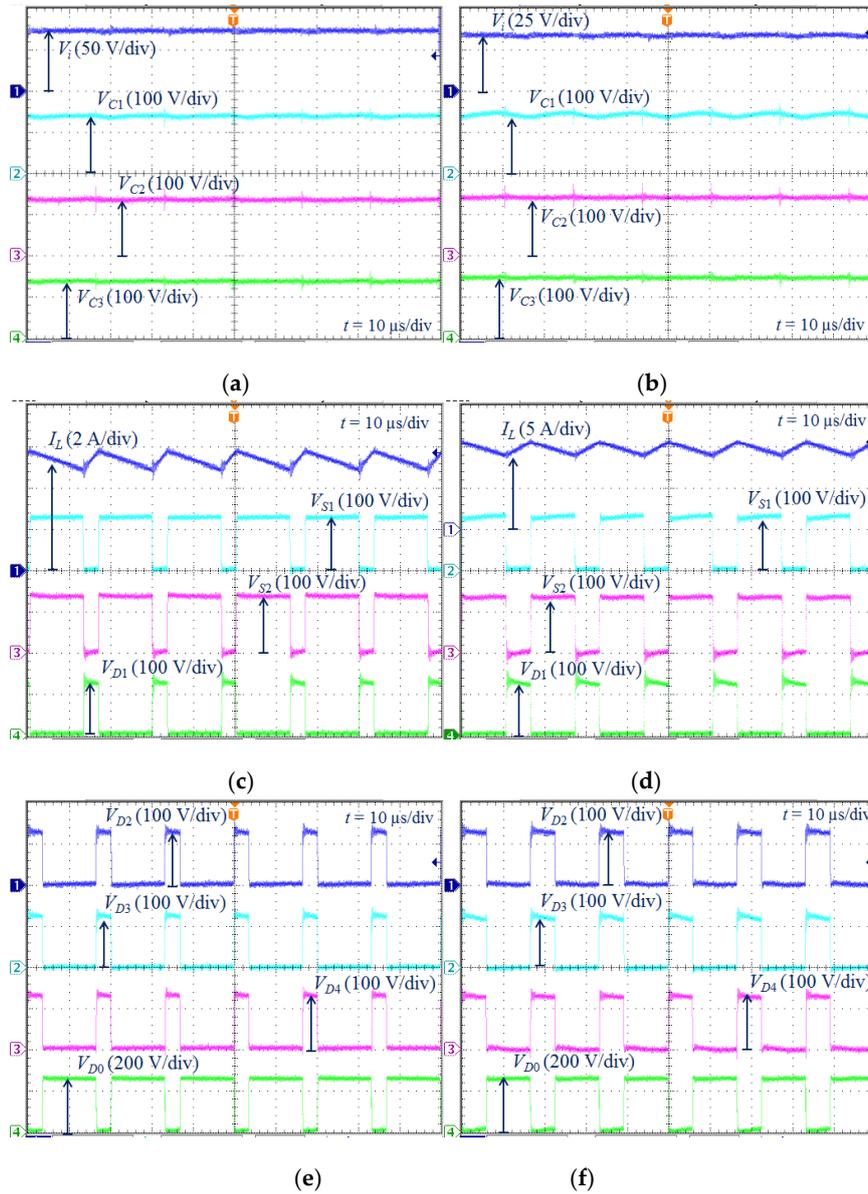
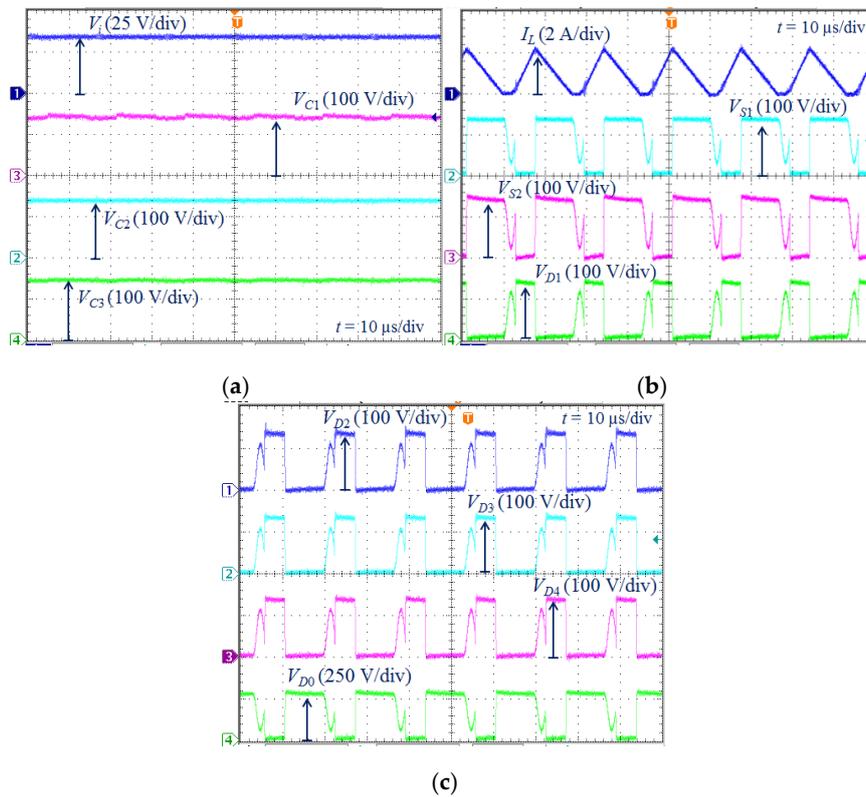
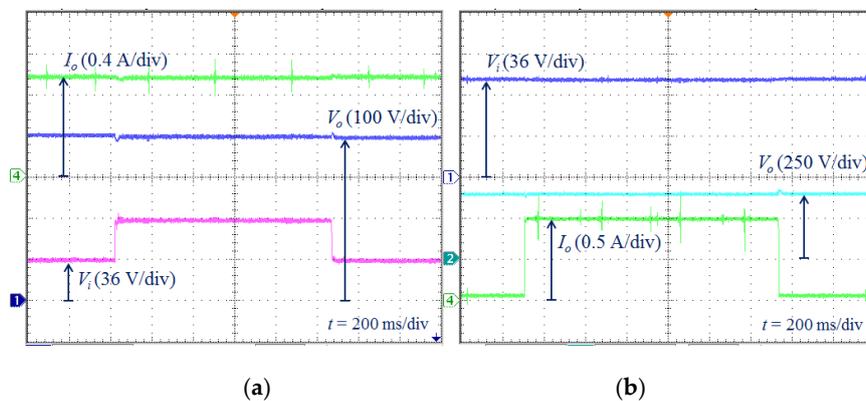


Figure 15. Experiment waveforms with  $V_i = 72\text{ V}$  (a,c,e) and  $V_i = 36\text{ V}$  (b,d,f). From top to bottom: (a,b) input voltage, capacitors  $C_1, C_2, C_3$  voltage; (c,d) inductor current, switch  $S_1$ - $S_2$  voltage, diode  $D_1$  voltage; (e,f) diode  $D_2$ - $D_3$ - $D_4$ - $D_0$  voltage.



**Figure 16.** Experiment waveforms in DCM. From top to bottom: (a) input voltage, capacitors  $C_1, C_2, C_3$  voltage; (b) inductor current, switch  $S_1$ - $S_2$  voltage, diode  $D_1$  voltage; (c) diode  $D_2$ - $D_3$ - $D_4$ - $D_0$  voltage.

Figure 17 validates the experimental waveforms of the proposed 3-SCNC type 1 while the controller is executed. Thereby, the output reference voltage is set as 400 V and the output power is 400 W, while the input DC source is adjusted from 36 V to 72 V. In next case, the input voltage is set 36 V when power load changes from the light load (5% of full load) to full load of 400 W. Figure 18 presents the experimental efficiency of the proposed 3-SCNCs regarding load under  $V_i = 36$  V and 72 V. The measurement both input and output power are performed by WT230 Power Meter from YOKOGAWA. It can be seen that the efficiency is reduced when the low input voltage is suggested, this is because the conduction loss on devices is high. It is obvious that the efficiency of the proposed 3-SCNC type 1 and 2 are higher than the proposed 3-SCNC type 3 and 4. Because the proposed 3-SCNC type 1 and 2 have lower voltage stress across capacitors, diodes and MOSFETs than that of proposed 3-SCNC type 3 and 4.



**Figure 17.** Transient experiment results. (a) Input voltage changed. (b) Load changed.

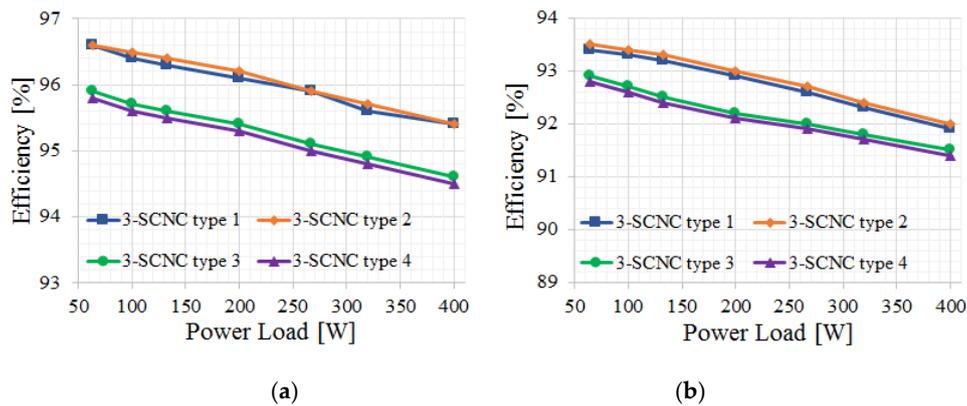


Figure 18. Efficiency of the proposed 3-SCNCs at different output powers. (a)  $V_i = 72$  V, (b)  $V_i = 36$  V.

## 7. Conclusions

According to the advantages of the switched-capacitor technique, a class of high step-up transformer-less DC-DC converters with three switched-capacitor networks has been proposed in this paper. The characteristics of the proposed 3-SCNCs are as follows: providing a high voltage ratio with small duty cycle, thereby achieving low conduction loss of the power switches; and having a low voltage stress on the capacitors and power devices. The operating principle in CCM/DCM boundary condition, analysis with parasitic components and parameters design are derived in detail. In addition, the comprehensive comparison between the proposed 3-SCNCs and other transformer-less high step-up DC-DC converter topologies has been done, which highlighted the merits and drawbacks of the proposed 3-SCNCs. Finally, the simulation and experimental results with closed-loop controller are shown to verify the theoretical analysis.

**Author Contributions:** T.-D.D. determined topology, data analysis, and original draft preparation. M.-K.N. contributed to review and editing. T.-T.T. contributed to validating in simulation and experimental work. Y.-C.L. provided resources and supervision. J.-H.C. provided resources and funding acquisition.

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