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Fully-Integrated Converter for Low-Cost and Low-Size Power Supply in Internet-of-Things Applications

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Abstract: The paper presents a fully-integrated and universal DC/DC converter to minimize cost and size of power supply systems in wireless nodes for Internet-of-Things (IoT) applications. The proposed converter avoids the use of inductors and is made by a cascade of switching capacitor stages, implementing both step-down and step-up converting ratios, which regulate input sources from 1 V to 60 V to a voltage of about 4 V. Multiple linear regulators are placed at the end of the cascade to provide multiple and stable output voltages for loads such as memories, sensors, processors, wireless transceivers. The multi-output power converter has been integrated in a Bipolar-CMOS-DMOS (BCD) 180 nm technology. As case study, the generation of 3 output voltages has been considered (3 V, 2.7 V, and 1.65 V with load current requirements of 0.3 A, 0.3 A, and 0.12 A, respectively). Thanks to the adoption of a high switching frequency, up to 5 MHz, the only needed passive components are flying capacitors, whose size is below 10 nF, and buffer capacitors, whose size is below 100 nF. These capacitors can be integrated on top of the chip die, creating a 3D structure. This way, the size of the power management unit for IoT and CPS nodes is limited at 18 mm². The proposed converter can also be used with changing input power sources, like power harvesting systems and/or very disturbed power supplies.

Keywords: DC/DC converter; power supply; Internet-of-Things (IoT); Cyber-Physical-Systems (CPS)

1. Introduction

This paper presents the design of a scalable DC/DC converter architecture to achieve a high-efficient management of the power supply, with low-cost and low-size hardware devices, in the nodes used in Internet-of-Things (IoT) and Cyber-Physical-Systems (CPS) applications.

In IoT and CPS applications, all units belonging to a system are connected together and exchange data and information in a large global network [1–17]. These “things” can be part of complex systems for healthcare [18–25], smart agriculture [26], science experiments [27], vehicles [28–32], satellites [33–35], domotics [36,37], robots/drones or industrial machines [38–40], telecom or surveillance apparatus [41–43], sport [44,45] or energy/smart-grid systems [46–50], and/or consumer electronics [51–57]. These units are usually wireless nodes, working at sub-GHz frequencies or in the range 2.4 GHz to 6 GHz [58–61], or at mm-waves [62–64]. Therefore, the power supply is provided by a battery and/or is harvested from the environment.

Low cost, small size, and high integration capabilities are the key issues for a rapid success of IoT and CPS technologies. Therefore, a high-efficient management of the power supply, with low-cost and low-size hardware devices, is a key issue for IoT and CPS nodes.

The input levels of the voltage supply for an IoT or a CPS node are from few Volts, e.g., in case of energy-harvesting or if a single battery cell is used (e.g., 3 V for a lithium cell), to tens of Volts for DC power bus on-board vehicles or drones or in telecom apparatus. For example, DC power buses for vehicles, robots, drones, and telecom/networking apparatus have nominal values of 12 V, 24 V,

36 V, or 48 V. Over-voltage levels can be up to 60 V [65–68]. DC/DC converters are needed to regulate the input supply level V_{in} to the required output level V_{out} . An IoT or CPS node includes low-power loads such as sensors, memories, A/D converters, microcontrollers, and wireless transceivers [69–71]. Thanks to technology scaling, all these blocks are now low-power consumption devices where the voltage supply is around 1 V in consumer-grade devices, and can be increased at 3 V or 5 V in devices used in harsh environments such as industrial automation, robotics, and vehicles.

Conventional voltage regulator hardware [72–74] uses inductor-based switching converters due to their superior efficiency vs. linear converters and their capability to work both in step-up and step-down modes. However, inductor-based switching converters are difficult to integrate since they entail a high cost in term of area and assembly effort. Inductors are difficult to integrate in silicon technology. Integrated inductors have been proposed in literature, but limited to high-frequency wireless applications, where inductors well below 1 nH are needed. Silicon-integrated inductors suffer of scarce quality factors Q [75,76].

Instead, linear DC/DC converters can work only as step-down converters, i.e., $V_{out} < V_{in}$, and the power efficiency depends on the ratio V_{out}/V_{in} [77–80]. In [70,78] linear regulators facing high voltage applications have been proposed. However, to regulate an input voltage of 48 V to an output value of 1 V, the power efficiency, using only linear regulators, would be dramatically low: only 2%. Hence, when the difference between V_{out} and V_{in} is high, the linear regulator is useful only for very low power applications.

To overcome the above issues this work presents a universal switched capacitor DC/DC converter, with multiple stages and multiple output voltages, which has the following distinguishing features vs. state-of-art:

- (i) It can sustain a wide input voltage range from 1 V to 60 V;
- (ii) It can work both in step-up or step-down modes as an inductor-based switching converters, but it is inductorless, and has low-ripple performance as linear regulators;
- (iii) It keeps power-efficiency levels much higher than linear regulators and comparable with inductor-based regulators;
- (iv) It uses only switches and capacitors, and hence can be easily integrated in a single chip reducing area and assembly effort/cost vs. inductor-based DC/DC converters.

Section 2 introduces the models used to analyze and design at architecture level the multi-stage multi-output switched capacitor DC/DC power converter. Section 3 presents the circuit-level design of the power converter. Section 4 discusses the implementation results achieved when integrating the converter designed in Section 3 in a 180 nm BCD technology. Section 4 shows a comparison of the proposed design vs. the state-of-the-art. Section 5 draws some conclusions and some hints for future work.

2. Models and Architecture of the Multi-Output Switched Capacitor Converter

2.1. Models of the Multi-Output Switched Capacitor Converter

The proposed architecture is based on switched capacitor (SC) converter [81–98] stages that can be easily integrated in silicon since they are characterized by the use of only capacitors and switches. The switches are realized in silicon through MOS transistors. If the required capacitor values are below 1 nF, then the capacitors may be realized as on-chip structures using MIM (Metal Insulation Metal) or using trench capacitors in the same 2D chip where there are also the active components. Instead, capacitors in the range from 1 nF to 100 nF can be realized as trench capacitors integrated in a passive interposer layer that can be assembled in recent 3D technologies on top of the classic 2D chip (see [99,100]). Since switched capacitor converters can be integrated in a single chip, this leads to benefit of a smaller area and assembly cost for the power sub-system of an IoT or CPS node. Based on a switching principle, the performance in terms of power efficiency of a SC-based converter is higher

than linear converters when the difference between V_{in} and V_{out} is large. On the other hand, SC converters can achieve the efficiency of inductor-based switching converters, but only for discrete voltage ratios. The voltage conversion factor (VCF) (see Equation (1)) of these converters is mainly determined by the repetitive changing of the circuit structure, thanks to switches that reconfigure the connections of capacitors. The SC converter can be modelled at low frequency, as an equivalent ideal transformer to represent the VCFs (the ratio 1:n in Figure 1A). The losses are taken into account with an output series resistor, R_s in Figure 1A, and a parallel resistor, R_p in Figure 1B.

$$V_{out} = VCF \cdot V_{in} \quad (1)$$

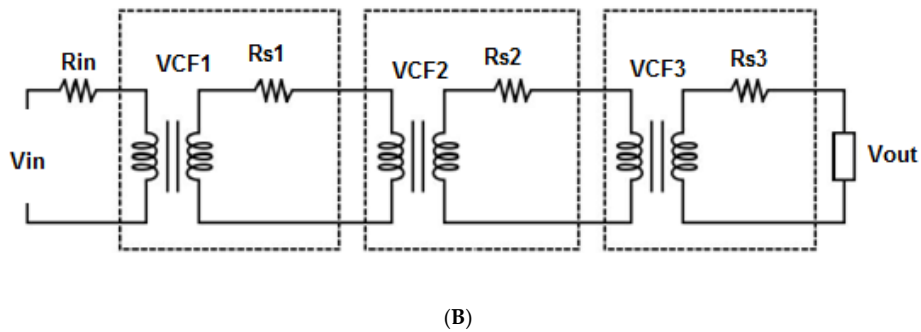
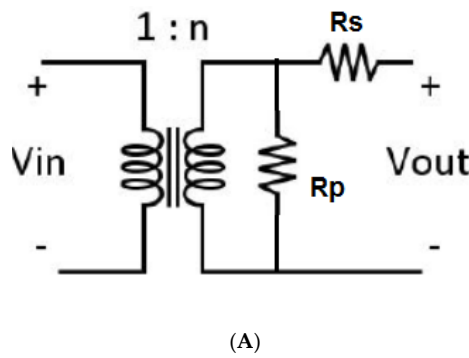


Figure 1. (A) Equivalent model of a generic switched capacitor converter; (B) Equivalent model of a three-stage cascade switched capacitor converter with negligible R_p effects.

The losses in a real transformer-based converter due to hysteresis and the losses in the magnetic are not negligible, and hence the contribution of R_p is important. Instead, in a switched capacitor converter, the losses due to the VCF are negligible [86]. In Figure 1, the contribution of R_p can be neglected vs. that of R_s for a switched capacitor converter.

In the case of a converter architecture made of a cascade of multiple stages, the model in Figure 1A can be repeated for each i -th stage being VCF_i , R_{s_i} , and R_{p_i} the conversion factor and the equivalent loss resistors of that specific stage. For example, Figure 1B shows the equivalent model of a three-stage cascade converter where the R_p contribution is neglected, and where the values of VCF and R_s can be different for each stage. In Figure 1B the contribution of the input source resistance R_{in} is also considered. In case the values of R_s and VCF for each stage of the cascade are known, the equivalent output resistor R_{s_eq} of the whole converter can be calculated using Equation (2).

$$R_{s_eq} = \left[(R_{IN} \cdot VCF_1^2 + R_{s1}) \cdot VCF_2^2 + R_{s2} \right] \cdot VCF_3^2 + R_{s3} \quad (2)$$

The output resistor R_s of the generic converter stage in Figure 1A can be calculated considering the charge flow analysis, which analyses the converter in two well-defined operating regimes: the Slow Switching Limit (SSL) and the Fast Switching Limit (FSL). In SSL, the converter operates at a frequency much lower than the time constant of the converter, thereby allowing the full charge and discharge of the capacitors. The losses are then dominated by the charge transfer between capacitors, see Equation (3), where f_{sw} is the switching frequency.

$$R_{SSL} \propto \frac{1}{f_{sw}} \sum_{i \in cap} \frac{1}{C_i} \quad (3)$$

In FSL, the converter operates with a switching frequency much higher than the time constant of the converter, limiting the charge and discharge transient times of the capacitors. Hence, in FSL the conduction losses due to the parasitic resistive elements (R_{ON}) dominate (see Equation (4)) where D is the duty cycle of the control signal and R_i is the on-resistance of the i -th switching element.

$$R_{FSL} \propto \frac{1}{D} \sum_{i \in sw} R_i \quad (4)$$

Both SSL and FSL approaches can be unified by considering them as complementary. The total output impedance, R_s in Figure 1, can be accurately approximated by R_{s_eq} in Equation (5). Due to the presence of R_{s_eq} when the converter is providing a current I_{load} to the load, then the output voltage can be calculated according to Equation (6).

$$R_{s_eq} \approx \sqrt{[(R_{SSL})^2 + (R_{FSL})^2]} \quad (5)$$

$$V_{out} = VCF \cdot V_{in} - R_{s_eq} \cdot I_{load} \quad (6)$$

Starting from these equations, a simulating model in Matlab/Simulink has been created, allowing for architecture definition and exploration. This is a behavioral and technology independent model. A more accurate simulating model in CADENCE design environment is then implemented, where ideal devices are substituted with their accurate models of the BCD 180 nm technology library. In the transistor-level model, all non-idealities and non-linearities of the devices are taken into account. Time-domain simulation, including steady-state and transient phases, can be carried out and all hardware parameters (area, power consumption, thermal behavior, performance in terms of ripple, line and load regulation, PSRR) of the converter can be evaluated considering PVT (process-voltage-temperature) technology corner cases.

2.2. Architecture of the Multi-Output Switched Capacitor Converter

The main feature of a DC/DC converter is regulating the output voltage V_{out} starting from the input voltage V_{in} , under the constraint of a load current requirement I_{load} . Taking into account the models discussed in Section 2.1, there are two ways to achieve this regulation in the proposed architecture according to Equation (6):

- (i) change the VCF by reconfiguring the circuit, thus modifying the term $VCF \cdot V_{in}$ in Equation (6);
- (ii) change the output resistor equivalent value in Equation (5), thus modifying the term $R_{s_eq} \cdot I_{load}$ in Equation (6).

The first technique keeps high the efficiency but requires a very large number of VCFs to obtain a good regulated output voltage. A large number of the VCFs can be obtained with a very complex network. The number of capacitors and switches necessary to obtain the desiderate VCFs can be calculated according to the Makowski's rules in Ref. [92].

To reduce the number of required VCF factors, and to reduce the complexity of the circuit but still keeping a good signal quality of the regulated output, it is possible to change the value of the

output resistance R_{s_eq} with a feedback circuit. Such a feedback circuit should modulate the frequency or the duty cycle of the switching signal, see Equations (3) and (4). This technique allows for an output signal quality close to that of linear converters but entails a power efficiency lower than the first discussed technique.

Moreover, each device (e.g., memory, sensor, microcontroller, RF transceiver) in a complex IoT system or CPS may require a different supply voltage level to optimize its performance. Therefore, the power management unit needs more than one output voltage. To this aim, we propose a modular and scalable architecture for the converter (see Figure 2) that can be expanded or reduced in relation to the application.

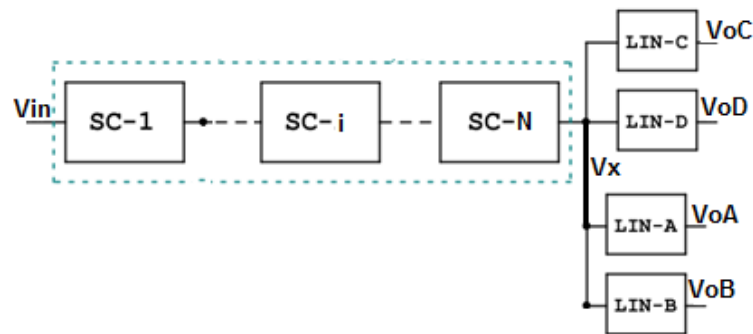


Figure 2. Generic converter architecture based on multi switched capacitor (SC) and linear (LIN) converters.

The basic idea is to have a cascade of switched capacitor converter stages, SC-1, SC-2 and SC-N in Figure 2, each with a configurable VCF, being VCF_i the VCF of the i -th switching converter stage SC- i with $i = 1, 2, \dots, N$. If a stage works in step-up mode then $VCF > 1$, otherwise in step-down mode $VCF < 1$. This way, the overall VCF for the whole cascade of switching converters, i.e., V_x/V_{in} in Figure 2, is the product of all the VCF_i values of the N converter stages.

Once V_x in Figure 2 is regulated from V_{in} , thanks to the switched capacitors stages, then, at the end of the cascade, several linear regulators are placed in parallel to obtain multiple-output voltages. In the example case of Figure 2, four linear regulators are placed in parallel to obtain four output regulated voltages. The linear converters can only work as step-down converters and their efficiency levels depend on the difference between their input, V_x in Figure 2, and their output voltages, VoA or VoB or VoC or VoD in the example of Figure 2.

If the input and output voltages of a linear converter are similar, they have an acceptable efficiency level. Therefore, the purpose of the cascade of SC converters in Figure 2 is to reduce or increase the input voltage V_{in} to put the linear converters at the last stage (LIN-A, LIN-B, LIN-C, and LIN-D in Figure 2) in their best working conditions. In addition, the use of linear converters to obtain different output voltages improves the quality of the output in terms of line regulation, load regulation, ripple, and power supply rejection ratio (PSRR).

The switching converters with inductors have a high efficiency but only one output voltage. A greater number of outputs requires more than one inductor, e.g., a converter for each output voltage level. Alternatively, some linear converters in cascade can be used, but this leads to the loss of benefits in terms of efficiency of the inductor-based converter.

3. Designed DC/DC Converter

3.1. DC/DC Architecture and Circuit-Level Design

The proposed power converter has been designed following the models and architecture discussed in Section 2 and configured to face a very wide input voltage range (from 1 V to 60 V), thus covering all possible requirements of an IoT or CPS node. Particularly, a four-stage architecture has been

implemented, see Figure 3, where the first three stages are SC stages, each with a VCF that can be selected as $\times 2$, $\times 1$, $\times 1/2$ and $\times 1/3$.

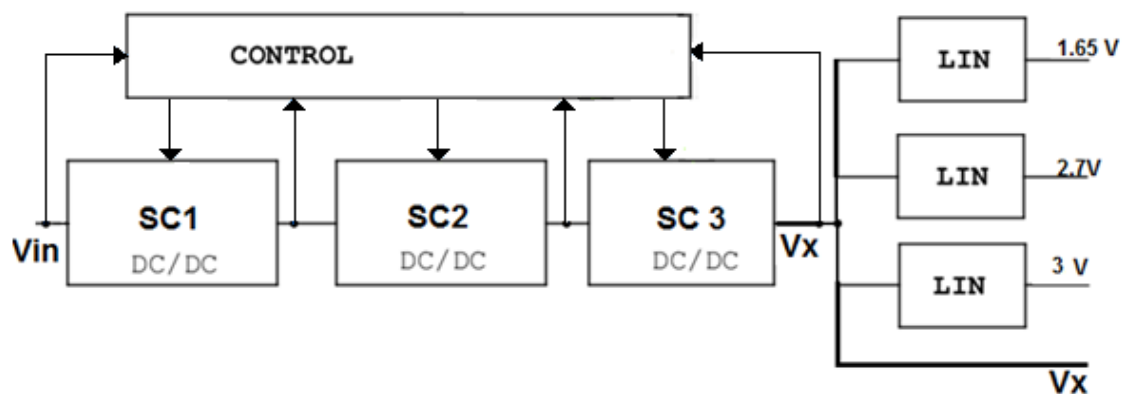


Figure 3. Implemented converter architecture.

As consequence, the possible different values of VCF that can be obtained from the global architecture are the following.

In step-up mode: $\times 8$, $\times 4$, $\times 2$, $\times 4/3$.

In step-down mode: $\times 2/3$, $\times 1/2$, $\times 1/3$, $\times 1/4$, $\times 2/9$, $\times 1/6$, $\times 1/8$, $\times 1/9$, $\times 1/12$, $\times 1/18$, $\times 1/27$.

At the end of the cascade of the three SC converter stages, the global architecture, displayed in Figure 3, has three linear regulators working in parallel to obtain three typical values for the power supply of IoT nodes. Also the V_x value is provided as a fourth output, which is also useful for diagnostic reasons.

For example, referring to an IoT system for ambient intelligence, it may include sensors to monitor temperature, humidity, light intensity, magnetic field intensity, and gas presence in an environment, using components off the shelf (COTS), where sensors are connected in an analog way to the internal A/D converter of a microcontroller or in digital way through an I2C or SPI digital bus [101]. For example, by using COTS device from Texas Instruments, a MSP432 host microcontroller (based on 32-bit Cortex-M4 microcontroller) and a CC3120 simple-link network processor can be used. The following voltage levels are required for the IoT node. Humidity sensor HDC1080 and gas sensor LMP91002 require a 2.7 V voltage supply; the microcontroller and the DRV52 magnetic sensor and the temperature sensor need a 1.65 V supply, whereas 3 V are used for the wireless transceiver, to reach a connection distance up to 100 m per device with IEEE 802.11 b/g/n protocol, and for the light intensity sensors.

The future evolution of COTS components in deep scaled technologies (also for IoT) is moving toward multi-core system-on-chip where different macrocells (e.g., processors, memories) are integrated on-chip interconnected through a network on chip [102–106] and/or to application specific processors for sensor conditioning [107–110]. In such cases, the voltage level requirements will remain more or less the same. If a different set of output voltages is required (e.g., 1.2 V, 1.8 V, and 2.5 V), these values can be obtained by a simple trimming of the feedback loop inside the linear regulators. The latter are characterized by a conventional pass-transistor architecture with an analog feedback loop realized through a differential operational amplifier.

The role of the controller in Figure 3 is measuring the input voltage and then properly configuring the VCF of the different SC stages to regulate a V_x higher than 3.2 V, from which the outputs of the linear regulators are obtained. The pass transistor, realized as an LDMOS in the adopted 0.18 μm BCD technology, in each linear regulator in Figure 3 has a minimum voltage drop of 200 mV.

The aims of the SC converter blocks are summarised hereafter.

The first conversion stage (called SC1) is a step-up/step-down converter and manages the wide input dynamic voltage (from 1 V to 60 V) regulating it in the range 2 V (e.g., step-up $\times 2$ of an input

voltage of 1 V) to 20 V (e.g., step-down $\times 1/3$ of an input voltage of 60V). This is the most challenging stage since it faces the highest voltage levels.

The second and the third conversion stages (called SC2 and SC3 in Figure 3) reduce the output resistance of the whole converter to ensure the correct operation of the final cascaded linear converters so that V_x is about 4 V when there is 1 V at the input of the converter. Instead, 60 V at V_{in} is regulated with a step-down factor $\times 1/18$ to a voltage of 3.33 V. To be noted that, by using for 60 V a step-down factor $\times 1/12$, then V_x is 5 V, which is another typical value for voltage supply of COTS components in IoT and CPS nodes.

To ensure the correct functionality of the 3 V linear converter, the VCFs thresholds are set to obtain an output voltage of the SC sub-system higher than 3.2 V for all the input dynamic. The system is optimized to supply a variable number of loads. It has been sized to face current requirements of 300 mA for the 3 V output and 2.7 V output and 120 mA for the 1.65 V.

According to the Ref. [92] to obtain the desiderate VCFs the SC architecture displayed in Figure 4 is used. The proposed circuit in Figure 4 uses two fly capacitors and a buffer capacitor.

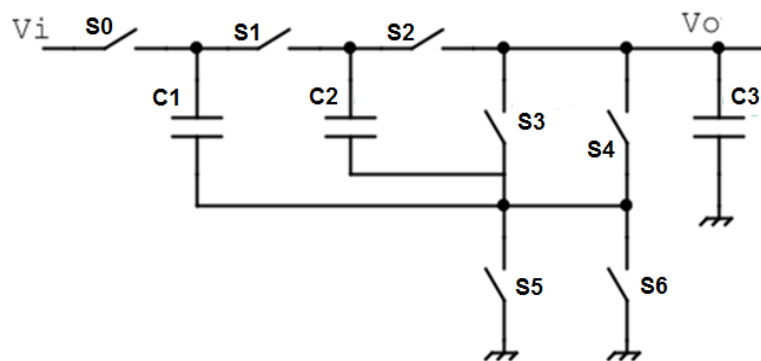


Figure 4. Circuit level design of the SC stages SC-1, SC-2, and SC-3 in Figure 3.

For this application, a 0.18 μm BCD technology is chosen to manage voltage levels up to 60 V. The specific technology has an influence on the ON-resistance of the switches and hence on the R_{FSL} value. Each switch in Figure 4 is sized according to the voltage to be faced and its role in the converter. Each switch can be made with single P-MOS/N-MOS or with a complex configuration up to four MOS devices.

Indeed, in the architecture of Figure 3, depending on the stage where the switch is used, the device that implements the switch may face voltage levels going from few Volts to several tens of Volts. Hence, three different circuit configurations, listed hereafter, can be used, which require from one to four transistors.

- (1) When facing low voltages the switch may be realized with a simple MOS transistor.
- (2) When facing higher voltages, an LDMOS (Laterally Diffused Metal Oxide Semiconductor), available in the BCD technology, is used as switch. In the selected configuration (see in Figure 5 the case of a P-MOS switch) two MOS devices are used: one is the switching element (device SW in Figure 5), and the other is another device (AUX in Figure 5) that connects the bulk of the pass transistor SW to his drain to bypass the drain-bulk parasitic diode. Indeed, in Figure 5 if the bulk is connected at the source of the device SW, then during some transients the bulk can have a lower potential than the drain. In this case, the current can flow inside the drain-bulk parasitic diode and is not possible to turn OFF the MOS just driving the gate voltage. Furthermore, the parasitic BJT in each LDMOS may inject current in the substrate. This current injection, if not avoided, could have destructive effects. To avoid these issues the circuit with two MOS in Figure 5 may be used. In this circuit the gate driver is connected between the gate and the source of the SW pass transistor to handle its V_{GS} . This way, when the gate driving signal is 0 V the gate is

connected at the source of the SW device and the whole circuit acts as a diode configuration where $V_{DG} = V_{DS}$. The proposed solution differs from other approaches in literature where the diode configuration is made connecting the gate with the drain of a MOS device ($V_{GS} = V_{DS}$). In the considered application the used transistor should sustain V_{DS} values of several tens of Volts but the gate-source junction of the LDMOS in the considered technology can sustain only few Volts. Instead, the diode configuration in Figure 5 is obtained connecting in the pass element SW the gate with the source. Being $V_{DG} = V_{DS}$ the gate-source junction is protected from high voltages.

- (3) The voltage drop on some switches in the circuit, when the converter performs both step-down and step-up conversions, changes from positive to negative and vice versa. In this case a back-to-back circuit switch is needed, which is obtained putting in cascade two structures as in Figure 5, so four transistors are needed. The first stage is in the direction Drain to Source and the following stage is in the opposite direction Source to Drain.

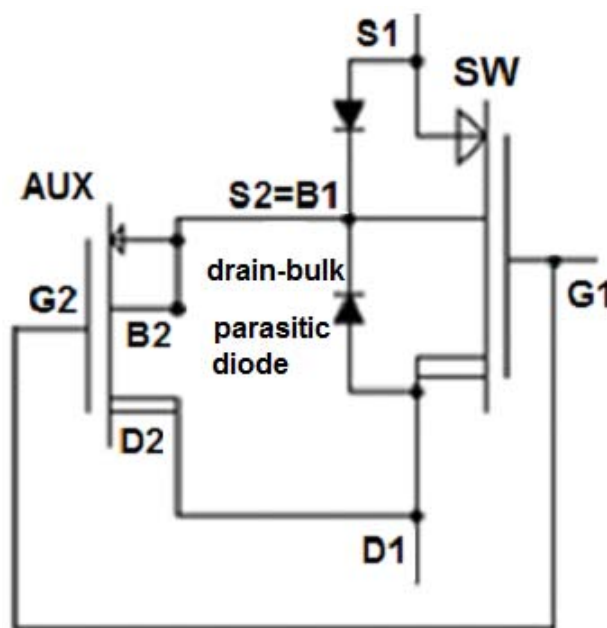


Figure 5. Transistor level design of a switch for high-voltage.

As detailed in Section 3.2, the selected switching frequency is 4.5 MHz and this allows to keep the used capacitors within 100 nF for buffer capacitors and below 10 nF for flying capacitors. This way the whole converter can be completely integrated on-chip since capacitors integrated in passive interposers are available with densities of tens of nF/mm².

The final LIN (Linear regulator) stages are placed to ensure the output nominal voltages and to meet stringent requirements in terms of PSRR, line regulation, load regulation and ripple. Figure 6 shows the circuit level schematic of the linear regulators. For each of the three linear regulators in Figure 3 the pass element is a P-MOS, which is integrated in the chip since this application considers loads of few Watts. The minimum voltage drop on the pass element is about 0.2 V and hence the minimum linear regulator input is about 1.85 V for the 1.65 V output, 2.9 V for the 2.7 V output, and 3.2 V for the 3 V output. For each of the three linear regulators the error amplifier in Figure 6 is made by a P-type folded cascode stage plus an AB-class output stage to drive the pass element. To avoid stability issues, for the error amplifier a compensation technique is used, which introduces a polo-zero singularity in the folded cascode stage. The internal reference V_{ref} in Figure 6 is obtained through an integrated bandgap circuit. Although the circuit architecture for the three regulators is the same, the different output voltages (1.65 V, 2.7 V and 3 V in the considered case study) starting from

the same V_x value, are obtained by configuring in different ways the resistors $R1$ and $R2$ in Figure 6. A 100 nF capacitor is used at the output of the converter to reduce the output voltage ripple.

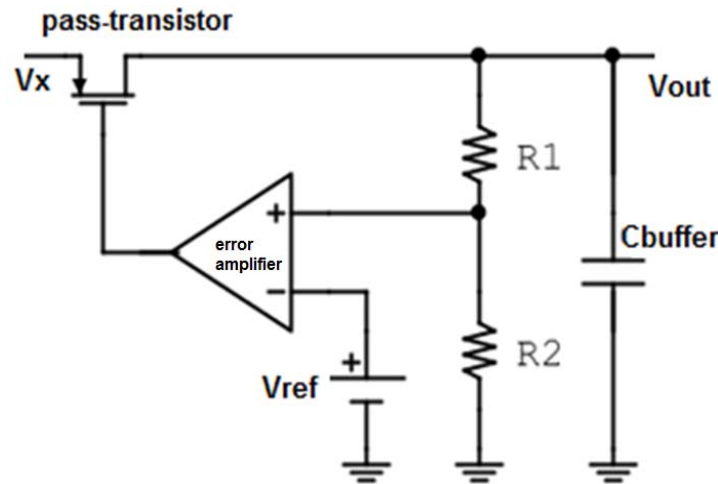


Figure 6. Circuit level design of the linear regulator.

3.2. Frequency Control

The controller block in Figure 3 exploits 3 main techniques: selection of the VCF for each SC stage by proper comparing the input voltage to threshold voltages; soft-start, similarly to what implemented in [111], and dithering of the switching frequency. The dithering of the switching frequency is needed to minimize the converter emissions of electromagnetic interference. If the switching frequency is constant at a value f_{SW} , then the power spectrum of the system is concentrated at this frequency reaching a very high level, not compliant with regulations for maximum emissions in the environment. The technique of the dithering consists in slightly changing the switching frequency. This allows spreading the power spectrum over a wider range of frequency, thus reducing emission peak value. Once the programmable switching frequency f_{SW} is set, the dithering function periodically changes the switching period according to a triangular law, as in Figure 7. The maximum frequency in Figure 7 depends on the maximum switching frequency of the transistors that have to sustain 60 V in the selected technology. In this work, we have adopted a 180 nm BCD technology for the converter implementation and in this technology the high voltage transistors can operate without performance degradation with a switching frequency up to 5 MHz. Once fixed the maximum switching frequency, in the proposed design the actual switching frequency is modified in a range from 4 MHz to 5 MHz around a nominal value of 4.5 MHz according to a triangular law. This way the maximum value of the power density of the interference emission spectrum is reduced by about 17 dB according to Equation (7), as already demonstrated in literature [112]. In Equation (7), f_{SW} is the nominal switching frequency of the controller (4.5 MHz in the proposed design), δ is the percentage dither about the fundamental switching frequency (between $\pm 11.1\%$ in this design), f_{DITHER} is the dither modulation rate (set at 100 kHz in the proposed design so that the dithering period is a multiple of the switching period being $f_{SW}/f_{DITHER} = 45$), and K is the system clock frequency divider used by the regulator ($K = 8$ since the 4.5 MHz clock rate is obtained from a 36 MHz on-chip ring oscillator). To be noted that in Figure 7 T_{DITHER} is 10 μ s. Using a technology node smaller than 180 nm the values of K , f_{SW} and δ can be increased; hence, also the spectral attenuation of EMI emissions can be increased. However, in scaled technologies the maximum sustained voltage of the transistors (70 V in this design) is lower. Therefore, a trade-off has to be found between spectral attenuation thanks to frequency dithering and maximum sustained voltage.

$$\text{Spectral attenuation (dB)} = 10 \times \log[(f_{SW} \times \delta) / (f_{DITHER}/K)] \quad (7)$$

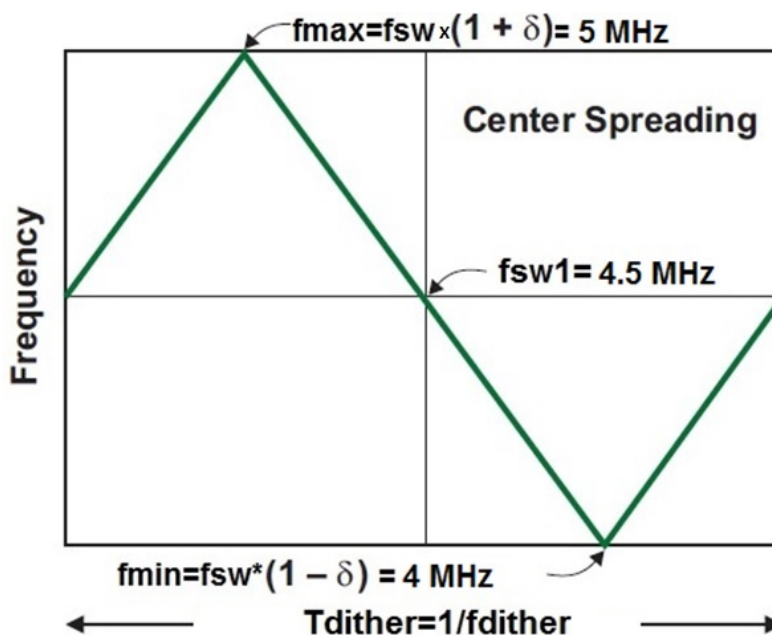


Figure 7. Triangular-like dithering of the switching frequency.

4. Implementation Results and Comparison to the State-of-the-Art

4.1. Implementation in BCD Technology

The architecture and circuits proposed in Section 3 have been implemented in a BCD 180 nm technology. The three SC converter stages and the linear regulators for 3 V, 2.7 V, and 1.65 V output have been integrated in a single chip of size $4.25 \times 4.25 \text{ mm}^2$, i.e., an area of about 20 mm^2 . The package is a ceramic dual in line package with 12 I/O pins (DIL 12). The integration of the passive components (capacitors in this case since the proposed architecture is inductorless) plays a key role in the possibility to realize a completely integrated converter. The architecture in Figure 3 needs about six flying capacitors (two for each of the three SC stages in Figure 3), each with a size of about 10 nF, and six buffer capacitors (one for each of the three SC stages, plus one for each of the linear regulators in Figure 3), each with a size of about 100 nF. The needed integration capability is 660 nF.

The use of 3D technology allows stacking the passive devices on top of the silicon die reducing the area of the printed circuit board (PCB), and the assembly cost of the whole system in case an inductor-based power converter is used. At the state-of-the-art the integration density of 3D capacitors in passive interposers to be assembled on top of the chip die is up to 250 nF/mm^3 in case the operating voltage is limited to 6 V. This is the case of the capacitors used in the point of load linear regulators. Instead, to sustain voltages up to 60 V (e.g., in the SC1 stage in Figure 3) the width of the capacitor should be increased and the integration density decreases at about 32 nF/mm^3 . Given the requirement of about 660 nF and considering the worst case of a density of 32 nF/mm^3 and a maximum area of 20 mm^2 for the interposer to be stacked on top of the chip, then the height of the passive interposer should be about 1 mm. These values are feasible in current 3D stacking technology. The use of 3D capacitors with direct contact between the chip and the capacitor layer (like flip chip techniques) reduces the use of bonding wire. This reduces the parasitic resistance problems and the antenna effects that generate radiated EMI problems.

The implemented converter has been tested through the experimental laboratory set-up in Figure 8 where a configurable power supply is used to generate an input DC voltage ranging from 1 V to 60 V. This variation is needed to measure the line regulation range. In case a PSRR performance measurement has to be done an AC source is placed in series to add a sinewave disturb. The amplitude of the sinewave disturb is $V_p = 0.2 \text{ V}$ if the DC input is in the range 1 V to 5V, otherwise V_p is 1 V.

If the test does not include the PSRR evaluation, the AC source is bypassed. The three voltage outputs plus the V_x output (see Figure 3) are measured through a multimeter. At the output of the three linear regulators, three configurable loads are applied so that we can measure also the load regulation performance, i.e., we can make several tests with different load currents.

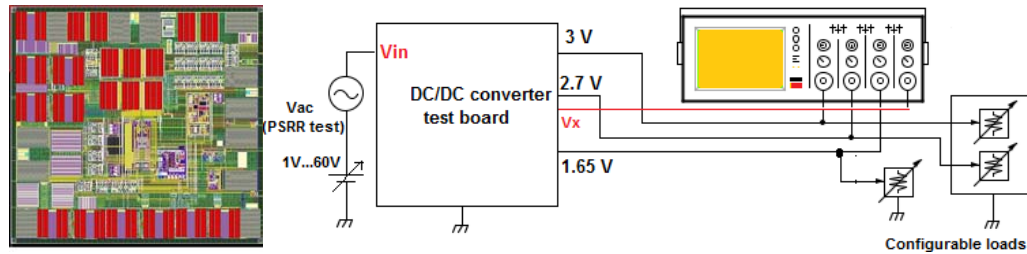


Figure 8. Schematic of the experimental test set-up and chip prototype.

Figure 9 shows the achieved power efficiency as a function of the input regulation voltage ranging from 1 V to 60 V when the output is regulated at 3 V. For comparison also the performance achieved by an ideal linear regulator and by a commercially-available converter, the Analog Devices chip LT3245 in [96], are shown. It is worth noting that the proposed converter is the only one able to regulate a 3 V output starting from a voltage in the range 1 V to 60 V, and hence acting both as step-up or step-down converter. Instead, the linear regulator can work only as step-down. The LT3245 DC/DC converter has a working range of about 33 V, from 3 V to 38 V. Hence, it cannot be used with energy harvesting systems where the harvested power source is usually working with voltage levels below 3 V. From an efficiency point of view, the proposed converter outperforms the LT3245 for all input voltages above 15 V. The proposed design has an efficiency ranging from about 50% to 70% when the input voltage varies from 1 V to 60 V. The linear regulator is efficient only for very low inputs. Its efficiency is reduced down to 5% when the input voltage increases to 60 V. Repeating the power efficiency analysis also for the other outputs (2.7 V and 1.65 V in the considered design), similar results are obtained.

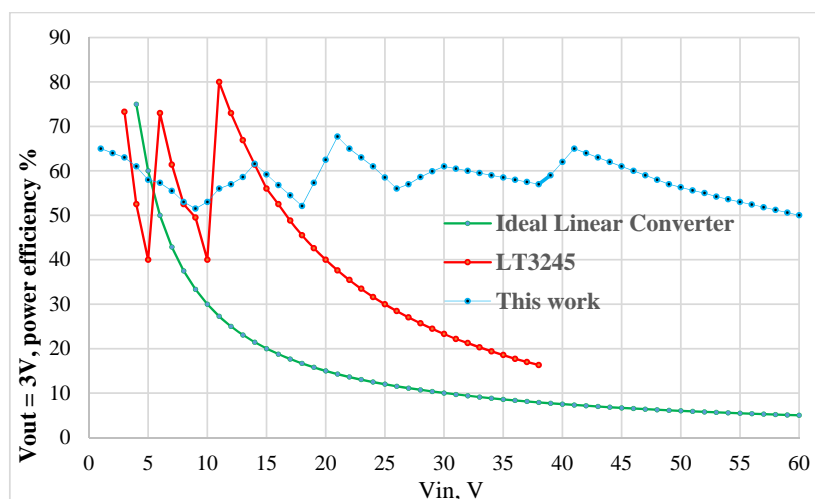


Figure 9. Power efficiency of the 3V output stage when V_{in} varies from 1 V to 60 V.

Figure 10 shows the load regulation capability of the proposed converter. The output voltage for each of the three outputs is evaluated for different values of the load current in the range from 0 to 300 mA for the 3 V and the 2.7 V outputs and in the range 0 to 120 mA for the 1.65 V output. In Figure 10, the input voltage is kept at a constant value of 12 V. Instead, Figure 11 shows the line regulation capability of the proposed converter, i.e., how the output voltage varies (for three outputs)

when the input voltage changes from 1 V to 60 V. The output current is considered for two different load values: 10 mA and 300 mA for the 3 V and 2.7 V outputs, and 10 mA and 120 mA for the 1.65 V output.

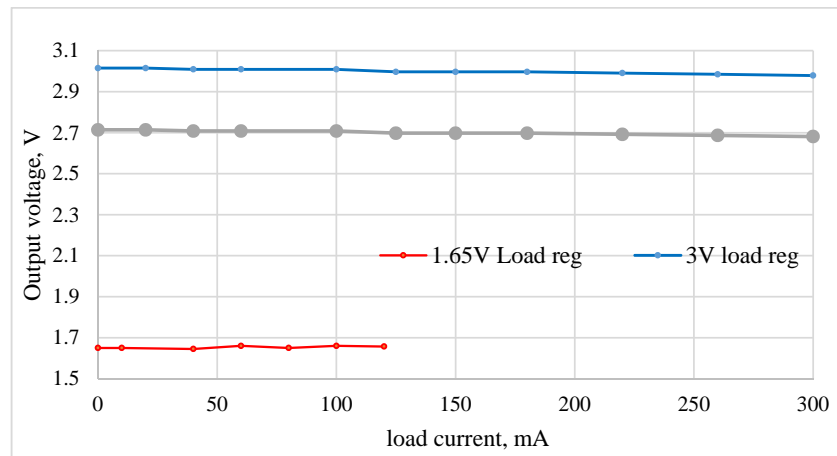


Figure 10. Measured load regulation for the 3 V, 2.7 V, and 1.65 V outputs, when the load current varies from 0 to 300 mA for the 3 V and 2.7 V outputs and from 0 to 120 mA for the 1.65 V output ($V_{in} = 12$ V).

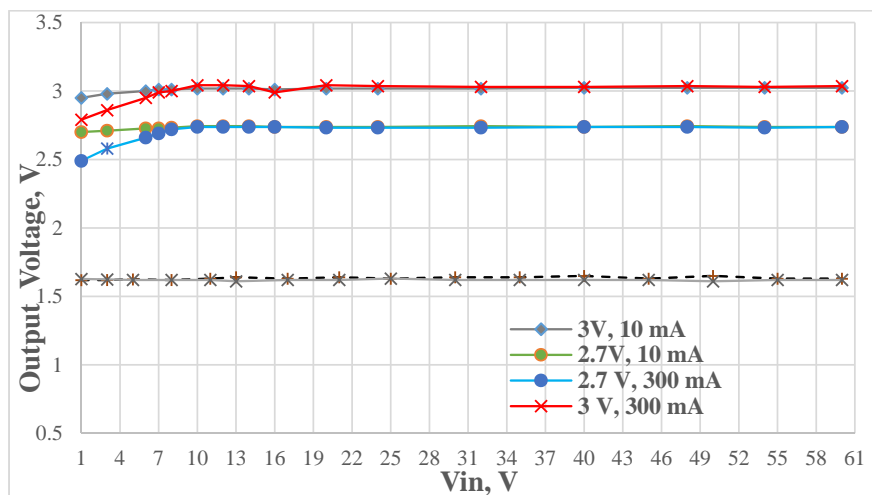


Figure 11. Measured line regulation for 3 V, 2.7 V, and 1.65 V outputs.

4.2. State-of-Art Comparison

In this section, the proposed DC/DC converter is compared to several other state-of-the-art converters [88,91,94,96] (see Table 1). The proposed design has several specific characteristics listed hereafter.

Table 1. Comparison to other state-of-the-art converters.

	Type	Input Range	PSRR, [dB]	Passive Devices	Temp., [°C]
OUR	Mixed SC+linear	1 V to 60 V	−60	On-chip capacitors Total 0.66 μ F (f_{SW} 4 to 5 MHz)	−40, 150
[88]	Mixed SC+linear	6 V to 60 V	−60	Off-chip capacitors Total 52 μ F (f_{SW} 100 kHz)	−40, 150
[94]	Inductive	36 V to 60 V	Off-chip	Off-chip passives, >12 μ H inductors	−40, 100
[96]	SC	2.7 V to 38 V	LDO needed	and >5 mF capacitors Off-chip capacitors, total size 12 μ F	−40, 150

- (1) The converter in this work is one of the few that avoid the use of cumbersome inductors, but at the same time is facing voltages up to 60 V. Instead, inductors are up tens of μH in state-of-the-art converters with the same input voltage range [94].
- (2) With respect to other SC converters, the proposed design sustains a wider input range, from 1 V to 60 V. Instead, the LTC3245 DC/DC [96] converter addresses similar voltage and current levels of the load but is limited to min 2.7 V and to max 38 V. Other works are limited at a maximum input voltage of 42 V. Instead, the inductor-based PT4667 [94] switching converter needs at minimum a 36 V input. An inductorless regulator has been recently proposed in [88,90] but in this case the input voltage is at minimum 6 V and hence this converter is not suited for energy harvesting applications where the harvested power is available at very low voltages, ie. 1 V.
- (3) With respect to the SC converter LTC3245 in [96], the proposed design achieves better efficiency for inputs above 15 V. Moreover, the LTC3245 SC converter can provide only outputs equal or above 2.5 V.
- (4) The voltage change of this work, around the regulated output is ± 30 mV, while for the SC converter LTC3245 converter is ± 60 mV. The proposed design achieves a PSRR of -60 dB, thanks to on-chip linear converters at the last stage of the cascade. Other state-of-the-art switching converters such as [94,96] do not declare their PSRR and need an off-chip LDO regulator to reach values comparable to our design.
- (5) With respect to state-of-the-art inductor-based converters, regulating up to 60 V, e.g., PT4467 in [94], with an efficiency of 70% for load currents below 1 A, our design allows for a PCB saving of a factor $\times 5$. Indeed the PCB of our converter can be realized with about 2 cm^2 while the PT4467 requires at least 13 cm^2 .
- (6) Our design has been characterized to sustain a thermal range up to $150\text{ }^\circ\text{C}$, while the PT4467 is limited at $100\text{ }^\circ\text{C}$. Hence, the proposed converter is suited for both consumer or telecom applications and industrial and vehicles applications.
- (7) Beside inductors, the PT4667 converter in [94] requires also an off-chip 5 mF capacitor, while this work requires less than $1\text{ }\mu\text{F}$ capacitors. By avoiding the use of inductors/transformers, the proposed design also enables system-on-package implementations with an area occupation below 1 cm^2 , one order of magnitude lower than [94]. Indeed, in the proposed design trench capacitors are integrated in passive interposers, assembled in 3D fashion with the DC/DC converter chip.
- (8) The increase of the switching frequency, between 4 MHz and 5 MHz, see Figure 7, vs. the 90 kHz adopted in [88] reduces the ripple values on the signals inside the system and reduces also the conductive EMI due to request of input charge. An increase of the switching frequency leads to an increasing of the power to switch the MOS devices. However, the used devices have a low gate capacitance and so the efficiency losses due to this effect are negligible (about $50\text{ }\mu\text{W}$ vs. output power of about 1.8 W, of which 0.9 W for 300 mA at the 3 V output, 0.8 W for 300 mA at the 2.7 V output, 0.2 W for 120 mA at the 1.65 V output).

5. Conclusions

A universal and fully-integrated DC/DC converter is proposed in the paper. It aims at minimizing cost and size of power supply systems in wireless nodes for IoT and CPS applications. The proposed converter is made by a cascade of three switching capacitor converters, implementing both step-down and step-up converting ratios, thus regulating all input sources to a voltage of about 4 V. Then, multiple linear regulators are placed at the end of the cascade to provide multiple and stable output voltages to loads such as memories, sensors, processors, wireless transceivers in IoT and CPS nodes. The multi-output power supply regulator has been integrated in a single-chip in a BCD 180 nm technology. In this case study, the generation of three output voltages has been considered (3 V, 2.7 V, and 1.65 V, with load current requirements of 0.3 A, 0.3 A, and 0.12 A, respectively).

The proposed converter has the following distinguishing features vs. other state-of-art converters:

- (i) It can sustain a wide input voltage range from 1 V to 60 V. This way it is not optimized for a particular input voltage, but it can be used with changing input power sources, like power harvesting systems and/or very disturbed power supplies;
- (ii) It keeps power-efficiency levels up to 70% in the whole input range from 1 V to 60 V being more efficient than linear regulators and with comparable efficiency to inductor-based regulators;
- (iii) The converter avoids the use of inductors and, thanks to the adoption of a high switching frequency up to 5 MHz (much higher than the 100 kHz adopted by other works in state-of-art converters [88]), the only needed passive components are flying capacitors (whose size is below 10 nF) and buffer capacitors (whose size is below 100 nF). The total amount of passive devices to be integrated is less than 1 μ F while in other works [88], switching around 100 kHz: this value is 50 times higher. Hence, the proposed converter can be integrated in a single chip (of 18 mm² for the case study of three output voltages and 2 Watts of total load power), reducing area and assembly effort/cost vs. inductor-based DC/DC converters;
- (iv) It implements control techniques such as soft-start and dithering of the switching frequency to minimize the emission of electromagnetic interference and hence to ensure electromagnetic compatibility in IoT and CPS applications.

The proposed solution's main limitation is its power efficiency, below 70%, which prevent its use for power levels higher than a few Watts or for low-power applications where a very long battery duration is needed or the harvested energy is low. Therefore, on-going activity is focused on optimizing the power efficiency of the proposed solution. Moreover, new chips will be designed and verified through measurements considering configuration different from the case study (3 V, 2.7 V, and 1 V outputs) discussed in this work.

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