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Analysis and Design of a DSTATCOM Based on Sliding Mode Control Strategy for Improvement of Voltage Sag in Distribution Systems

Ghazanfar Shahgholian * and Zahra Azimi

Najafabad Branch, Islamic Azad University, Najafabad, 8514143131 Isfahan, Iran; azimi_zahra_deh@yahoo.com * Correspondence: shahgholian@iaun.ac.ir; Tel.: +98-31-42292220

Academic Editor: Mostafa Bassiouni

Received: 20 June 2016; Accepted: 13 July 2016; Published: 20 July 2016

Abstract: Voltage sag is considered to be the most serious problem of power quality. It is caused by faults in the power system or by the starting of large induction motors. Voltage sag causes about 80% of the power quality problems in power systems. One of the main reasons for voltage sag is short circuit fault, which can be compensated for by a distribution static compensator (DSTATCOM) as an efficient and economical flexible AC transmission system (FACTS) device. In this paper, compensation of this voltage sag using DSTATCOM is reviewed, in which a sliding mode control (SMC) technique is employed. The results of this control system are compared with a P+Resonant control system. It will be shown that this control system is able to compensate the voltage sag over a broader range compared to other common control systems. Simulation results are obtained using PSCAD/EMTDC software and compared to that of a similar method.

Keywords: sliding mode control; power quality; FACTS devices; voltage sag; DSTATCOM

1. Introduction

In recent years, by granting the power industries to the private sector, and high demand for this kind of energy, the power companies—in order to prove their competence—are trying to provide high quality power to consumers [1,2]. Generally, any problem or defect in voltage, current, or frequency that leads to errors or malfunctions in electrical equipment is considered as a power quality problem. In electrical disturbance classification, voltage sag is the most conventional power quality problem [3,4]. According to IEEE 1159–1995 standard, voltage sag or temporary loss of voltage is defined as a reduction of root mean square (RMS) voltage to a value between 0.1 and 0.9 per unit at the power frequency for the duration of a half-cycle to 1 minute, where the interruption is a short time deviation and the total voltage loss (<0.1 per unit) in one or some conductors of phase for the duration of a half-cycle to 3 s [5,6]. The main causes of voltage sag include short circuit fault, starting large induction motors, sudden load variations, and energization of the transformer [7,8]. Voltage sag is a temporary event and its causes are also considered as a temporary low or medium frequency phenomenon [9,10]. Nowadays, with high demands and increases in sensitive equipment, voltage sag is not tolerated in power systems, and various methods have been applied to decrease it [11,12]. The conventional methods for decreasing voltage sag include using capacitor banks, installing new parallel feeders, and uninterruptible power supplies (UPS). Applying such methods cannot completely solve the problems of power quality. The reasons are uncontrollable reactive power compensation and the high cost of installing new feeders and using UPS [13,14]. Therefore, the conventional methods are not generally recommended. In recent years, by the rapid development of semi-conductor industries and control systems, compensation using high speed controllable electronics devices has become more popular. These devices are called flexible AC transmission systems (FACTS) [15,16]. The distribution static compensator (DSTATCOM) is an important member of this family that is used to improve power quality [17]. This three-phase compensator is installed near and in parallel with sensitive loads of distribution systems, and is generally used to compensate the voltage sag. It can also be used to limit the active and reactive power oscillations or harmonics currents drawn by the load [18,19]. The main block of DSTATCOM is the voltage source inverter (VSI), in which inverters convert the input DC voltage into three-phase output voltage at the basic frequency. Different strategies have been suggested regarding the control of the DSATCOM voltage source inverter. These conventional controllers include direct quadrature (d-q), state feedback, vector, proportional-integral (PI) and P+Resonant controls, are designed for a highly-accurate linearized mathematical model around a certain operating point, and give a superior performance at that particular point [20,21]. However, due to variations in the system parameters and the presence of nonlinear loads, these methods are unable to provide an appropriate operation [22,23]. The closed-loop sliding mode control (SMC) system for DSTATCOM is neither sensitive to variations in the system parameters, nor does it need an accurate mathematical model [24,25]. According to the alternative structures of the power inverters, this controller has various advantages, such as system stability against large supply and load variations, robustness, proper dynamic response, and simple practical performance [26,27]. In this paper, the voltage sag due to short circuit faults is reviewed and its compensation using DSTATCOM and SMC technique is proposed. To prove the theory and reveal the efficiency of the suggested control system, voltage sag compensation due to short circuit faults on the IEEE Standard 13-bus system is simulated by PSCAD/ EMTDC software. Then, the results of this control system are compared with a P+Resonant control system (P+Resonant control system is an improved PI controller).

2. Voltage Sag

Voltage-quality problems are as follows: voltage sag, voltage swell, and harmonics. The short circuit faults causing voltage sag are classified into symmetrical and unsymmetrical groups. Single-phase short circuit to ground is an unsymmetrical fault that happens more than the symmetrical faults; it is noted that symmetrical faults (three-phase to ground fault has the most effect on the voltage sag) hardly ever occur [28,29]. To determine the voltage sag domain in radial distribution networks, a voltage division model (depicted in Figure 1) is used where Z_s is the source impedance in the point of common coupling (PCC) and Z_f is the impedance between PCC and fault location. Voltage in PCC bus and accessories terminal is as follows:

$$V_{sag} = \frac{Z_f}{Z_f + Z_s} E \tag{1}$$



Figure 1. Voltage division model in measuring voltage sag. PCC: point of common coupling.

When the faults occur close to the customers (lower Z_f), the voltage sag is more serious than the case with the least fault level (large Z_s). Based on Thevenin theorem in a looped system, it is also possible to have voltage sag domain in bus *i* due to a fault in bus *r*, as follows:

$$V_{sag,i} = V_{o,i} - \frac{Z_{tr}}{Z_f + Z_{rr}} V_{o,i}$$
(2)

where $V_{sag,i}$ is the voltage sag due to the fault in bus *i*. $V_{o,i}$ and $V_{o,r}$ are the voltage before the fault. Z_{rr} and Z_{tr} are the elements in the bus impedance matrix Z_{bus} , and Z_f is the fault impedance.

3. DSTATCOM Structure

DSTATCOM is installed close to and in parallel to the sensitive loads. That is based on power electronics equipment. The main parts of this compensator are shown in Figure 2. The components of DSTATCOM include capacitor, DC supply, three-phase inverter, filter capacitor, coupling transformer, and control strategy. The main block of DSTATCOM is the VSI, which inverts the input DC voltage into three-phase output voltage at basic frequency. Therefore, this compensator is used to dynamically set the domain and the angle between the inverter voltage and distribution system voltage. Thus, the DSTATCOM exchanges the active and reactive power with the distribution network through leaking reactance of the coupling transformer [30,31]. The injected current of the compensator is as follows:

$$i_m = \frac{V - V_i}{X_f} \tag{3}$$



Figure 2. Basic structure of a distribution static compensator (DSTATCOM). VSI: voltage source inverter.

In which the transformer resistance is neglected. In (3), the inverter output phase voltage based on thyristor (V_i), is controlled by the V distribution system voltage. X_f is the leaking reactance of the coupling transformer.

4. Sliding Mode Control

Sliding mode controllers have some advantages, such as parameter insensitivity and realization simplicity [32]. SMC is a variable structure control system that increases the robustness of the system and preserves stability under variations and external disturbances [33]. The general structure of VSI

is first reviewed. The voltage control loop of VSI will use a SMC in order to achieve the intended purpose. The design of the SMC of the VSI is discussed in this section. The SMC is designed based on the following three-step algorithm [34,35]:

Step 1—writing the state-space equations of the system.

Step 2—selecting the linear sliding surface for the system and evaluating the existence of sliding mode.

Step 3—determining control law.

4.1. System Equations

Consider the schematic block diagram of DSTATCOM in Figure 2. In order to design a control law independent of the parameters network and load, the following state vector is defined:

$$V^{\mathrm{T}} = \left[\begin{array}{cc} v & \dot{v} \end{array} \right] \tag{4}$$

where state variable v is the voltage in PCC point and v is its derivative. Considering state vector V as the output, the state spatial equation of the DSTATCOM is defined as follows:

$$\frac{d}{dt}V = AV + Bu + Cd$$

$$y = V$$
(5)

where:

$$A = \begin{bmatrix} 0 & 1\\ -\frac{1}{C_f L_f} & -\frac{R_f}{L_f} \end{bmatrix}$$
(6)

$$B = \begin{bmatrix} 0\\ \frac{V_{dc}}{C_f L_f} \end{bmatrix}$$
(7)

$$C = \begin{bmatrix} 0\\1 \end{bmatrix}$$
(8)

Variable *d* is the disturbance, depending on the parallel branch current as follows:

$$d = -\frac{1}{C_f} \left(\frac{di_{sh}}{dt}\right) - \left(\frac{R_f}{C_f L_f}\right) i_{sh}$$
(9)

SMC technique is used to solve the tracking problem; here the goal is that the output (y) follows the desired output $V_{ref}^T = \begin{bmatrix} v_{ref} & \dot{v}_{ref} \end{bmatrix}$. Its error state vector is expressed as follows:

$$V_e^T = \begin{bmatrix} v_{ref} - v & \dot{v}_{ref} - \dot{v} \end{bmatrix}$$
(10)

4.2. Sliding Surface Selection and Sliding Mode Existence Evaluation

In order to control the inverter output voltage, an appropriate sliding surface directly affected by the switching law must be found. A sliding surface is in fact a surface on which the state trajectories are located to attain a stable condition. So, the sliding surface equation should be dynamically stable. A common form for choosing this surface is the following state feedback law:

$$S(V_e, t) = K V_e = k_1 \frac{d}{dt} v_e + k_1 v_e$$
(11)

where *K* is a feedback gain matrix with two non-zero positive gains, k_1 and k_2 . The following equation shows that the sliding surface has dynamic stability.

$$S(V_e, t) = 0 \Rightarrow k_1 \dot{v}_e = -k_2 v_e \Rightarrow v_e = v_e(0)e^{-\frac{\kappa_2}{k_1}t}$$

$$t \to \infty \Rightarrow v_e \to 0 \Rightarrow v(t) \to v_{ref}(t)$$
(12)

In the suggested control system, all state trajectories should be converted to a sliding surface of $S(V_{e,t}) = 0$ over a limited time. Therefore, the switching law should ensure the stability condition for the system in SMC. This is the sliding mode existence condition, defined as follows:

$$S(V_e, t) S(V_e, t) < 0$$
 (13)

Equation (13) is the Lyapunove function that ensures the system stability condition, since:

- if S > 0 and $\dot{S} < 0$, then $S(V_{e},t)$ will decrease towards zero.
- if S < 0 and $\dot{S} > 0$, then $S(V_e, t)$ will increase towards zero.

The sliding mode existence condition implies that the distance between the system states and the sliding surface will lend to zero.

4.3. Determination of Control Law

After verifying the sliding mode existence condition, the switching law for the semiconductor switches can be devised as follows:

$$u(t) = \begin{cases} +1 & S(V_e, t) > 0\\ -1 & S(V_e, t) < 0 \end{cases}$$
(14)

If u(t) = +1, then S_{w1} and S_{w2} switches are on. If u(t) = -1, then S_{w3} and S_{W4} switches are on. In the ideal SMC, at infinite switching frequency, state trajectories are directed toward the sliding surface. However, a practical power inverter cannot have an infinite switching frequency. So, the states trajectories will not tend towards the origin, and move along the discontinuity surface with undesired oscillation known as Chattering. These oscillations may excite un-modeled dynamics of the system. Therefore, to implement practically and to eliminate chattering, the system characteristics are compared to a 2ε hysteresis band, where switching occurs at $|S(V_e,t)| < \varepsilon$. By applying the above hysteresis surface comparator, the switching law is modified as follows:

$$u(t) = \begin{cases} +1 & S(V_e, t) > \varepsilon \\ -1 & S(V_e, t) < \varepsilon \end{cases}$$
(15)

Figure 3 shows the complete strategy to implement the SMC of the DSTATCOM. The derivative part of the SMC in (11) is implemented using the filter capacitor current feedback loop as follows:

$$k_2(\dot{v}_{ref} - \dot{v}) = \frac{k_2}{C_f}(i_{Cfref} - i_{Cf})$$
(16)



Figure 3. DSTATCOM in sliding mode control (SMC).

5. Simulation Results

Voltage sag in the distribution system due to short circuit faults can be simulated using PSCAD/EMTDC software on the IEEE 13-bus standard test system. The impact of DSTATCOM compensator on the voltage sag compensation in the distribution system (Figure 4) is studied. In Figure 4, bus 650 is chosen as the input bus of the system, and is fed by the 20 kV voltages. A voltage regulator is used between buses 650 and 632. For regulator simulation, a transformer with a tap changer under load is employed, enabling stabilization of the voltage oscillations due to system disturbances. Two transformers with Y-Y connection and a turns ratio of 20/0.4 are used to model the low voltage network. These transformers are 500 kVA with R = 1.1% and X = 2%, located between buses 633 and 634 and between buses 671 and 680. In this system, seven different network configurations are used to model the distribution lines. The loads in this network are in the lumped and distributed forms, and a nonlinear load is connected to bus 680 consisting of a full bridge diode rectifier with equivalent DC side resistance of 5 Ω and smoothing DC capacitor of 500 μ F.



Figure 4. Schematic diagram of the proposed system.

5.1. Voltage Sag

Short circuit faults, as one of the most important reasons for voltage sag, can be simulated in the distribution networks. The types of different short circuit faults regarding the network structure are created in bus 671. Then, the voltage changes of buses 650, 634, 646, 675, and 611 due to these short circuits are obtained and summarized in Table 1. In this case, simulation time is 2 s and the fault occurs in $t_s = 1$ s, and is cleared after 0.1 s. In these simulations, the fault impedance is 1 Ω and the fault resistance between the lines is 0.1 Ω . Figures 5 and 6 shows the voltage variations in typical bus 611 due to symmetrical and unsymmetrical faults.



Figure 5. Voltage variations in bus 611 due to types of unsymmetrical short circuit faults in bus 671 and in uncompensated system: (**a**) single-phase to ground fault; (**b**) two-phase fault; (**c**) two-phase to ground fault.



Figure 6. Voltage variations in bus 611 due to types of symmetrical short circuit faults in bus 671 and in uncompensated system: (**a**) three-phase fault; (**b**) three-phase to ground fault.

Table 1. Domain of bus voltage due to different short circuits in the uncompensated system.

Bus Number Short Circuit Type	650	634	646	675	611
Single-phase to ground	19.950	0.379	19.164	17.233	17.190
Two-phase	19.941	0.373	18.243	10.579	10.470
Two-phase to ground	19.935	0.364	18.101	9.791	9.669
Three-phase	19.914	0.335	17.793	0.385	0.363
Three-phase to ground	19.892	0.319	17.685	0.141	0.135

5.2. Voltage Sag Compensation

Considering that the majority of nonlinear and sensitive loads were located nearly or on bus 671, DSTATCOM is used for voltage sag compensation on the same bus. Voltage variations due to different short circuit faults in bus 611 in the presence DSTATCOM with two different control systems—P+Resonant and SMC—in bus 671 are simulated in Figures 7 and 8. The two factors of P+Resonant controller $k_P = 50$ and $k_I = 100$ are assumed. In the SMC controller, two parameters are designed ($k_1 = 0.01$ s, $k_2 = 2$) and the hysteresis band is $\varepsilon = 0.5$ kv. It is easily possible to determine and recognize the voltage sag and interruption as shown in Tables 2 and 3, and Figures 5–8.



(c) Two-phase to ground fault

Figure 7. Voltage domain variations in bus 611 due to unsymmetrical short circuit faults in bus 671 and compensation with P+Resonant and SMC control systems.



 (\mathbf{b}) three-phase to ground fault

Figure 8. Voltage domain variations in bus 611 due to symmetrical short circuit faults in bus 671 and compensation with P+Resonant and SMC control systems.

Table 2. Domain of bus voltage due to differen	t short circuits in the DSTATCOM-compe	ensated system.
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Bus Number	Control System	650	634	646	675	611
Short Circuit Type		000	001	010	070	011
Single-phase to ground	SMC	19.983	0.390	19.531	18.413	18.407
	P+Resonant	19.963	0.382	19.241	17.601	17.589
Two-phase	SMC	19.976	0.384	18.984	17.718	17.705
	P+Resonant	19.957	0.377	18.442	16.891	16.998
Two-phase to ground	SMC	19.968	0.373	18.525	17.008	16.922
	P+Resonant	19.949	0.369	18.229	16.423	16.313
Three-phase	SMC	19.959	0.359	17.992	16.023	15.995
	Control system	650	634	646	675	611
Three-Phase to ground	SMC	19.959	0.359	17.992	16.023	15.995
	P+Resonant	19.940	0.347	17.851	14.889	14.908

Table 3. Domain of bus voltage due to different short circuits in the DSTATCOM-compensated system.

Bus Number Short Circuit Type	Control System	650	634	646	675	611
Three-Phase to ground	SMC	19.948	0.347	17.841	15.482	15.135
	P+Resonant	19.921	0.331	17.716	14.304	14.361

As shown in Table 2 and Figures 7 and 8, the P+Resonant (an improved type of PI controller) and SMC controllers are able to improve the voltage profile due to different short circuit faults in the typical network. As it is shown, in presence of the nonlinear load, the proposed control method can provide fewer disturbances (especially sensitive loads) and better compensate the voltage sag compared to P+Resonant controller.

To compare the effectiveness of the SMC, simulation results of these two control systems are presented in Table 3. Comparison of these figures and tables indicates that in using the SMC system, the voltage sags due to the different short circuit faults are reduced by 100% if the domain of the voltages are in the range of d < 0.1 and 0.3 < d < 0.6; in addition, the fault domain lies in the range of 0.6 < d < 0.9. Thus, this reduces the impacts of the voltage sag. So, compensation using DSTATCOM has led to a 59.88% improvement in voltage quality. The level of this reduction depends on the type of fault, which lies in the range of 5% to 18%. The compensator enables the provision of the required power for full compensation of the symmetrical and unsymmetrical faults through DSTATCOM, in such a way that if the fault is cleared in shorter than 75 ms, the compensator is able to fully compensate the voltage interruption through its energy stored system. Figure 9 shows the voltage variations of buses 611, 675, and 646, and also low voltage bus 634 due to three-phase to ground fault in bus 671. As depicted in Figure 9, the voltage domain increases more than 0.9 per unit of the basic voltage—this indicates the full compensation of the voltage interruption.



Figure 9. Comparison of voltage interruption due to three-phase to ground fault in bus 671 with DSTATCOM.

6. Conclusions

In this paper, short circuit faults were reviewed as an important cause of voltage sag, and DSTATCOM was used to compensate this phenomenon. Different strategies have been suggested

so far for the control of DSATCOM. The conventional controllers (such as P+Resonant) are optimized for a certain operating point and give a superior performance at that particular point. However, considering the presence of nonlinear loads in power systems and parameter variations of distribution networks, the P+Resonant controller fails to maintain good performance. Therefore, for system nonlinearity and uncertainties in the distribution network, control techniques for variable structure systems such as SMC can find a natural application in FACTS devices. In this paper, the design and operation of the robust control of SMC in DSTATCOM to compensate voltage sag phenomena were explained. Use of the SMC technique in this compensator enables compensation of voltage sag appropriately over a wider range with less disturbance than other conventional control systems. So, SMC represents a powerful tool to improve the performance of power inverters. In order to validate the proposed control, the types of different short circuit faults on the IEEE standard system related to distribution networks were simulated, and the results of the simulation indicated that the aforementioned compensator with the proposed controller is able to improve the voltage profile about 59.88%, with almost no disturbance.

Author Contributions: Ghazanfar Shahgholian and Zahra Azimi proposed the methodology. Zahra Azimi performed the simulations and wrote the manuscript. Both authors reviewed and polished the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

References

- 1. Shahgholian, G.; Movahedi, A. Power system stabiliser and flexible alternating current transmission systems controller coordinated design using adaptive velocity update relaxation particle swarm optimisation algorithm in multi-machine power system. *IET Gener. Transm. Distrib.* **2016**, *10*, 1860–1868. [CrossRef]
- 2. Shahgholian, G.; Haghjoo, E.; Seifi, A.; Hassanzadeh, I. The improvement DISTATCOM to enhance the quality of power using fuzzy-neural controller. *J. Intell. Proc. Electr. Technol.* **2011**, *2*, 3–16.
- 3. Goswami, A.K.; Gupta, C.P.; Singh, G.K. Minimization of voltage sag induced financial losses in distribution systems using FACTS devices. *Electr. Power Syst. Res.* **2011**, *81*, 767–774. [CrossRef]
- 4. Naidu, S.R.; de-Andrade, G.V.; da-Costa, E.G. Voltage sag performance of a distribution system and its improvement. *IEEE Trans. Ind. Appl.* **2012**, *48*, 218–224. [CrossRef]
- 5. Bingham, R.P. Measurement instruments for power quality monitoring. In Proceedings of the IEEE/PES, Chicago, IL, USA, 21–24 April 2008; pp. 1–3.
- 6. IEEE Std. 1159–1995. *IEEE Recommended Practice for Monitoring Electric Power Quality, Technical Report;* The Institute of Electrical and Electronics Engineers, Inc.: New York, NY, USA, 1995.
- Heine, P.; Khronen, M. Voltage sag distributions caused by power system faults. *IEEE Trans. Power Syst.* 2003, 18, 1367–1373. [CrossRef]
- 8. Nagpal, M.; Martinich, T.G.; Moshref, A.; Morison, K.; Kundur, P. Assessing and limiting impact of ttransformer inrush current on power quality. *IEEE Trans. Power Deliv.* **2006**, *21*, 890–896. [CrossRef]
- 9. Martinez, J.A.; Arnedo, J.M. Voltage sag studies in distribution networks—Part I: System Modeling. *IEEE Trans. Power Deliv.* **2006**, *21*, 338–345. [CrossRef]
- 10. Khanh, B.Q.; Dong-Jun, W.; Seung, M. Fault distribution modeling using stochastic bivariate models for prediction of voltage sag in distribution systems. *IEEE Trans. Power Deliv.* **2008**, *23*, 347–354. [CrossRef]
- 11. Milanovic, J.V.; Zhang, Y. Modeling of FACTS devices for voltage sag mitigation studies in large power systems. *IEEE Trans. Power Deliv.* **2010**, *25*, 3044–3052. [CrossRef]
- 12. Basu, M.; Das, S.P.; Dubey, G.K. Investigation on the performance of UPQC-Q for voltage sag mitigation and power quality improvement at a critical load point. *IET Gener. Transm. Distrib.* **2008**, *2*, 414–423. [CrossRef]
- 13. Faiz, J.; Shahgholian, G.; Ehsan, M. Stability analysis and simulation of the single-phase voltage source UPS inverter with two-stage cascade output filter. *Eur. Trans. Electr. Power* **2008**, *18*, 29–49. [CrossRef]
- 14. Azpeitia, M.A.P.; Fernandez, A.; Lamar, D.G.; Rodriguez, M.; Hernando, M.M. Simplified voltage-sag filler for line-interactive uninterruptible power supplies. *IEEE Trans. Ind. Electron.* **2008**, *55*, 3005–3011. [CrossRef]
- Shahgholian, G.; Movahedi, A.; Faiz, J. Coordinated design of TCSC and PSS controllers using VURPSO and genetic algorithms for multi-machine power system stability. *Int. J. Control Autom. Syst.* 2015, 13, 398–409. [CrossRef]

- 16. Valderrábano, A.; Ramirez, J.M. DStatCom regulation by a fuzzy segmented PI controller. *Electr. Power Syst. Res.* **2010**, *80*, 707–715. [CrossRef]
- 17. Masdi, H.; Mariun, N.; Mahmud, S.; Mohamed, A.; Yusuf, S. Design of a prototype DSTATCOM for voltage sag mitigation. In Proceedings of the IEEE/NPEC, Chicago, IL, USA, 28–29 June 2004; pp. 61–66.
- 18. Elnady, A.; Salama, M.M.A. Unified approach for mitigating voltage sag and voltage flicker using the DSTATCOM. *IEEE Trans. Power Deliv.* **2005**, *20*, 992–1000. [CrossRef]
- 19. Blazic, B.; Papic, I. Improved D-Statcom Control for Operation with Unbalanced Currents and Voltages. *IEEE Trans. Power Deliv.* **2006**, *21*, 225–233. [CrossRef]
- 20. Molina, M.G.; Mercado, P.E. Control design and simulation of DSTATCOM with energy storage for power quality improvements. In Proceedings of the IEEE/PEC, Caracas, Venezuela, 15–18 August 2006; pp. 1–7.
- 21. Ortega, R.; Trujillo, C.; Garcera, G.; Figueres, E.; Carranza, O. A PI-P+Resonant controller design for single phase inverter operating in isolated microgrids. In Proceedings of the IEEE/ISIE, Hangzhou, China, 28–31 May 2012; pp. 1560–1565.
- 22. Singh, B.; Arya, S.R. Adaptive theory-based improved linear sinusoidal tracer control algorithm for DSTATCOM. *IEEE Trans. Power Electron.* **2013**, *28*, 3768–3778. [CrossRef]
- 23. Singh, B.; Arya, S.R. Back-propagation control algorithm for power quality improvement using DSTATCOM. *IEEE Trans. Ind. Electron.* **2013**, *61*, 1204–1212. [CrossRef]
- 24. Nasiraghdam, H.; Jalilian, A. Balanced and unbalanced voltage sag mitigation using DSTATCOM with linear and nonlinear Loads. *Int. J. Electr. Comput. Syst. Eng.* **2007**, *1*, 86–91.
- 25. Kumar, C.; Mishra, M.K. Operation and control of an improved performance interactive DSTATCOM. *IEEE Trans. Ind. Electron.* **2015**, *62*, 6024–6034. [CrossRef]
- 26. Jain, A.; Behal, A.; Zhang, X.; Dawson, D.; Mohan, N. Nonlinear controllers for fast voltage regulation using statcoms. *IEEE Trans. Control Syst. Technol.* **2004**, *12*, 827–842. [CrossRef]
- 27. Shahgholian, G.; Karimi, H.; Mahmoodian, H. Design a power system stabilizer based on fuzzy sliding mode control theory. *Int. Rev. Mod. Sim.* **2012**, *5*, 2191–2196.
- 28. Bollen, M.H.J. Understanding Power Quality Problems: Voltage Sags and Interruptions; Wiley-IEEE Press: New York, NY, USA, 1999.
- 29. Nam, S.R.; Sohn, J.M.; Kang, S.H.; Park, J.K. Ground-fault location algorithm for ungrounded radial distribution systems. *J. Electr. Eng.* 2007, *89*, 503–508. [CrossRef]
- 30. Mokhtari, M.; Khazaie, J.; Nazarpour, D.; Farsadi, M. Interaction analysis of multifunction FACTS and D-FACTS controllers by MRGA. *Turk. J. Electr. Eng. Comput. Sci.* **2013**, *21*, 1685–1702. [CrossRef]
- 31. Karmiris, G.; Tsengenes, G.; Adamidis, G. A multifunction control scheme for current harmonic elimination and voltage sag mitigation using a three phase three level flying capacitor inverter. *Simul. Model. Pract. Theory* **2012**, *24*, 15–34. [CrossRef]
- 32. Shahgholian, G.; Rajabi, A.; Karimi, B. Analysis and design of PSS for multi-machine power system based on sliding mode control theory. *Int. Rev. Electr. Eng.* **2010**, *4*, 2241–2250.
- 33. Carpita, M.; Marchesoni, M. Experimental study of a power conditioning system using sliding mode control. *IEEE Trans. Power Electron.* **1996**, *11*, 731–741. [CrossRef]
- 34. Guptaand, R.; Ghosh, A. Frequency-domain characterization of sliding mode control of an inverter used in DSTATCOM application. *IEEE Trans. Circuits Syst.* **2006**, *53*, 662–676.
- 35. Bajpai, R.S.; Gupta, R. Sliding mode control of converter in distributed generation using DSTATCOM. In Proceedings of the IEEE/ICPCES, Allahabad, India, 28 December–1 January 2010; pp. 1–7.



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