

Article

## Heterojunction Diodes and Solar Cells Fabricated by Sputtering of GaAs on Single Crystalline Si

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**Abstract:** This work reports fabrication details of heterojunction diodes and solar cells obtained by sputter deposition of amorphous GaAs on p-doped single crystalline Si. The effects of two additional process steps were investigated: A hydrofluoric acid (HF) etching treatment of the Si substrate prior to the GaAs sputter deposition and a subsequent annealing treatment of the complete layered system. A transmission electron microscopy (TEM) exploration of the interface reveals the formation of a few nanometer thick SiO<sub>2</sub> interface layer and some crystallinity degree of the GaAs layer close to the interface. It was shown that an additional HF etching treatment of the Si substrate improves the short circuit current and degrades the open circuit voltage of the solar cells. Furthermore, an additional thermal annealing step was performed on some selected samples before and after the deposition of an indium tin oxide (ITO) film on top of the a-GaAs layer. It was found that the occurrence of surface related defects is reduced in case of a heat treatment performed after the deposition of the ITO layer, which also results in a reduction of the dark saturation current density and resistive losses.

**Keywords:** sputtering; gallium arsenide; heterostructures; silicon; solar cells

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## 1. Introduction

GaAs/Si heterojunctions could allow cost reduction and integration of fast electronic and optical devices on Si in different fields of electronics and have been of interest to the materials science community since the 1980s. The integration of GaAs on Si is still a challenge with respect to the fabrication of high quality devices, since a large lattice mismatch and different thermal expansion coefficients give rise to a network of misfit dislocations in the GaAs/Si interface [1]. In addition, interface charges and antiphase domain boundary defects can appear due to the polar-on-nonpolar nature of the GaAs/Si heterocontact [2].

Several groups have investigated various methods concerning the deposition of GaAs on Si. Heterojunction (HJ) diodes based on n-GaAs/p-Si were fabricated by molecular beam epitaxy (MBE) and exhibited surprisingly ideal device characteristics, despite the high density of misfit dislocations in the interface region [3,4].

Pulsed-laser deposition (PLD) techniques [5,6] as well as the deposition of p-GaAs on n-Si by laser pulses (355 nm, 532 nm, and 1064 nm) in the ns regime were used to manufacture rectifying and photosensitive diodes [7,8]. Furthermore, graded SiGe layers, prepared by chemical vapor deposition (CVD), molecular beam epitaxy (MBE) or low-energy plasma enhanced CVD (PECVD), were used as buffers between Si and GaAs in order to reduce the lattice mismatch [9–13].

A two-stage GaAs deposition process based on metalorganic chemical vapor epitaxy (MOVPE) followed by thermal annealing was used to fabricate GaAs solar cells on Si leading to an efficiency jump from 14.5% [14] to 20% [15]. A two-step MOVPE process combined with a hydrogen-assisted plasma treatment was applied to fabricate GaAs based schottky diodes on Si [16]. Also good results were reported for GaAs/Si solar cells fabricated by the same method [17,18] resulting in a significantly decrease of the saturation current density of the passivated cell due to reduction of surface recombination velocity and increase of minority carrier lifetime as well as remarkable improvements of the spectral response. Moreover, Si/GaAs heterojunction solar cells were prepared with a standard low cost radio frequency (RF) PECVD system for the deposition of Si on a GaAs substrate at temperatures below 200 °C [19].

On the other hand, Schottky barrier solar cells and diodes as well as GaAs/Si heterojunctions fabricated by magnetron sputter deposition techniques were reported in the past [20,21]. Especially magnetron sputtering allows the deposition of thin GaAs films with good quality at low temperatures [22], which also makes this technique interesting for large scale solar cell fabrication. In this work we describe fabrication details of diodes and solar cells prepared by sputter deposition of n-type GaAs on p-type single crystalline Si (c-Si) wafers focusing our research on two varying process steps: An HF etching treatment prior to the GaAs film deposition and a heat treatment afterwards. Therefore, we first investigate GaAs/Si diodes and their electronic properties (dark current behavior). Then, we are dealing with GaAs/Si based solar cells analyzing their photoelectrical behavior with respect to different preparation recipes (photo current behavior).

## 2. Device Preparation

Thin films of amorphous GaAs (a-GaAs) with a typical thickness of 200 nm were deposited on single crystalline p-type Si(100) wafers (doping concentration about  $5 \times 10^{16} \text{ cm}^{-3}$ ) at room temperature using an ESM100 Edwards & RFS5 Generator-300W sputtering system.

Prior to the deposition, the single crystalline p-Si wafers were cleaned in acetone and isopropanol followed by a water rinse afterwards. The native oxide was etched off in 2% diluted HF for 2 min.

The sputter conditions were: (1) chamber pressure  $5 \times 10^{-1} \text{ Pa}$ ; (2) Ar flux 10 sccm; (3) RF input power 50 W; (4) as sputter target, a four inch n-type GaAs(100) wafer (Si doping concentration about  $7 \times 10^{17} \text{ cm}^{-3}$ ) was used; (5) target-to-substrate distance 6.5 cm; and (6) all depositions were made under continuous rotation. After the deposition of GaAs, aluminum was sputtered at room temperature on the back side of the Si(100) wafers to get an ohmic back contact [23]. Then, the samples with a size of  $1 \text{ cm}^2$  were annealed in  $\text{N}_2$  atmosphere at  $425 \text{ }^\circ\text{C}$  for 20 min. This treatment reduces the As content on the a-GaAs film, thereby compensating preferential sputtering of As which otherwise would result in GaAs layers with a low Ga content [24]. Moreover, this process step favors recrystallization [25–27]. The device fabrication was finalized by sputtering a 200 nm thick Au layer as front contact on the GaAs film. The baseline process for the fabrication of solar cells was identical to the process described above with an additional 80 nm thick ITO film, which was deposited by sputtering on the top of the GaAs layer to provide an additional conducting and antireflection surface layer. An additional Au contact on the ITO was verified to provide a good ohmic contact by measurements carried out in our laboratory. Several samples with an area of  $1 \text{ cm}^2$  were fabricated in this second batch with a gold grid covering 3.5% of the solar cell area.

Our scientific work is focused on the investigation of the variation of two fundamental process steps: (1) some of the samples were prepared without HF etching of the Si substrate prior to the GaAs deposition; and (2) for some of the samples the thermal annealing step was performed before doing the ITO deposition instead of doing it afterwards.

For all devices, the J-V characteristics were measured under dark conditions and under standard irradiance conditions (STC), which are equivalent to AM1.5. The impact of the two process steps (1) and (2) is discussed in the following.

## 3. Results and Discussion

### 3.1. Diode Current-Voltage Characteristics

Typical measurements of the J-V characteristics of a diode based on an a-GaAs/c-Si heterocontact reveal an explicit rectification trend as shown in Figure 1 where forward and reverse bias regions can be clearly distinguished.

Further J-V curves of a-GaAs/c-Si heterojunction were also measured at different temperatures ranging from 286.8 K to 448 K using an HP4124B DC source/monitor system. The results are shown in a semilogarithmic plot in Figure 2 where the slope of the forward current remains constant for all temperatures in the low voltage regime. This behavior indicates that for low voltages, the forward current is dominated by a tunneling mechanism [21]. For a larger forward bias voltage, the dependence of the current can be written as follows [21]:

$$J = J_0 \exp(AV) \tag{1}$$

where A is a constant that is independent on the temperature. In Figure 3, the dark saturation current density  $J_0$  determined from the data shown in Figure 2 is plotted as a function of  $1000/T$ . The linear behavior in this semilogarithmic plot indicates that  $J_0$  can be modeled by [21]:

$$J_0 \propto \exp\left(-\frac{\Delta E_{af}}{kT}\right) \tag{2}$$

where  $\Delta E_{af}$  as activation energy.

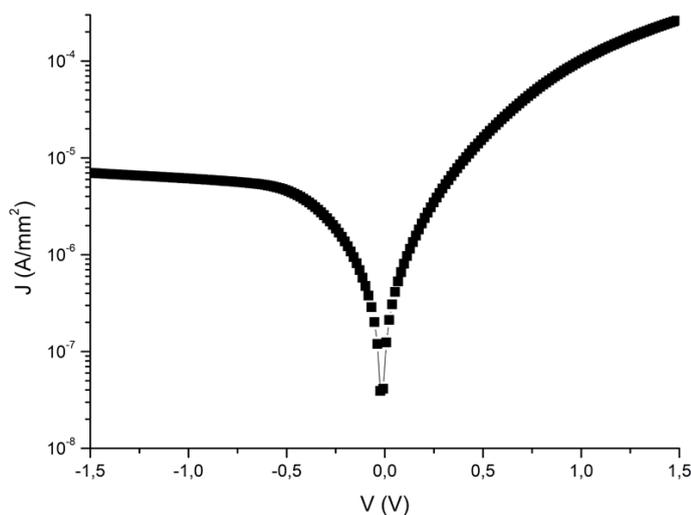


Figure 1. J-V characteristics of an a-GaAs/c-Si heterocontact diode measured at 300 K.

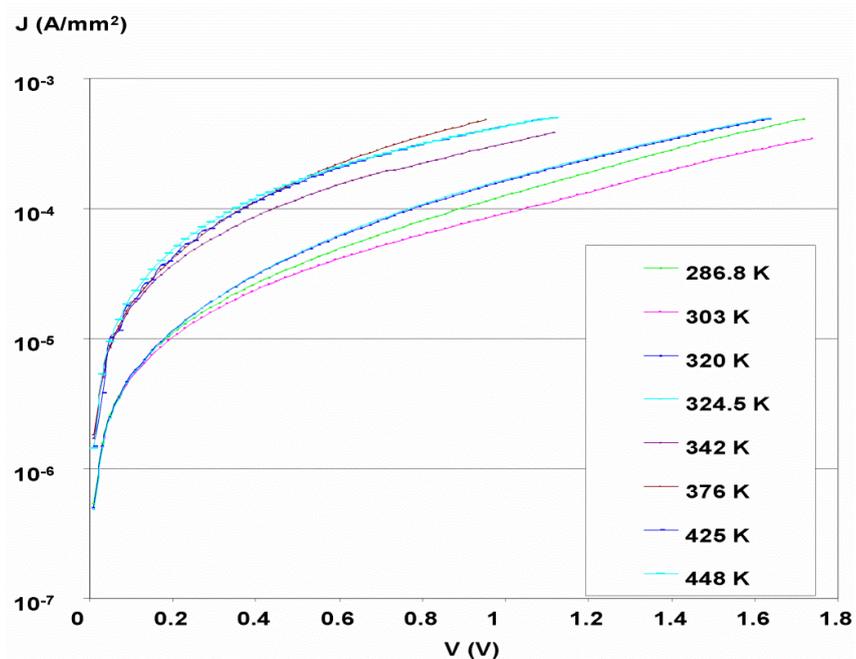
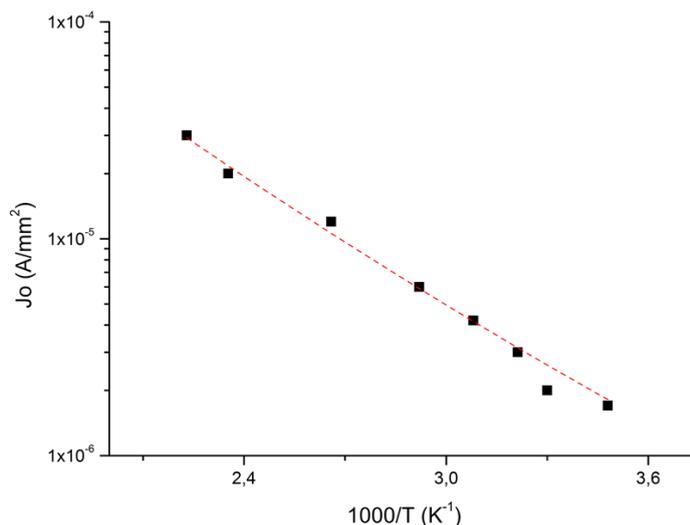
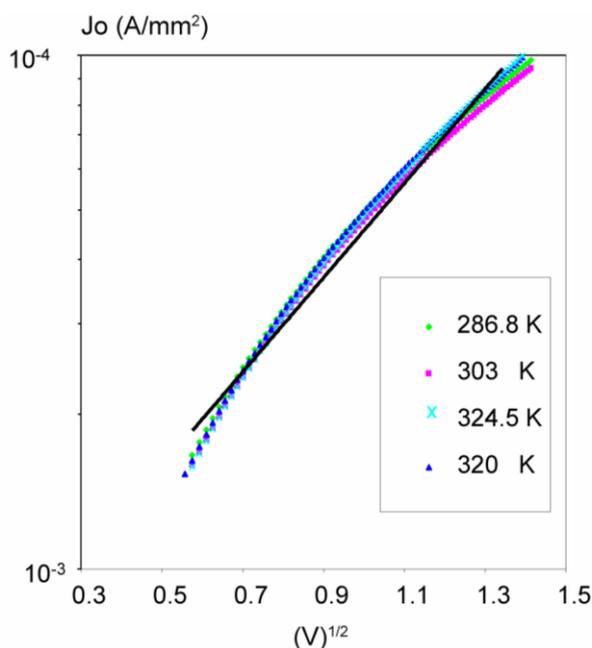


Figure 2. J-V characteristics of an a-GaAs/c-Si heterocontact diode measured at different temperatures in the forward bias voltage regime.



**Figure 3.**  $J_0$  of an a-GaAs/c-Si heterocontact diode as a function of  $1000/T$ .

A least square fit provides a value of the activation energy of  $0.18 \text{ eV} \pm 0.02 \text{ eV}$ . The result is considerably smaller than previously reported values for GaAs/c-Si heterojunctions fabricated by sputtering [19,20], which range from 0.34 to 0.43 eV. This can be explained by different deposition processes: Our samples were deposited at room temperature and sintered later in  $N_2$  atmosphere at  $425 \text{ }^\circ\text{C}$  for 20 min, while in the cited works GaAs was deposited at substrate temperatures of  $150 \text{ }^\circ\text{C}$  [20,21].

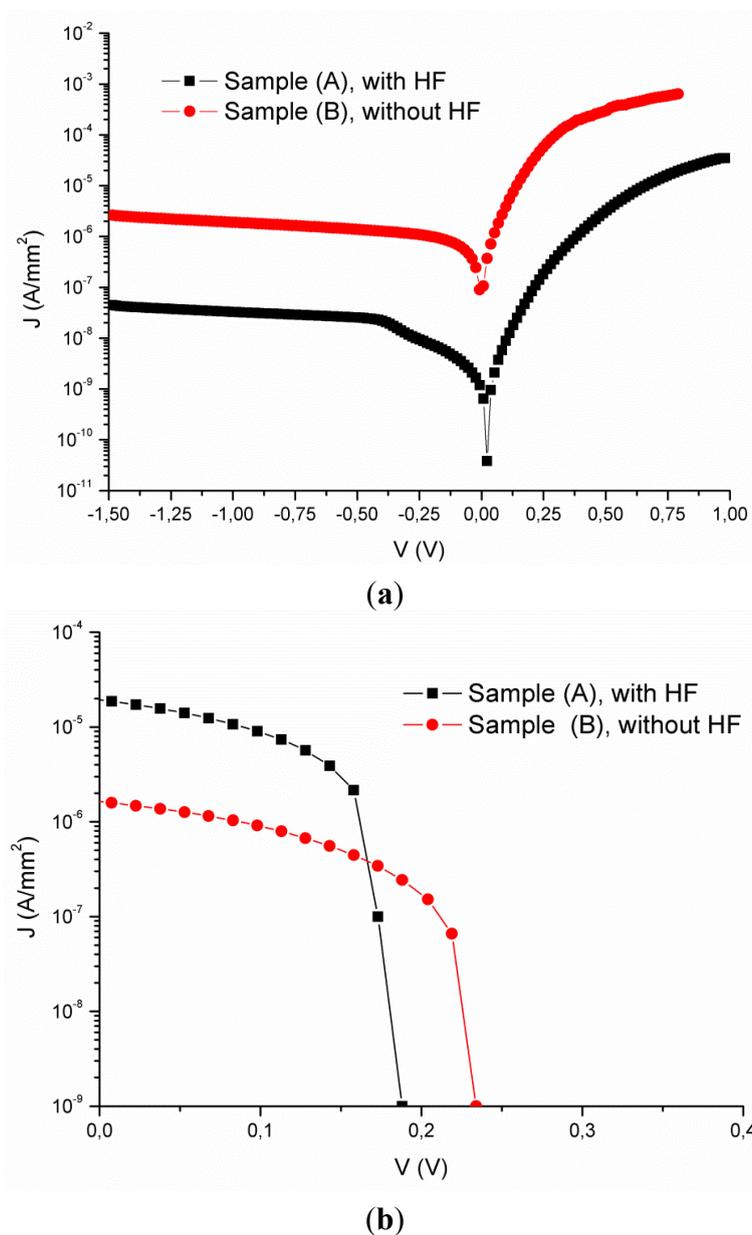


**Figure 4.** Reverse saturation current density of an a-GaAs/c-Si heterocontact diode measured for different temperatures as a function of  $V^{1/2}$ .

Figure 4 shows the reverse saturation current density plotted as a function of  $(V)^{1/2}$  for several temperatures with some kind of a linear behavior on the semilogarithmic scale in the reverse bias voltage regime ( $-2 \text{ V}$  to  $-0.4 \text{ V}$ ). This result indicates that the reverse saturation current density is probably limited by generation-recombination processes [29,30].

3.2. Solar Cell Photovoltaic Characteristics

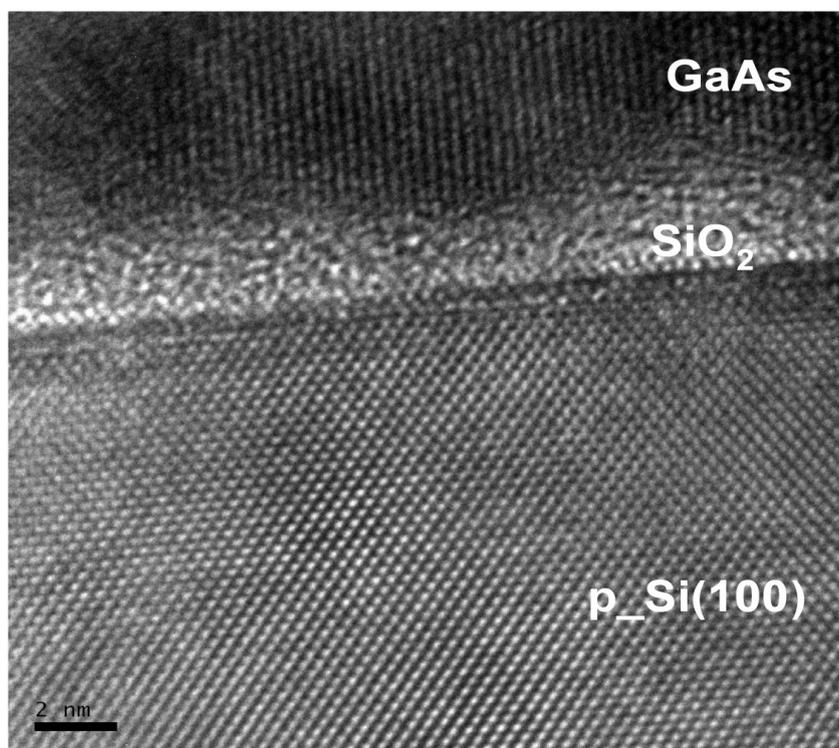
The HF treatment has a strong effect on the interface quality of the heterojunction as it can be seen in Figure 5a. The device without HF treatment (sample B) shows a dark saturation current density value that is roughly two orders of magnitude lower than that of the device where the HF treatment was applied (sample A).



**Figure 5.** J-V characteristics of an a-GaAs/c-Si heterocontact solar cell under dark conditions (a) and under standard illumination conditions (b).

J-V measurements under STC are shown in Figure 5b. For the HF treated device an increase of the short circuit current density is observed whereas the open circuit voltage is decreased. The open circuit voltages under illumination are 173 mV and 234 mV for samples A and B, respectively, which is consistent with the values of the saturation current density.

The values of the short circuit current density are  $2 \times 10^{-5} \text{ A/cm}^2$  and  $3.7 \times 10^{-6} \text{ A/cm}^2$  for samples A and B, showing that the HF treatment improves the photocurrent. This result can be explained by the quality of the GaAs/c-Si interface. In Figure 6, a TEM picture of the GaAs/c-Si heterocontact region of a sample prepared without HF treatment is shown in cross section geometry. A thin amorphous  $\text{SiO}_x$  can be observed at the GaAs/c-Si interface, which is due to the native oxide at the surface of the Si. Moreover, the GaAs film appears to be amorphous as well. The fill factors (FF), series ( $R_s$ ), and shunt resistances ( $R_p$ ) of samples A and B are given in Table 1.

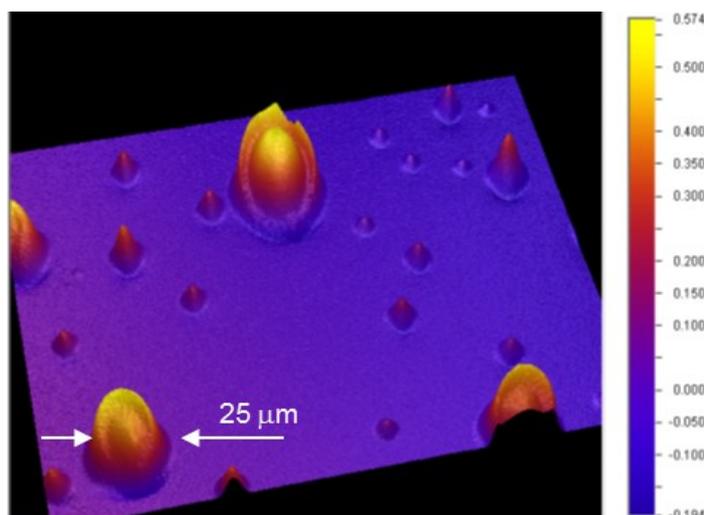


**Figure 6.** Transmission electron microscopy TEM micrograph of GaAs/Si interface.

**Table 1.** Summary of solar cell parameters of samples A and B.

	Sample A (with HF)	Sample B (without HF)
$R_s$ ( $\Omega$ )	1880	4390
$R_p$ ( $\Omega$ )	112	240
FF (%)	25.6	10.36

We have also analyzed the effect of the annealing step performed before or after the ITO deposition on samples that were treated with HF prior to the GaAs sputtering. Figure 7 shows a typical image of the sputtered GaAs surface after the heat treatment without any ITO layer using a VEECO Mic Interferometer.

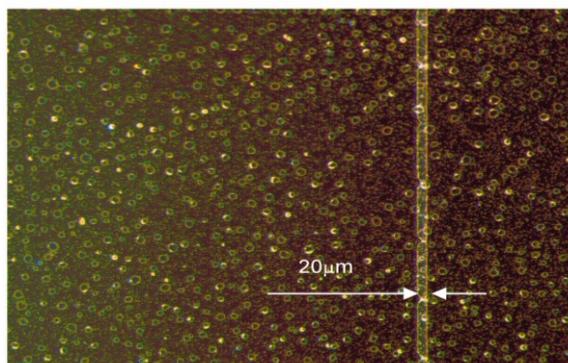


**Figure 7.** Front surface details of the GaAs absorber of an a-GaAs/c-Si heterocontact solar cell after an annealing (details in the text).

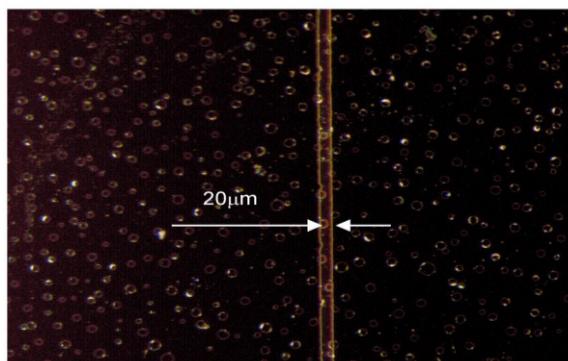
As it can be seen in Figure 7, many structures up to a diameter of 25  $\mu\text{m}$  are visible on the front side of the a-GaAs/c-Si heterocontact solar cell similar to oval defects and mounds which are observed on MBE grown GaAs where gallium droplets are formed [31–33]. Even under arsenic-rich growth conditions gallium droplets can be seen in the GaAs surface [21,33]. Furthermore, the thermal treatment causes a reduction of the As concentration in the GaAs film favoring its recrystallization, which can promote the apparition of gallium droplets due to stoichiometry changes [25–28]. Excessive As tends to migrate to the surface of the sample and sublimates during the thermal step [27].

In our research, we also focused on the effect of an annealing step before or after the ITO deposition procedure. The results are shown in Figure 8a,b. As it can be seen, the density of defect like structures on the front side of the solar cell is considerably reduced in case the ITO layer is deposited prior to the annealing. This fact has also implications on the electrical performance of the solar cells as shown in Figure 9. There, an increase of the open circuit voltage to a value of 250 mV is observed along with an increase of the short circuit current density to  $4.2 \times 10^{-5} \text{ A/mm}^2$  and an improved fill factor. We conclude that both, the saturation current density and the layer resistance are significantly reduced by protecting the GaAs layer with the ITO layer prior to the heat treatment. As it can be seen in Figure 9 the series resistance of sample 1 is lower than the series resistance of sample 2. The solar conversion efficiencies are 0.26% and 0.09% for samples 1 and 2, respectively. These values, even if they are low, exceed efficiencies that were recently reported for heterojunction solar cells on a highly doped GaAs Substrate with an intermediate undoped epitaxial Si layer followed by a doped amorphous Si absorber both deposited by PECVD [19].

The spectral response (SR) measurements of these samples are shown in Figure 10. The photogenerated current is clearly increased on the sample with the ITO layer deposited before the thermal treatment.

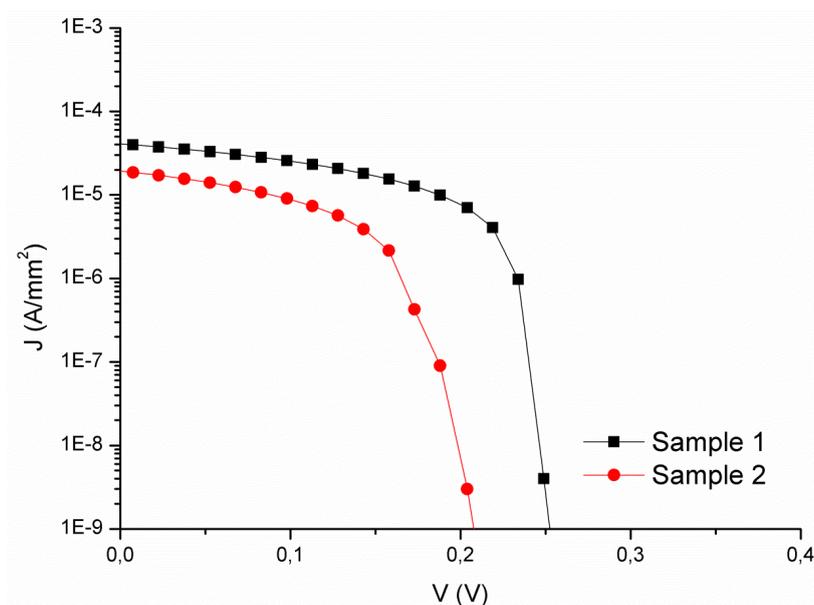


(a) Sample 1

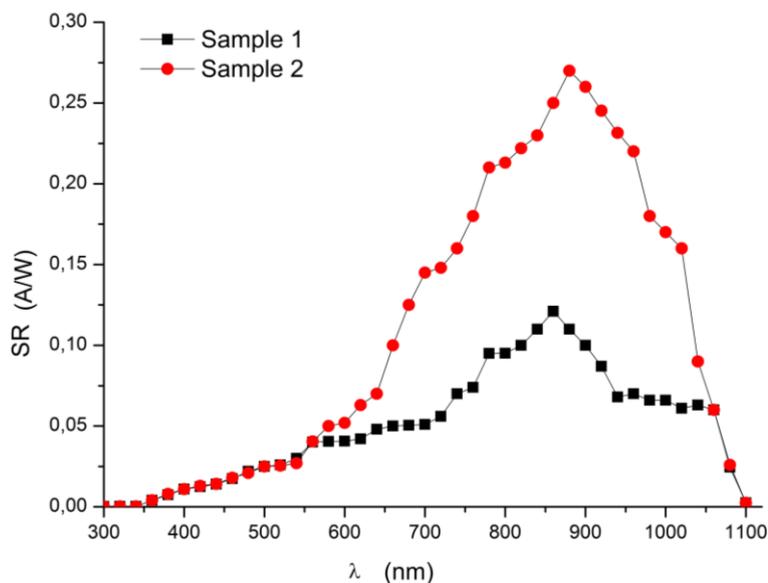


(b) Sample 2

**Figure 8.** Details of the front contact region of the a-GaAs/c-Si heterocontact solar cell. (a) Thermal treatment before ITO deposition. (b) Thermal treatment after ITO deposition. The vertical bars in the figure are Au collecting fingers.



**Figure 9.** J-V characteristics of an a-GaAs/c-Si heterocontact solar cell under standard illumination conditions. Sample 1: Annealing after ITO deposition; Sample 2: Annealing before ITO deposition.



**Figure 10.** Spectral response (SR) of different samples with the thermal treatment taken place before (sample 1) and after (sample 2) the ITO deposition.

#### 4. Conclusions

Thin films of a-GaAs were deposited by sputtering on p-Si(100) to fabricate heterojunction diodes and solar cells.

The amount of surface defects on the GaAs layer was reduced by the deposition of an ITO capping layer prior to the heat treatment of the interface. This interface shows a very thin layer of silicon dioxide, which can be removed by an HF treatment. However, the first few nanometers of the deposited GaAs film present an unexpected good crystallinity. The results show important changes in the dark saturation density current and on the interface resistance due to the HF treatment. The photovoltaic properties of the fabricated solar cells are significantly improved by a thermal annealing step of the a-GaAs/c-Si layer system prior to the deposition of the thin ITO film.

The heterojunction diodes show marked rectification characteristics, with forward currents dominated by tunneling mechanisms, while reverse currents are limited by the generation of carriers in the depletion region. An activation energy of 0.18 eV was obtained from I–V measurements at different temperatures which is relatively small compared to previously reported values. We attribute this to different deposition conditions leading to a changed interface with a reduced conduction band offset.

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#### Author Contributions

These authors contributed equally to this work.

## Conflicts of Interest

The authors declare no conflict of interest.

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