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Review

Variability and Reliability of Single-Walled Carbon Nanotube Field Effect Transistors

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Abstract: Excellent electrical performance and extreme sensitivity to chemical species in semiconducting Single-Walled Carbon NanoTubes (s-SWCNTs) motivated the study of using them to replace silicon as a next generation field effect transistor (FET) for electronic, optoelectronic, and biological applications. In addition, use of SWCNTs in the recently studied flexible electronics appears more promising because of SWCNTs' inherent flexibility and superior electrical performance over silicon-based materials. All these applications require SWCNT-FETs to have a wafer-scale uniform and reliable performance over time to a level that is at least comparable with the currently used silicon-based nanoscale FETs. Due to similarity in device configuration and its operation, SWCNT-FET inherits most of the variability and reliability concerns of silicon-based FETs, namely the ones originating from line edge roughness, metal work-function variation, oxide defects, *etc.* Additional challenges arise from the lack of chirality control in as-grown and post-processed SWCNTs and also from the presence of unstable hydroxyl (–OH) groups near the interface of SWCNT and dielectric. In this review article, we discuss these variability and reliability origins in SWCNT-FETs. Proposed solutions for mitigating each of these sources are presented and a future perspective is provided in general, which are required for commercial use of SWCNT-FETs in future nanoelectronic applications.

Keywords: single-walled carbon nanotube; field effect transistor; variability; reliability; hydroxyl group passivation; oxide defect; hysteresis; noise; radiation dose; degradation

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1. Introduction

Single-Walled Carbon NanoTubes (SWCNTs) were first discovered in 1991 [1] and their electronic properties depend on the directions at which two-dimensional graphene stripes are (hypothetically) rolled to make SWCNTs [2–4]. When a SWCNT is defined by rolling a graphene layer and by joining any of the solid symbols of Figure 1a with the lattice origin $(a_1,a_2) = (0,0)$, resultant SWCNT will have metallic properties with no bandgap in the energy *vs.* density of the state's relationship (Figure 1b). On the other hand, SWCNTs defined by joining the open symbols of Figure 1a with the lattice origin will have semiconducting properties with bandgaps (Figure 1c,d) that can be expressed as [2,3]:

$$E_G = \frac{2a_{C-C}|t|}{d}. \quad (1)$$

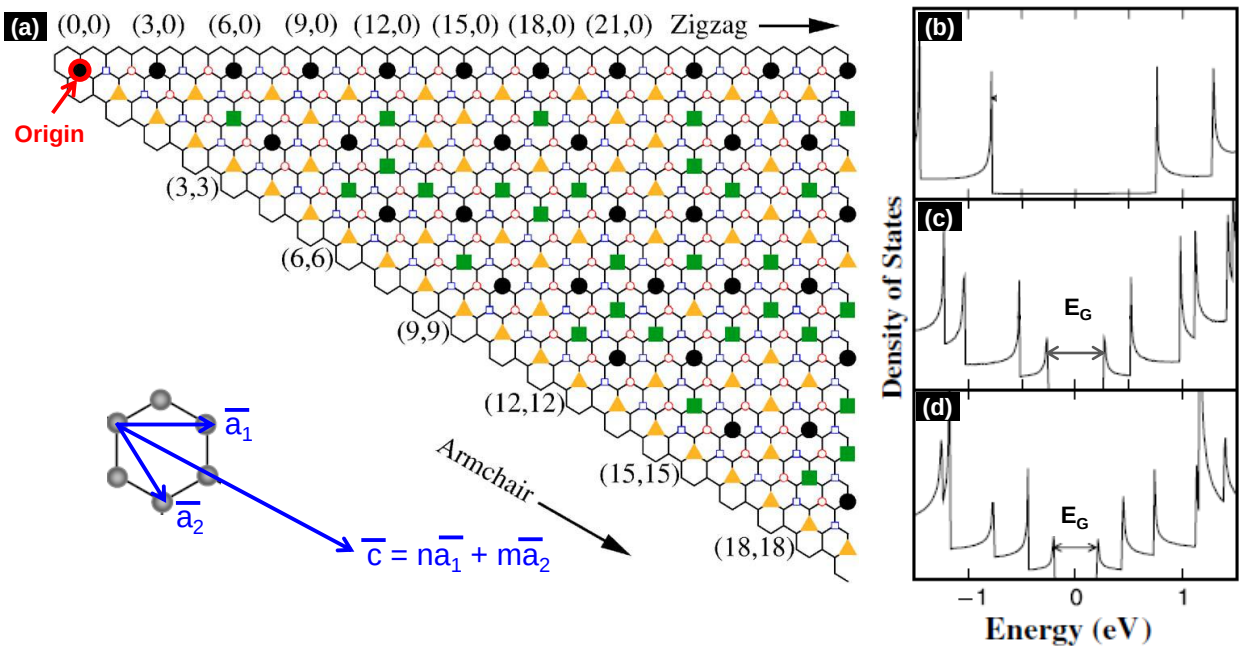
In Equation (1), d is the diameter of SWCNT and equals $\sqrt{3}a_{C\text{-}C}/\pi \times \sqrt{(n^2 + nm + m^2)}$, (n,m) is the chiral index designating the distance between the open symbols and the lattice origin via chiral vector $\bar{c} = n\bar{a_1} + m\bar{a_2}$ (Figure 1a), $a_{C\text{-}C}$ = 0.142 nm is the C–C bond length, $t \sim -3$ eV is the C–C bonding energy. SWCNTs with $n = m$ are called armchair nanotubes and always show metallic behavior, whereas SWCNTs with $n \neq m$ either show metallic behavior for mod $(n - m)/3 = 0$ or semiconducting behavior for mod $(n - m)/3 = 1, 2$. SWCNTs with $m = 0$ are called zigzag nanotubes and the rest with $n \neq m \neq 0$ are called chiral nanotubes.

Semiconducting SWCNTs (s-SWCNTs) are of particular interest for future electronic devices, where s-SWCNTs act as a channel in conventional field effect transistor (FET) configuration. Carrier mobility in such s-SWCNT-FETs can be as high as ~10^5 cm^2/V-s [5,6], which outperforms similar values in current-day FETs. In addition, the ultra-thin s-SWCNT layer that forms the channel of FET offers better electrostatic gate control, hence less short channel effect compared to classical silicon-based FETs [7]. Such ultra-thin layers also offer extreme mechanical flexibility to the resultant electronic device, thereby promoting the best platform for future flexible electronic devices [8,9], which are currently being manufactured using FETs made on thin silicon substrates [10,11]. Use of s-SWCNTs as channels, m-SWCNTs as contacts [12] and memory elements [13], SWCNT network [14,15] or single s-SWCNT [16,17] as memory, and CNT fabrics as coaxial cable [18] may open up the possibility of having "all-CNT" electronics for high performance applications. In addition to electronics, SWCNT-FETs are also considered as chemical-/bio-sensors because of their higher surface-to-volume ratio that reduces response time [19] and extreme sensitivity [20,21], and their selectivity [20] to chemical and biological species.

To enable all these applications stated in the last paragraph, SWCNT-FETs and memories not only require superior performance, but also require a controlled level of variability and reliability. Such controllability has to ensure that performance of associated devices does not drop below a certain limit, which can be compensated through circuit design via guard bands [22,23]. Figure 2 schematically explains the extent of guard band that is used in circuit design for handling variability and reliability. Devices have different variability sources that give rise to time-zero variation in device performance around its mean value. In addition, during the operation of the device, its performance degrades over time and such degradation comes with its own statistical variation. Based on this knowledge, circuits are designed with such devices considering that the tail of the performance distribution at the end of

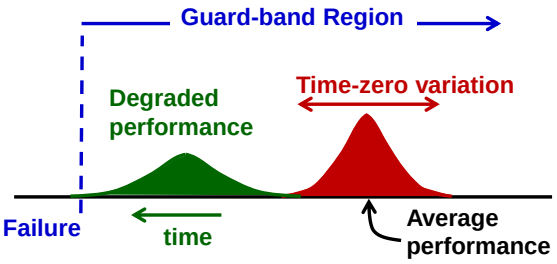
intended lifetime will not go beyond a certain limit—thus, the designed circuits are guard-banded against performance variations. As device performance improves via Moore's law scaling [24], device design is continuously modified to minimize guard-band such that the devices can be operated at higher performance without compromising the lifetime.

Figure 1. (**a**) Two-dimensional graphene lattice for defining structures of (*n*,*m*) Single-Walled Carbon NanoTubes (SWCNTs) (reprinted with permission from Ref. [3]; © 2005 by the American Physical Society.). Definition of lattice vectors a_1, a_2 with respect to carbon atoms in the graphene lattice is shown in the bottom part of the figure. SWCNTs can be formed by rolling this sheet to join the origin (a_1,a_2) = (0,0) with other points. Joining the open symbols with the origin makes semiconducting SWCNTs, while joining the solid symbols with the origin makes metallic SWCNTs. (**b**) Density of states (DOS) *vs.* energy plot obtained using a tight binding model [4] for an armchair (10, 10) SWCNT having metallic property. (**c**,**d**) DOS + energy plot for a chiral (11, 9) SWCNT and a zigzag (22, 0) SWCNT. Both these SWCNTs have semiconducting properties and a chirality-dependent band gap (E_G) defined using Equation (1). (**b**–**d**) are reprinted with permission from Ref. [4]; © 2003 IOP Publishing Ltd and Deutsche Physikalische Gesellschaft, Published under a CC BY-NC-SA license.



In this review article, we will discuss different aspects of variability and reliability in SWCNT-FETs that will eventually define guard-band in such devices. Section 2 discusses the configurations and performance of SWCNT-FETs that has potential use in future electronics. Section 3 highlights the sources of variability in SWCNT-FETs and the current solutions to control them. Section 4 performs a similar review for the reliability sources. Section 5 summarizes the paper and provides brief guidelines for improving variability and reliability phenomena in SWCNT-FETs based on current understanding of CNT growth conditions and device fabrication challenges.

Figure 2. Schematic representation of the amount of guard-band that is used in electronics for handling process (or time-zero) variation and reliability (time dependent variation) in device performance. The performance of a device has a distribution over and above its mean value and it degrades over time. Once of the tail of performance distribution for the device reaches the guard-band margin, the associated device is designed to fail.

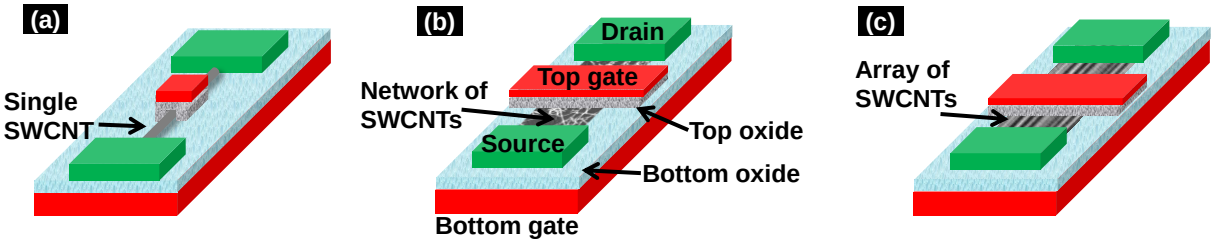


2. Configurations and Performance of SWCNT-FET

2.1. Device Geometry

For FET applications, SWCNTs are commonly grown in random networks or aligned arrays using metal catalyst placed on SiO_2 [9,12,25,26]. Alternately, SWCNTs are drop-casted from solution on SiO_2 [27–29] or hafnium dioxide (HfO_2) [30,31] and assembled in random networks [27–29] or parallel arrays [31,32] via coating of self-assembled monolayers on oxides. Bottom-gated FETs with thick SiO_2 as gate dielectric and heavily doped silicon as gate are widely used test configurations for SWCNT-FETs. Such bottom-gated structures though are suitable for bio-/chemical-sensing applications [20,21,33], top-gated geometry with thin, high-κ gate dielectric is preferred for high performance electronics [34,35]. (In some novel SWCNT-FETs, local bottom-gating [36], lateral gating with suspended SWCNTs [37], and surround-gate geometries [38] are also used for high performance electronics.) Measurement of SWCNT properties (e.g., conductivity, mobility, contact resistance of individual SWCNTs and their diameter dependence) by applying suitable bias at source, drain, and gate terminals involves fabrication of single SWCNT-FET. Schematic of such a FET in dual-gate (*i.e.*, having top and bottom gate with suitable gate oxides) configuration is shown in Figure 3a. Such single SWCNT-FET, however, cannot provide the amount of current required for different applications, e.g., ~mA per μm of channel width is required for high performance electronics [35]. Current in SWCNT-FETs can be increased either by having a network (Figure 3b) or an aligned array (Figure 3c) of SWCNTs' bridging sources and drain terminals. Magnitude of current in these configurations depends on the density of SWCNTs (per unit area for network SWCNTs of Figure 3b or per unit width across the length of SWCNTs for aligned SWCNTs of Figure 3c), diameter of SWCNTs, chirality of SWCNTs, and electrostatic coupling on SWCNTs via gate. For network SWCNT-FETs, current additionally depends on the charge transfer efficiency across different SWCNTs in the network [39–41].

Figure 3. Schematic representation of SWCNT-based field effect transistor (FETs) in top- and bottom-gated configuration for (**a**) single SWCNT, (**b**) SWCNT networks, and (**c**) aligned array SWCNTs. Generally, SWCNTs are grown or coated on oxides and then the source, drain, top oxide and top gate are formed on top of them via lithography. Though the schematics here show partial coverage of SWCNTs in between source and drain, the actual top-gate SWCNT-FET application uses full coverage of SWCNTs.



2.2. Materials for SWCNT-FETs

As mentioned before, SWCNTs are grown on insulating substrates like SiO_2, quartz, sapphire, *etc.* using metal (e.g., Fe, Ni, Co and their alloys) nanoparticles as catalyst. Length, diameter distribution, and chirality of grown SWCNTs vary among the growth methods being used [42,43]. In general, for as-grown SWCNTs, length varies from ~1 μm to several 100 μm, diameter ranges between ~0.7 nm and ~5 nm [26,44–46], density is approximately 14–200 per μm^2 for network SWCNTs [12,31] and ~2–45 per μm across the length of the SWCNT for aligned SWCNTs [26,31,44,47,48], and chirality varies randomly. Long SWCNTs (>100 μm) are only obtained during chemical vapor deposition (CVD) on stable temperature- (ST-) cut quartz substrates [25,49]. Diameter and chirality of as-grown SWCNTs can be sorted by dissolving SWCNTs in surfactants and then using post-processing techniques like ultra-centrifugation [50], gel electrophoresis [51], chromatography [52]. Such solution-processed, sorted SWCNTs can be assembled into a high-density compact film via Langmuir-Blodgett method [35]. However, solution-processing breaks SWCNTs into small segments (~μm or less) and reduces the carrier mobility or conductivity of SWCNTs (down to ~1–20 cm^2/V-sec [35,46] with a maximum of ~200–300 cm^2/V-sec [28,53]). An alternative approach of maintaining the integrity of SWCNTs in terms of length (up to several hundreds of μm) and carrier mobility (>1000 cm^2/V-sec) is to coat horizontally aligned SWCNTs with a molecular film and use thermo-lithography (thermal analogous of photo-lithography) to etch-off m-SWCNTs from the substrate [54]. Remaining s-SWCNTs have a low density; however, there is potential for density improvement via multiple transfers [55,56].

In addition to the requirement of having substrates with high density s-SWCNTs, future electronic devices require appropriate doping in s-SWCNTs to control their conduction. Absence of molecular doping in SWCNTs, however, necessitates the use of metals with lower (higher) work-functions to conduct electrons (holes) through the SWCNTs, hence make n- (p-) type SWCNT-FETs. Palladium (Pd) with work-function of ~5.1 eV is generally used as source/drain contacts for making p-type SWCNT-FETs that allows hole flow from contacts into and out of the SWCNT via Schottky contacts for d < 1 nm SWCNTs and via ohmic contact for d > 1 nm SWCNTs [57–59]. Presence of negatively charged hydroxyl (-OH) groups at SWCNTs interface also makes the p-type conduction in

SWCNT-FETs easier. N-type or electron conduction in SWCNTs, on the other hand, can be enabled using calcium (Ca) and scandium (Sc) source/drain contacts with work-functions ~3–4 eV [60,61]. In such case, conduction can be further enhanced via electrostatic doping with high-κ oxides [38,62].

2.3. FETs with Single SWCNT

Current-voltage (I-V) characteristics of FETs with single s-SWCNT have reasonably good switching behavior in the measured transfer characteristics (*i.e.*, drain current (I_{ds}) *vs.* gate voltage (V_g) characteristics, as shown in Figure 4a) and good saturation in output characteristics (*i.e.*, I_{ds} *vs.* drain to source voltage (V_{ds}) characteristics, as shown in Figure 4b) for any channel length (L_{ch}) down to ~10 nm [63]. These FETs have predominant p-type behavior because of the natural presence of –OH groups at the interface of SWCNTs. On-current (I_{on}; defined as I_{ds} at a certain high $|V_g - V_t|$, where V_t is the threshold voltage of a FET) and off-current (I_{off}; defined as the minimum of I_{ds}) in these FETs with single s-SWCNT show variation with d and source/drain contact material being used. Contacts with higher work-function (Φ_{WF}) can inject holes into the valence bands of s-SWCNTs more easily and have larger I_{on} and I_{off} (Figure 4c,d); [44,58,59]), especially for larger diameter s-SWCNTs that have smaller band-gap, E_g (see Equation (1)) and hence have negligible hole injection barrier at the metal/s-SWCNT interface. Therefore, contacts play a major role in the conduction of SWCNT-FETs and are considered to have dominant contribution in limiting I_{ds} in the near ballistic limit [28,63], when L_{ch} is much less than the channel mean free path that defines mobility. Sub-threshold slope (SS; defined as $\partial V_g/\partial(log_{10}I_{ds})$ in the region with $V_g << V_t$) for FETs with single s-SWCNT varies from ~80–95 mV/dec and increases with a decrease in L_{ch} due to ambipolar conduction [64]. (Use of appropriate chemical coating on SWCNT in a dual-gate device configuration can reduce SS to 63 mV/dec [65], which is close to the theoretical limit of $SS = 2.3k_BT/q \sim 60$ mV/dec at room temperature for a FET [66]; here, k_B is the Boltzmann constant, T is temperature in °K, and q is the electron charge.) Hole effective mobility ($\mu_{eff,h}$) of s-SWNTs ranges from ~10^3–10^5 cm^2/V-sec [5,6,25,63,67] and increases with d [5]. Such $\mu_{eff,h}$ value depends on CNT growth conditions and is better for CVD-grown CNTs compared to solution-processed CNTs [28].

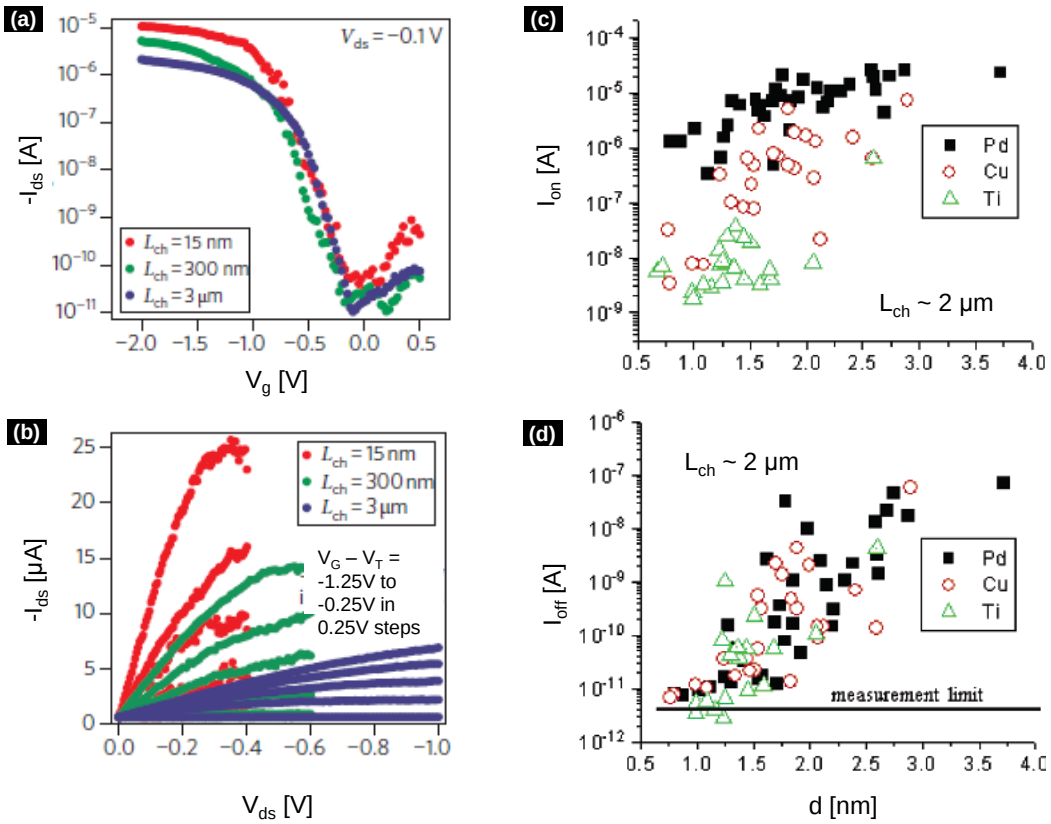
In contrary to s-SWNTs, FETs with single metallic (m-) SWCNT-FETs have very small gate modulation and show ambipolar behavior with a smaller n-type tail (Figure 5a). Such gate modulation is often attributed to the presence of Mott-insulating states [68] and/or strain-induced bandgap [69] in m-SWCNTs. FETs with s-SWCNTs also show ambipolar behavior, more significantly at higher $|V_{DS}|$ and for larger diameter s-SWCNTs (Figure 5b) due to band-to-band tunneling (BTBT) [70].

2.4. FETs with Multiple SWCNTs

Multiple SWCNTs in FET's channel are either arranged randomly as network or aligned parallel to each other bridging source and drain. Network SWCNT-FETs can be made using CVD-grown SWCNTs with mixed chiralities (Figure 6a shows a scanning electron microscope (SEM) image for one such bottom-gated FET near a source/drain contact). These FETs have low on/off ratio, unless the conduction through metallic SWCNTs is turned off via periodic stripping [9]. An alternate way of improving on/off ratio is to use solution-processed, chirality sorted s-SWCNTs for making FETs.

However, such FETs show lower conductance compared to CVD-grown SWCNTs because of the presence of structural defects [28].

Figure 4. (**a**) Transfer or I_{ds}-V_g and (**b**) output or I_{ds}-V_{ds} characteristics of single s-SWCNT-FETs (reprinted by permission from Macmillan Publishers Ltd: Nature Nanotechnology [63], © 2010). Diameter dependence of (**c**) on-current I_{on} and (**d**) off-current I_{off} for s-SWCNT-FETs using different types of metals (palladium: Pd, copper: Cu, titanium: Ti) as source/drain (reprinted with permission from Ref. [58], © 2006 American Chemical Society.). In general, easier hole conduction for higher work-function (Φ_{WF}) contact metals like Pd results higher I_{on} and I_{off} for associated FETs.



Network SWCNTs have impedances at the junctions of different SWCNTs; consequently, they have lower conductance and are suitable only for applications like non-volatile memories [14,15]. Parallel arrangement of aligned SWCNTs resolves the issue with junction impedance and promises applications of SWCNTs in high performance radio frequency (RF) electronics [47,71,72], and transparent electronics [73,74]. Figure 6b shows a SEM image of one such top-gated FET before gate dielectric and gate metal formation. These aligned array SWCNT-FETs are either fabricated by growing SWCNTs via CVD on special types of quartz or sapphire substrates, whose crystal orientations [49] and/or step-edges [75,76] help parallel alignment (with less than 0.1% imperfection [77]) of d ~ 0.7~3 nm SWCNTs [26,44,45], or fabricated by aligning solution-processed SWCNTs via dielectrophoresis [46]. CVD-grown SWCNTs are long (with a length of several hundreds of μm [77]) and have high conductivity [5,25,63,67], however, require the use of post-processing techniques like thermo-lithography [54] and laser irradiation [78] for removal of

m-SWNTs, or electrical breakdown [79] for breaking the continuity of m-SWNTs, and hence, cause FETs to use the remaining s-SWNTs.

Figure 5. (**a**) Transfer characteristics of single metallic (m-) SWCNT-FETs showing ambipolar behavior (reprinted with permission from Ref. [44]; © 2012, AIP Publishing LLC). (**b**) Ambipolar behavior is also observed for FETs with a d ~ 1.7 nm s-SWCNT and at larger V_{ds} (reprinted with permission from Macmillan Publishers Ltd: Nature Nanotechnology [54], © 2013).

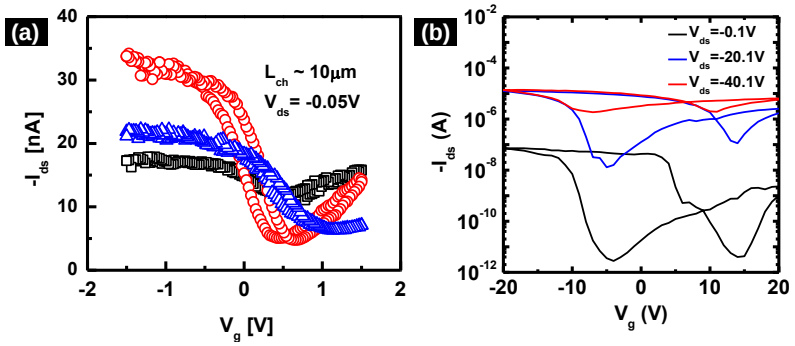
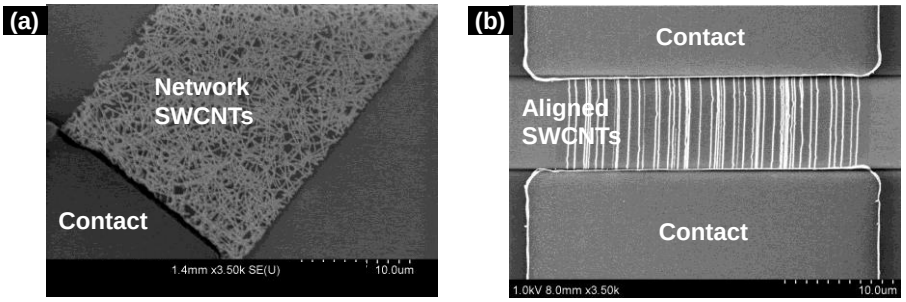


Figure 6. Scanning electron micrograph (SEM) of (**a**) random network of SWCNTs near one of the source/drain contact and (**b**) horizontally aligned SWCNTs bridging source/drain contacts.



3. Variability in SWCNT-FETs

3.1. Variability in FETs with Single SWCNT

Performance variation in FETs with single s-SWCNT arises from the variation in d, contact and gate metals' Φ_{WF}, L_{ch}, T_{ox} (oxide thickness), and interface and oxide defects from one FET to another. For FETs with L_{ch}>µm, variation in d can give rise to several orders of magnitude change in I_{ds}, as shown in Figure 7a for small V_{ds} = −50 mV. One can simulate such transfer characteristics for different d (dashed lines in Figure 7a) by considering the conductance of the FET (G_{ds}) as a series combination of conductances of s-SWCNT (G_{ss}; see Ref. [44] for appropriate expressions) and contact ($G_c = G_{c0}T_c$; where T_c is the transmission probability of carriers near the source/drain contact) with components from both electron (e) and hole (h), *i.e.*,

$$G_{ds} = G_{ds,e} + G_{ds,h} = \left(G_{ss,e}^{-1} + G_{c,e}^{-1}\right)^{-1} + \left(G_{ss,h}^{-1} + G_{c,h}^{-1}\right)^{-1}, \quad (2)$$

and hence, calculate I_{ds} using $I_{ds} = G_{ds} \times V_{ds}$. Simulated results for 0.6 nm < d < 1.75 nm are consistent with measurement at $V_g < V_t$, where G_{ss} dominates G_{ds}. The differences in the region of $V_g > V_t$, where G_c dominates G_{ds}, partly reflect variation in the fixed component of G_c [80] that is not considered in simulation and also reflect I_{ds} measurement limitation set at ~pA. Plots of diameter dependence of I_{on} ($\equiv I_{ds}$ @ $V_g - V_t = -1$V, V_{ds} = 50 mV), maximum transconductance $G_{m,max}$ ($\equiv$max $|\partial I_{ds}/\partial V_g|$), and V_t (Figure 7b) provide additional detail about the origin of performance variation in s-SWCNT FET. At large diameters, when the transmission of carriers through the Schottky barrier near the contacts is unity, variation of $I_{on} \sim d$ and $G_{m,max} \sim d^2$ originates from the diameter dependence of μ_{eff} in s-SWNTs [5,81,82]. Similarly, variation of V_t ($\equiv V_g$ @ $|I_{ds}| = |I_{ds,max}|/100$) with d follows that of I_{on}. At small diameters, non-linear dependence of transmission through the contact Schottky barrier leads to a non-linear variation in I_{on}, $G_{m,max}$, and V_t with d.

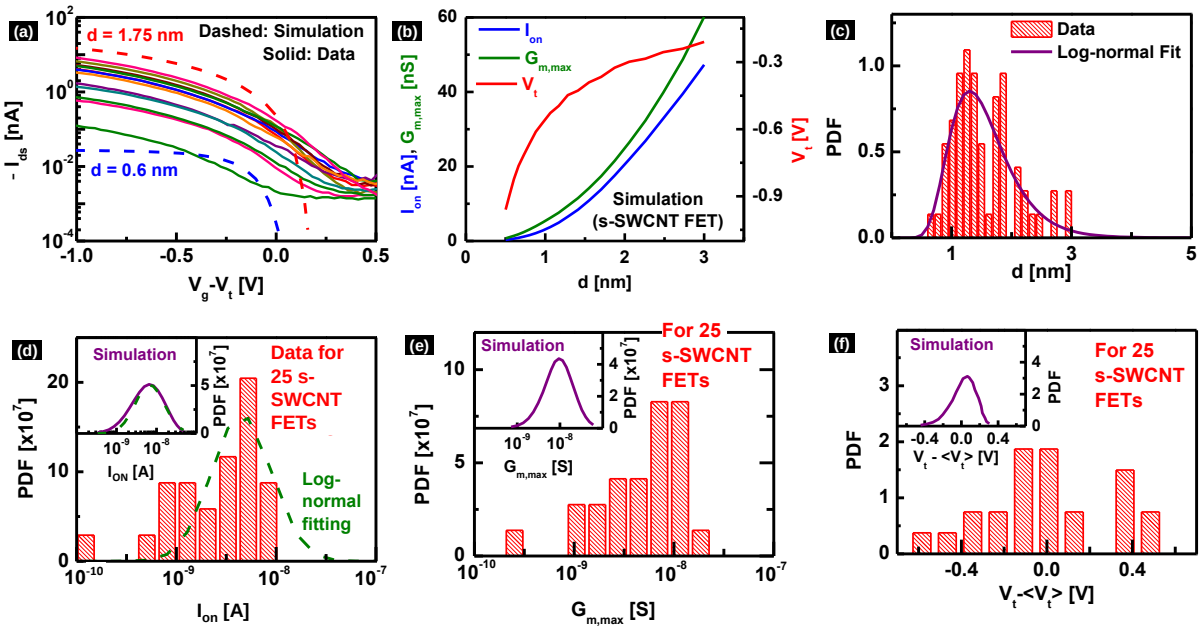
Simulated I_{on}, $G_{m,max}$, and V_t distributions (calculated using diameter distribution of Figure 7c and variations of I_{on}, $G_{m,max}$, and V_t *vs.* d from Figure 7b) suggest good consistency with respective measurements (Figure 7d–f). Similar to the diameter distribution of Figure 7c, I_{on} distribution fits log-normal statistics, except near the lower tails of the distribution where transport through the contacts' Schottky barrier with $T_c < 1$ dominates I_{ds}. Measured $V_t - \langle V_t \rangle$ distribution (where $\langle V_t \rangle$ is the average of the distribution) is wider than the simulated one due to the extra contributions from defects [16,83] and gate Φ_{WF} [84,85] variations that is not considered in the simulation. Passivation of SWCNT interface using hydrophobic self-assembled monolayers (SAMs) can tighten the V_t distribution by reducing hydroxyl (–OH) group related interface defects [86]. Figure 8a demonstrates utility of such SAM-based approach for reducing V_t distribution, where $L_{ch} <<$ µm s-SWCNT FETs are made using solution-processed SWCNTs and passivated with hexamethyldisilazane (HMDS). As in CVD-grown s-SWCNTs, distribution in G_m (Figure 8b) for such solution-processed s-SWCNT FETs follows that of diameter (Figure 8c). In addition, contact resistance $R_c = 1/G_c$ in such small L_{ch} s-SWCNT FETs plays a dominant role in transport. Distribution of R_c (Figure 8d) arises from variations in T_c with d [28] and also from variations in the contact's Φ_{WF}. In contrary, FETs with m-SWCNT and similar L_{ch} have tighter R_c distribution [28]; however, they still suffer from variations in I_{ds} (Figure 8e) and, hence, G_m (Figure 8f). Since m-SWCNTs are unattractive for high performance electronics applications requiring high I_{on}/I_{off}, parametric variations in m-SWCNT FETs are not well studied.

3.2. Variability in FETs with Multiple SWCNTs

Similar to single SWCNT-FETs, performance variation in FETs with multiple SWCNTs originates from variations in d, Φ_{WF}, L_{ch}, T_{ox}, and defects [87–89]. A simple translation of single SWCNT-FET analysis to multiple SWCNT-FET; however, they cannot explain related variations, mostly because of the added complexity coming from variations in the arrangements and types of multiple SWCNTs bridging source/drain contacts. Multiple SWCNT FETs can have random network or aligned SWCNTs with varied density of m- and s-SWCNTs, a wide range of variations in the orientation of SWCNT and its crossings (especially for network SWCNT FET), and a wide distribution in d. This section discusses performance variation in aligned array SWCNT-FETs that have significant promise for high performance device applications. Such FETs have negligible variation in SWCNT's orientation [77]

and also have negligible SWCNT crossings (Figure 6b). For a discussion on variabilities coming from SWCNT's orientation and crossings, which are more relevant for network SWCNT-FETs, please refer to Ref. [41].

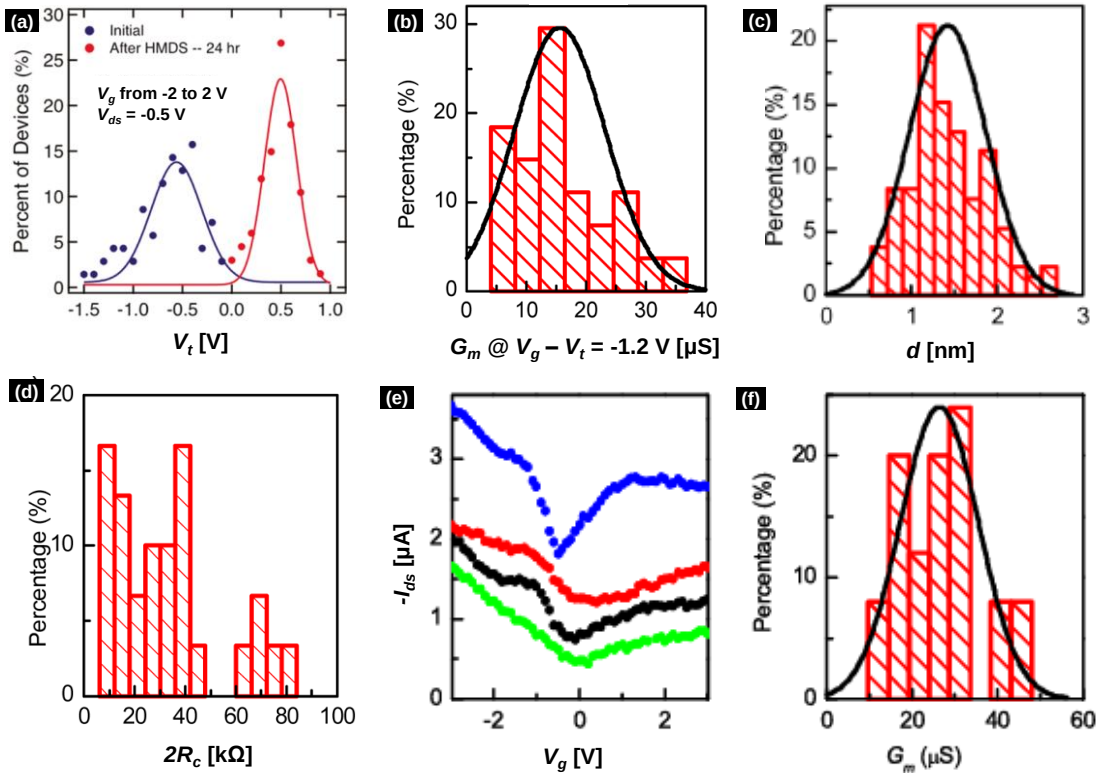
Figure 7. (**a**) Measured I_{ds} *vs.* $V_g - V_t$ ($V_t \equiv V_g$ @ $|I_{ds}| = |I_{ds,max}|/100$) characteristics for single s-SWCNT FETs ($L_{ch} \sim 10$ μm, $V_{ds} = -50$ mV) is within the simulated results for $d = 0.6$ nm and $d = 1.75$nm FETs. (**b**) Simulated I_{on} ($\equiv|I_{ds}|$@ $V_g - V_t = -1$ V, $V_{ds} = -50$ mV), $G_{m,max}$ ($\equiv\max(\partial I_{ds}/\partial V_g)$), and V_t *vs.* d for s-SWCNT FETs. (**c**) Diameter distribution that is used to simulate performance distributions of s-SWCNT FETs in (**d**–**f**). Measured distributions of (**d**) I_{on}, (**e**) $G_{m,max}$, and (**f**) V_t for s-SWCNT FETs agree well with the simulated distributions (insets). For (**f**), $<V_t>$ is the average of V_t distribution. These figures are reprinted with permission from Ref. [44]; © 2012, AIP Publishing LLC.



Solution-processed SWCNTs that are widely used for fabrication of FETs with network and partially aligned SWCNTs have yet to reach the target of 100% chiral selectivity. Some of the resultant FETs, therefore, have high on/off ratios when SWCNT density within the FET is low [35,46]. On the other hand, high performance electronics demand the availability of CVD-grown SWCNTs that always come with a mixture of m- and s-SWCNTs and require the application of post-processing techniques (e.g., electrical breakdown [79], gas-phase reaction [90], thermo-lithography [54]) for having high on/off ratio in multiple SWCNT FETs. In some cases, application of post-processing techniques like electrical breakdown [79] and gas-phase reaction [90] also leads to unwanted removal of s-SWCNTs and, hence, performance degradation or even transistor failure [91]. Considering p_m as the probability of a single SWCNT in the FET being metallic, p_{Rs} as the probability of s-SWCNT being removed via post-processing, *IDC* as the index of dispersion in SWCNT count within the FET, one can simulate the failure probability (p_F) for FETs with aligned SWCNTs at different SWCNT densities (Figure 9a). Such analysis, however, ignores a well-known aspect of 'inferential statistics' [92], *i.e.*, the distributions of SWCNT density and d in macro-scale (population distributions) is not always same as the distributions in micro-scale (sample distributions). As such, performance variability from

diameter variations were expected to diminish for high density multiple SWCNT FETs via statistical averaging [25,41,91], making SWCNT density and m-SWCNT's presence as the major contributors to performance variations (Figure 9b) [91].

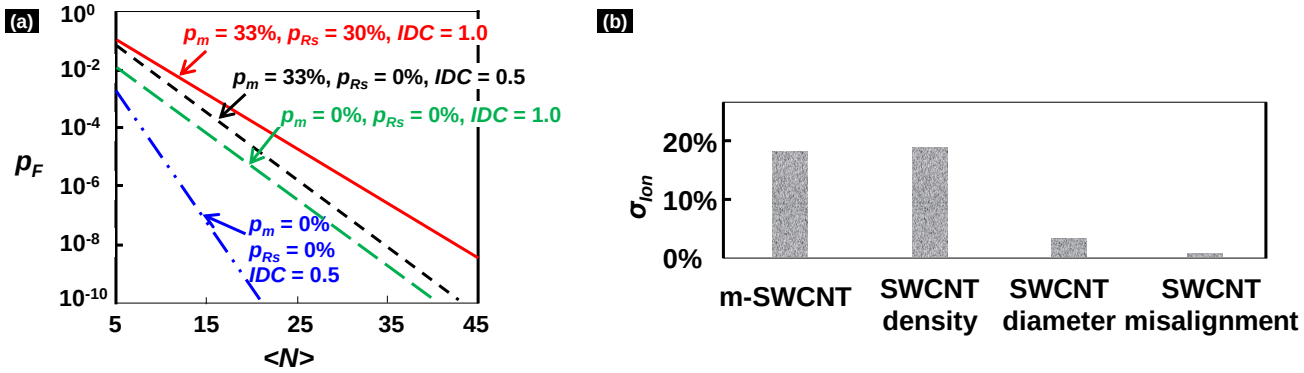
Figure 8. (**a**) Treatment of hexamethyldisilazane (HMDS) for 24 h narrows the V_t distribution significantly. V_g was swept from −2 V to 2 V for p-type, solution-processed s-SWCNT FETs during this measurement. Measured (**b**) G_m distribution and (**c**) diameter distribution for similar solution-processed, s-SWCNT FETs that has small channel length (L_{ch} = 150 nm). (**d**) Extracted contact resistance (R_c) distribution for L_{ch} = 150 nm, solution-processed s-SWCNT FETs. (**e**) Transfer characteristics and (**f**) G_m distribution for solution-processed, m-SWCNT FETs. (**a**–**c**) and (**d**–**f**) are reprinted with permission from Refs. [28] and [86], respectively; © 2012 American Chemical Society.



We performed a comprehensive experimental and theoretical study on FETs with aligned array SWCNTs [44] and ruled out the presence of statistical averaging in aligned-array SWCNT-FETs. Figure 10a plots distribution of I_{on} (measured at a $V_g - V_t = -1$ V) for aligned array-SWCNT FETs having $<N> \sim 11$ SWCNTs, where $<N> = <\rho>W$ is nominal number of SWCNT within the FET, W is the channel width, and $<\rho>$ is the average SWCNT density on the substrate per μm across the length of the nanotubes. Since variation in I_{on} follows Poisson statistics [44], we account for changes in μ_{Ion} (that arises from variation in sample preparation) from one set of array-SWCNT FET to another by dividing the standard deviation of $I_{on}/<N>$ (σ_{Ion}) with $\sqrt{\mu_{Ion}}$ (where μ_{Ion} is the average of $I_{on}/<N>$). Calculated $\sigma_{Ion}/\sqrt{\mu_{Ion}}$, normalized with respect to the same value measured for FETs with single SWCNT, shows a small reduction with the increase in $<N>$ (Figure 10b). If the diameter and density distributions of SWCNT for each array-SWCNT FETs (sample distribution) were the same as the

wafer-level distribution (population distribution) of these parameters, as per central limit theorem [92], the normalized standard deviation should have reduced as $1/\sqrt{<N>}$ due to statistical averaging. The existence of deviation from $1/\sqrt{<N>}$, therefore, suggests significant variations in SWCNTs' density and diameter across the wafer, as was confirmed via extensive atomic force microscopy (AFM) at different locations over a macroscopic area of ST-cut quartz substrate that had CVD-grown aligned arrays of SWCNTs [44].

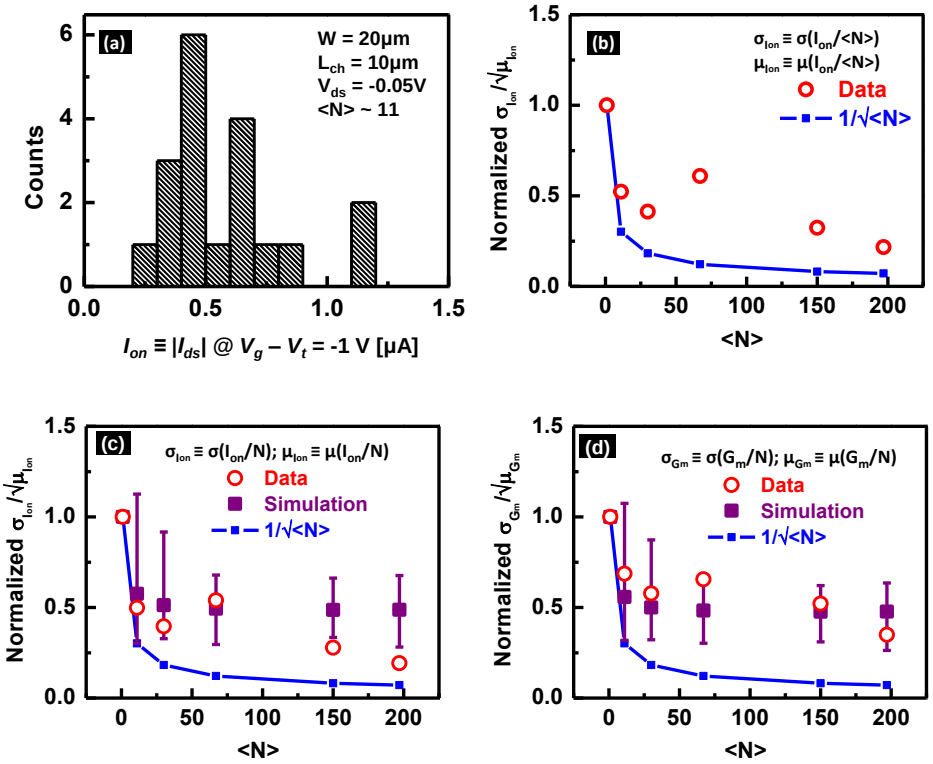
Figure 9. (**a**) Variation in failure probability (p_F; defined as probability of having no s-SWCNT within the FET) of m-SWCNT removed (via post-processing) aligned-array SWCNT-FETs with $<N>$ (defined as the average number of SWCNTs within the FET before post-processing). Simulation is performed for different values of p_m (defined as the probability of having m-SWCNT within the FET before post-processing), p_{Rs} (defined as the probability of s-SWCNT removal via post-processing), and *IDC* (index of dispersion in SWCNT count). (**b**) Different variation sources like the presence of m-SWCNT before post-processing, SWCNTs' density, diameter, and misalignment contributes differently to the overall variation in standard deviation of I_{on} (σ_{Ion}). Simulation suggests that the presence of m-SWCNT and density distribution are the key variability sources in SWCNT FETs. These figures are plotted using data from Ref. [91].



To clarify the differences between measured $\sigma_{Ion}/\sqrt{\mu_{Ion}}$ and expected $1/\sqrt{<N>}$ dependency, measured diameter and density variations across the wafer are used first to calibrate the variations measured at the microscopic level (*i.e.*, electronic properties of single-SWNT-FETs, as discussed in section 3.1). Later, the rules of "inferential statistics" [92] is used to analyze variations at the macroscopic level (*i.e.*, for array SWCNT FETs). Here, density variation is eliminated by counting the number of SWCNTs (N) for each array-SWNT FET and then using $(I_{ds}/N) - V_g$ characteristics for standard deviation calculation. Even after accounting for density variation, calculated σ_{Ion} at different $<N>$ (normalized to its value for $<N> = 1$) shows significant deviation from $1/\sqrt{<N>}$ scaling (Figure 10c). Such deviation suggests SWCNT density variation as a minor contributor to performance variation, thus contradicting the results of Refs. [25,41,91]. Finally, I_{ds}-V_g characteristics of array-SWCNT FETs are simulated for different $<N>$ by considering experimentally calibrated diameter dependence of single-SWCNT FETs's I_{ds}-V_g characteristics (Figure 7a) and measured (wafer-scale) density, diameter distributions of SWCNT. Figure 10c,d show normalized standard deviations of I_{on} (σ_{Ion}) and $G_{m,max}$ (σ_{Gm}), as simulated for different $<N>$ and their comparison to measured quantities. Since the sample

sizes in measuring the standard deviations were small (~17–35), simulated standard deviations show a range of magnitudes for similar sample sizes within which the measured data points fits in. (The simulation framework [44], used for calculating σ_{Ion} and σ_{Gm} of array-SWCNT FETs, neglects contributions from m-SWCNTs. However, the procedure is suitable for demonstrating the importance of wafer-level variations in diameter and density).

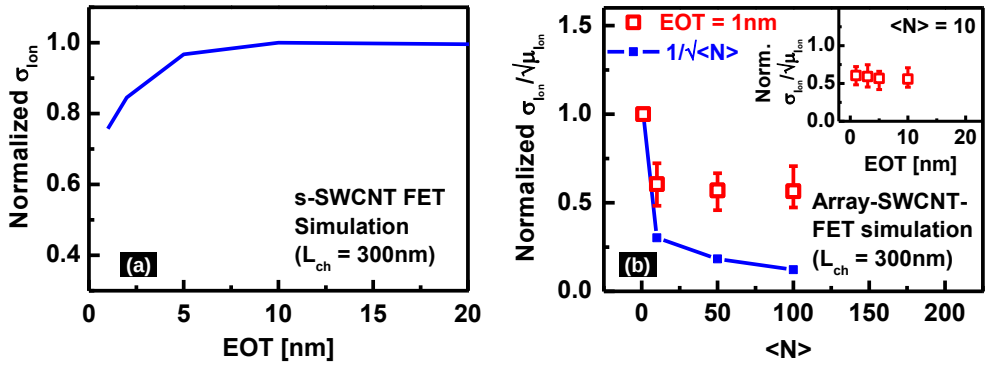
Figure 10. (**a**) Distribution of I_{on} among array-SWCNT FETs with mean SWCNT density $<N>$ ~ 11. (**b**) Normalized standard deviation of I_{on} (σ_{Ion}) *vs.* $<N>$ deviates from $1/\sqrt{<N>}$ scaling or central limit theorem. Normalized (**c**) σ_{Ion} and (**d**) σ_{Gm} for array-SWCNT FETs, where the effect of SWCNT density variation is removed by counting N for each FET and then calculating the standard deviations using I_{ds}/N–V_g characteristics of each FET. Variations in σ_{Ion} and σ_{Gm} still differs from $1/\sqrt{<N>}$ and required the consideration of wafer-scale diameter distribution for matching experimental trends via detailed simulation. Figures are reprinted with permission from Ref. [44]; © 2012, AIP Publishing LLC.



Recently, use of smaller equivalent oxide thickness ($EOT \equiv \varepsilon_{SiO2}/\varepsilon_{HK}T_{ox}$; where ε_{SiO2}, ε_{HK} are dielectric constants of SiO_2 and high-κ dielectrics, respectively) has been shown to reduce the performance variation in FETs with single s-SWCNTs [93]. Decreasing *EOT* reduces the width of the Schottky barrier near the SWCNT and source/drain junction [57] and removes the long negative tails in the I_{on} distribution [44]. Moreover, as L_{ch} approaches the carrier mean-free path of SWCNT, I_{ds} saturates for large diameter SWCNTs and hence diameter dependence of I_{ds} is less pronounced [44]. Both these effects are studied by simulating small-scale array-SWCNT-FETs with *EOT* ~ 1 nm and L_{ch} = 300nm. (Here, simulated I_{ds}-V_g [44] is calibrated with measurements of Ref. [63]). Simulation suggests a decrease in σ_{Ion} for FETs with $<N>$ = 1 with decreasing *EOT* (Figure 11a). However, at larger $<N>$, neither *EOT* nor L_{ch} scaling could improve the statistics because the effects of variations

in density and diameter remain significant (Figure 11b). Therefore, narrowing diameter and density distributions are identified as the main areas for improvement via advanced growth and/or purification techniques to reduce performance variation in multiple-SWCNT FETs.

Figure 11. (**a**) Oxide scaling of s-SWCNT FET reduces σ_{Ion} (normalized by its value at equivalent oxide thickness (*EOT* = 20nm), as observed in Ref. [93]. (**b**) Normalized σ_{Ion} (*i.e.*, $\sigma_{Ion}/\sigma_{Ion,<N>=1}$) differs from $1/\sqrt{<N>}$ scaling for *EOT* = 1 nm array-SWNT FETs and show negligible effect of oxide scaling at fixed <*N*> (inset). Figures are reprinted with permission from Ref. [44]; © 2012, AIP Publishing LLC.



4. Reliability of SWCNT-FETs

Reliability (*i.e.*, device performance degradation) for any device can be interpreted by understanding its origin. For SWCNT-FETs, degradation arises from defects at the interface of SWCNT/oxide and also from defects within the oxide. Trapping and detrapping of carriers (*i.e.*, electrons and holes) into and out of these defects changes performance parameters like V_t, I_{ds}, G_m, *etc.* over time [94–96] and also causes hysteresis in the measured I_{ds}-V_g characteristics [83]. In addition to these interface and oxide defects, performance of SWCNT-FET is also affected by topological or Stone-Wales defects [97,98]. They affect the transport of carriers through SWCNT; hence, they lower the mobility of associated FETs. On the other hand, controlled introduction of defects via UV/ozone/chemical treatment [99], doping [20,100], *etc.* enable the application of SWCNTs as sensors by providing low-energy adsorption sites for introduction of chemical species. These structural defects, however, do not evolve with time during the operation of SWCNT-FET, hence do not affect reliability.

In this section, we discuss the nature of interface (section 4.1) and oxide (section 4.2) defects in SWCNT-FETs and show how these defects raise reliability concerns such as hysteresis (section 4.3), low-frequency noise (section 4.4), radiation damage (section 4.5), and time-dependent performance degradation (section 4.6). These interface and oxide defects though cause reliability concerns at different *quantities* depending on the orientation and density of SWCNTs within the FET, the *qualitative* features of reliability remain the same for any orientation and density, as studied in context of hysteresis and performance degradation in Ref. [94]. Therefore, in contrary to Section 3, where variability of FETs with single and multiple SWCNTs is discussed separately, a general discussion of reliability without reference to SWCNTs' density and orientation within the FET is sufficient for this section.

4.1. Interface Defects in SWCNT-FETs

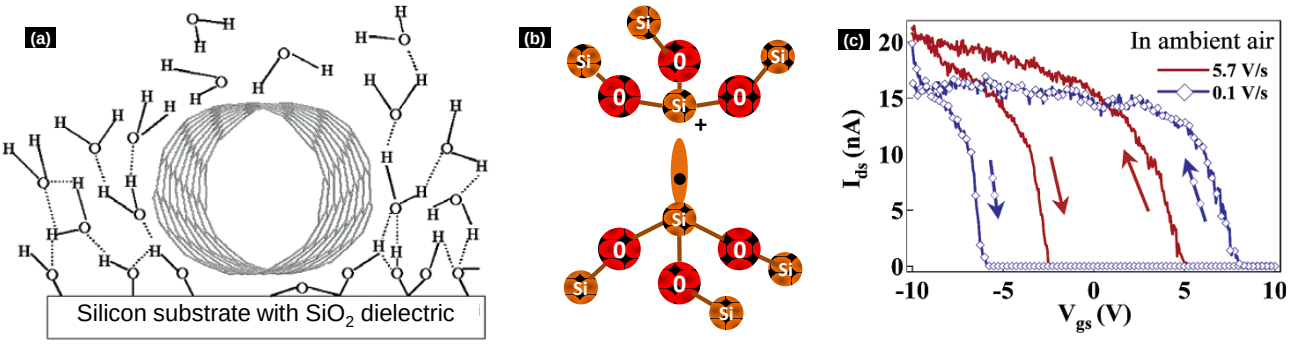
Hydroxyl group (–OH), commonly present at any oxide surface [101,102], is the source of interface defects in SWCNT-FET [83,103,104]. Physisorbed water molecules and oxygen, present at the SWCNT/oxide in ambient condition, control –OH density [102] through electrochemical reaction: $O_2 + 4H^+ + 4e^- \leftrightarrow 2H_2O$ [102,105]. These –OH groups or interface defects surround SWCNTs laying on SiO_2 surface (Figure 12a) and can give rise to large hysteresis in measured I_{ds}-V_g characteristics [83,103,104], as well as potential time-dependent degradation in measured current [95,96]. Application of positive V_{gs} negatively charges –OH groups via electron capture from SWCNT positively shifts V_t and enhances hole conduction in commonly used p-type SWCNT-FET. Application of negative V_g, on the other hand, discharges the –OH group into neutral state, negatively shifts V_t and reduces hole conduction. Marcus-Garischer theory is generally used for modeling charging into or discharging from interface defects in SWCNT-FETs [94,105].

High temperature annealing under vacuum can reduce –OH groups [83,104] by eliminating water molecules at temperatures >190 ℃ [101]. Annealing at even higher temperature (at >1000 ℃ [101]) in vacuum would have completely removed the –OH groups; however, they have never been tested because of the high potential for damage to the SWCNTs and to the characterization system at such high temperatures. In addition to annealing in vacuum, –OH group or interface defects can also be reduced by using poly-methyl methacrylate (PMMA) encapsulation with thermal annealing [83] or by growing SWCNTs on different types of hydrophobic surfaces like octadecyltrichlorosilanated-SiO_2 [103,106], hexamethyldisilazanized-SiO_2 [86], octachlorotrisiloxane-capped organic dielectrics [107], *etc.*

4.2. Oxide Defects in SWCNT-FETs

Defects that are present within the gate dielectric, either near the SWCNTs or deep into the dielectric, also affect device performance. These oxide defects are broken bonds (Figure 12b) and pre-exist within the amorphous oxide network at various quantities, depending on the type of oxidation being performed. These pre-existing oxide defects can be annealed, for example, at high temperatures in hydrogen ambient [108]. Oxide defects are also generated near the vicinity of SWCNT during its growth, unless appropriate measures are taken to reduce the defects by running the growth in an inert environment [94]. In addition to the pre-existing ones, oxide defects are also generated during operation of FETs and causes dielectric breakdown [109–111]. The nature and origin of these oxide defects have been studied extensively using electron paramagnetic resonance [112,113], stress-induced leakage current [109], sweep-rate dependent I_{ds}-V_g hysteresis [94], and optical excitation [114]. Unlike interface defects in SWCNT-FET, oxide defects are ambipolar and can either switch between negative and neutral charged states (*i.e.*, act as electron traps) or switch between positive and neutral charged states (*i.e.*, act as hole traps) [115]—thus, showing a wide range of reliability concerns as discussed below.

Figure 12. (**a**) Schematic representation of hydroxyl (–OH) group present at the surface of silicon dioxide on which SWCNTs are grown or placed. These –OH groups act as interface defect in SWCNT FETs. (**b**) Schematic representation of oxygen-vacancy related oxide defects [113] within silicon dioxide. (**c**) Transfer characteristics of s-SWCNT FET show large hysteresis between V_g sweeps performed in positive to negative and negative to positive directions. Measured hysteresis depends on sweep rate of V_g. (**a**,**c**) are reprinted with permission from Ref. [83]; © 2003 American Chemical Society.

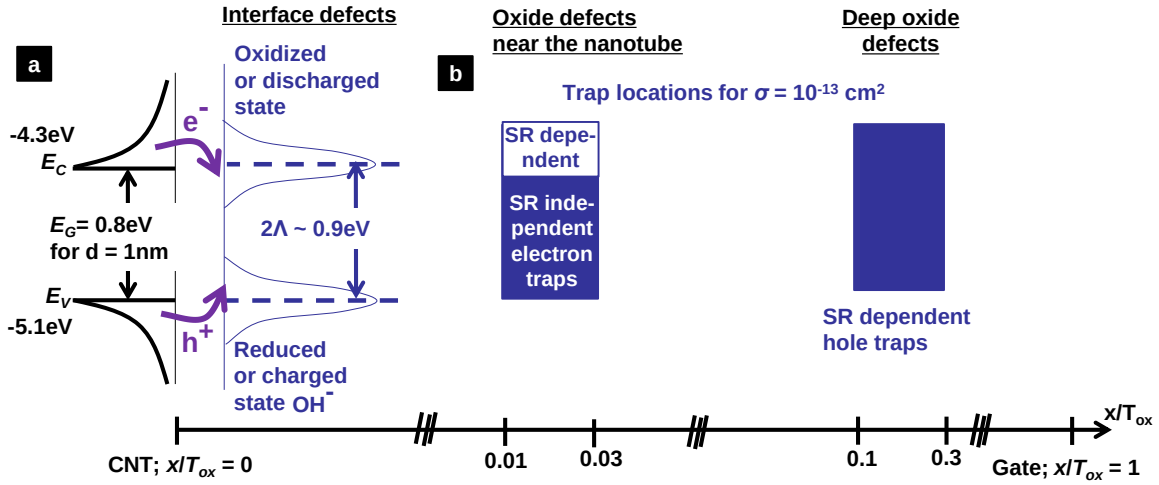


4.3. Hysteresis in SWCNT-FETs

Large hysteresis in I_{ds}-V_g characteristics is a common phenomenon in SWCNT-FET and its magnitude depends on the concentration of defects in the FET [83,94], density of SWCNT [116], and also on the magnitude [94,107,117] and sweep-rate of V_g [83,94] (Figure 12c). Two stable charged and discharged states for the defects and switching between these states by application of appropriate V_g is the origin of hysteresis. Though such hysteresis promises memory applications using SWCNT, it is detrimental for device applications.

As mentioned before, both interface and oxide defects can give rise to hysteresis in SWCNT-FET. According to Marcus-Garischer theory [118], –OH groups or interface defects in SWCNT have separate, broad energy levels for discharged (neutral) and negatively charged state, as shown in Figure 13a. In FETs where interface defects predominantly controls hysteresis, the separation between these neutral and charged energy levels of –OH (known as reorganization energy) controls the magnitude of hysteresis [94]. Charging and discharging of oxide defects, on the other hand, can be modeled within a Shockley-Read-Hall framework [119]. Density and type of oxide defects depend on the oxide quality on which carbon nanomaterials are grown or placed on [94]. In some harsh growth conditions, oxides near the FET channel are damaged and give rise to large amount of near-interface oxide defects that dominate the trends in measured hysteresis. In other optimized conditions, we only have a small amount of bulk oxide defects that controls the hysteresis trends.

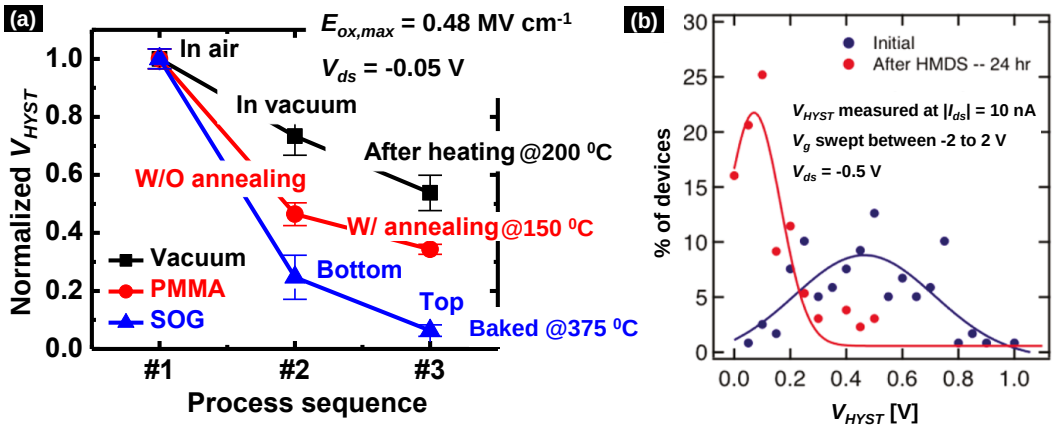
Figure 13. (**a**) Schematic representation of the Marcus-Gerischer theory [118] used to represent the dynamics of –OH group related interface defects to simulate hysteresis in a SWCNT FET with one d = 1 nm s-SWCNT [94]. E_C, E_V, E_G are the conduction band, valence band, bandgap of the s-SWCNT, and Λ is the reorganization energy [105]. (**b**) Representative spatial and energy locations of near-interface electron traps (*i.e.*, oxide defects that switch between negative and neutral charged states) and deep hole traps (*i.e.*, oxide defects that switches between neutral and positive charged states) with $\sigma \sim 10^{-13}$ cm^2 [120] used for simulating oxide-defect related hysteresis in Ref. [94]; © 2012 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.



Self-consistent Poisson and drift-diffusion solution [94], supported by detailed experiments, suggest contrasting sweep rate dependence of hysteresis for different types of defects in SWCNT-FET. Interface defects are characterized by short charge capture and emission times compared to the time used for sweeping V_g to measure hysteresis and, therefore, have sweep rate independent hysteresis. On the other hand, near-interface oxide defect have small capture but comparatively larger emission times, such that hysteresis increases with sweep rate; whereas oxide defects within the bulk of the dielectric have large capture and emission times, such that hysteresis decreases with sweep rate. Measurement of hysteresis at different sweep-rate dependencies, therefore, is used to identify the contributions from different types of defects on hysteresis in SWCNT-FET and modify the fabrication steps appropriately to optimize different defects. Growing SWCNTs in an inert environment reduces the amount of near-interface oxide defects [94] and enables one to employ different interface defect removal techniques to compare their effectiveness. A comparison of different –OH group reduction methods (e.g., heating FETs in vacuum [83], coating SWCNT with PMMA [83] or spin-on-glass [94]; Figure 14a) suggests high temperature annealing, quality of coatings to block water penetration, and reaction of OH-group with coated molecules as the key for reducing hysteresis originating from –OH group related interface defects. All these –OH removal techniques have shown negligible hysteresis when SWCNT-FET is swept with smaller $|V_{g,max}|$. Table 1 summarizes the values of $|V_{g,max}|$ and corresponding maximum of average oxide electric fields ($E_{ox,max}$) that has been reported to show negligible hysteresis under various conditions [9,83,94,103,106,107,121,122]. ($E_{ox,max}$ calculation steps for all the references are shown in the caption of Table 1.) Among these conditions, SWCNT-FETs

with spin-on-glass/HfO_2 gate dielectric shows negligible hysteresis for highest $E_{ox,max}$ ~ 0.45 MV/cm. At higher $|V_{g,max}|$ or $E_{ox,max}$, hysteresis reappears [94,107] which suggests incomplete removal of interface and oxide defects using the techniques mentioned above. Use of combinatorial approaches such as placing SWCNT on hydrophobic surfaces, annealing at temperatures above 400 ℃ in an inert environment, and then coating with hydrophobic gate dielectric may eliminate hysteresis even at higher $E_{ox,max}$. Hysteresis reduction is critical for SWCNT-FET, because reduced hysteresis is generally accompanied with a narrower distribution in V_t (Figure 8a) and also for the hysteresis itself (Figure 14b) [86]. Removal of –OH group from SWCNT-FETs, therefore, is necessary to improve variability in SWCNT-FET.

Figure 14. (**a**) Comparison of effectiveness of different hysteresis reduction techniques like heating in vacuum, use of poly-methyl methacrylate (PMMA) and SOG. Measured hysteresis (V_{HYST}) in each case at similar $E_{ox,max}$ is normalized with that measured in air. For heating in vacuum, hysteresis is first measured in air at room temperature, then after 10 h in vacuum (10^{-5} Torr), and finally after 10 h of heating at 200 ℃ followed by cooling to room temperature in vacuum. For PMMA passivation (with: W/ and without: W/O), hysteresis is first measured in air before PMMA coating, then after PMMA coating and heating for 1min at 110 ℃, and finally after an additional 15 h annealing at 150 ℃. For SOG encapsulation, hysteresis is first measured in air using a bottom-gated configuration, then after SOG encapsulation and 375 ℃ baking using bottom- and top-gated configurations. This figure is taken from Ref. [94]; © 2012 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. (**b**) Use of hysteresis reduction technique like HMDS treatment before placing SWCNTs on oxides is also effective for narrowing distribution of measured hysteresis. This figure is reprinted with permission from Ref. [86]; © 2012 American Chemical Society.



4.4. Low-Frequency Noise in SWCNT-FETs

Low-frequency noise measurement is a general way of characterizing deformations or defects in any nanoscale systems [123–127]. It is also a reliability concern for flash memories [128,129], radio-frequency (RF) circuits [130], and, in general, for many different digital and analog applications employing nanoscale FETs. Among different components of low-frequency noise, the following

components are routinely measured: (i) the frequency independent thermal noise component with power spectral density of $4k_BTR$, which originates from the statistical Brownian motion of carriers at temperature T in a resistive system with resistance R; (ii) the Lorenzian-type noise component with power spectral density ~ $1/[1 + (2\pi f\tau)^2]$, which originates from trapping/detrapping events for a small number of deformations or defects with time constant τ and cut-off frequency $f_c = 1/\tau$; and (iii) the flicker noise component with power spectral density ~ $1/f^n$, which originates from a distribution of trapping/detrapping events.

Table 1. Values of *EOT*, SWCNT density (D), capacitance ratio (Ξ) [131], maximum electric field with parallel plate assumption (*i.e.*, SWCNT is presumed to form a dense film), and maximum of the average oxide electric field ($E_{ox,max}$) for reported instances [9,83,94,103,106,107,121,122] of negligible hysteresis in SWCNT-FETs. Here, $\Xi = 4\pi \times EOT/\varepsilon_{SiO2} \times \lambda_0[2/\varepsilon_{SiO2} \times ln[\lambda_0/d \times sinh(2\pi \times EOT/\lambda_0)/\pi] + C_Q^{-1}]$ [131] (where $\lambda_0 = 1000/D$ is the average distance between each SWCNT, $C_Q = 4 \times 10^{-12}$ F/cm is the quantum capacitance [132]), $E_{P,max} = V_{G,max}/EOT$, and $E_{ox,max} = \Xi \times E_{P,max}$.

Reference	EOT [nm]	D [μm^{-1}]	Ξ	$V_{g,max}$ [V]	$E_{P,max}$ [MV cm^{-1}]	$E_{ox,max}$ [MV cm^{-1}]	Type of Dielectric
[9] Cao *et al*., Nature ’08	8.2	~6	0.01	2	2.44	0.02	HfO_2
[106] Weitz *et al*., NL ’07	20.3	5.48	0.16	2	0.98	0.16	Octadecyltrichlorosilanated-SiO_2
[107] Hur *et al*., JACS ’05	6.9	1 (Single CNT)	0.01	1	1.45	0.02	Octachlorotrisiloxane-capped organic dielectric
[83] Kim *et al*., NL’03	500	1 (Single CNT)	0.36	10	0.2	0.07	SiO_2 with PMMA coating
[103] McGill *et al*., APL ’06	100	~3	0.30	2	0.2	0.06	Octadecyltrichlorosilanated-SiO_2
[121] Hu *et al*., Phys. E ’08	200	~3	0.45	10	0.5	0.23	Aminopropyltriethoxysilaned-SiO_2
[131] Kim *et al*., APL ’07	6.5	1 (Single CNT)	0.01	1	1.54	0.02	Al_2O_3
[94] Jin *et al*., AFM ’12	40	~6	0.29	6	1.5	0.45	Spin-on-glass (SOG) + HfO_2

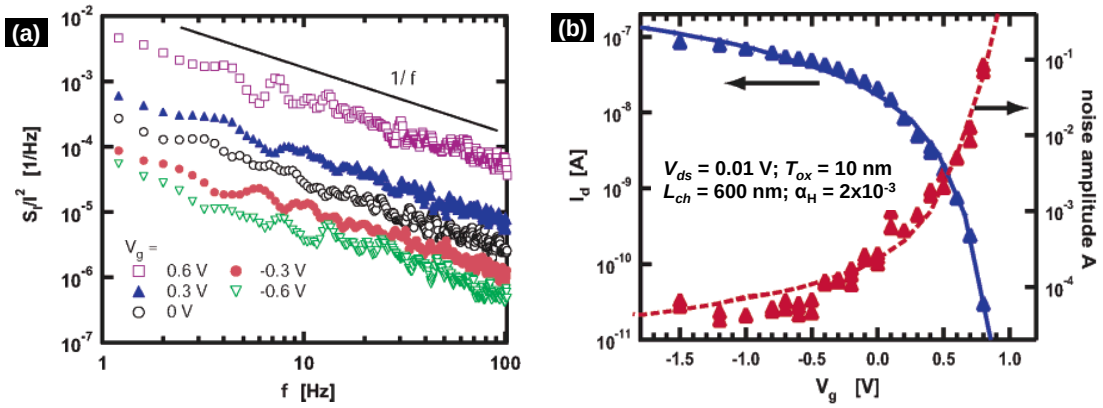
Noise in SWCNT-FETs has been widely studied to understand the origin of deformations or defects in SWCNT lattice and in its surrounding oxides [123–125,128,129], and also to explore the effect of radiation damage [133] and chemical exposure [134]. Measured low-frequency noise in SWCNT is much more pronounced than in silicon electronics [135,136] because of the presence of a few carriers for conduction [134]. In addition to structural defects in the SWCNT lattice [135], oxide defects contribute significantly to low-frequency noise behaviors in SWCNT-FETs [137]. (A recent discussion on different sources of low-frequency noise in SWCNT materials and devices can be found in Ref. [138].) Interface defects interact at faster time-scales and hence noise because interface defects are generally overwhelmed by thermal noise at high frequencies. Oxide defects, on the other hand, have comparatively longer and distributed charging and discharging times (either due to distribution in

tunneling distance [126,127] or due to distribution in defects' energetics [139]) that give rise to *1/f* behavior in the power spectral density of measured noise in I_{ds} at low frequencies [134,135], as shown in Figure 15a, which is measured for a single s-SWCNT-FET at different V_g [134]. From Hooge's number fluctuation theory [140] noise power spectral density (S_I) can be expressed as,

$$S_I = I_{ds}^{\ 2} \frac{A}{f}, \text{ where } A \sim \frac{\alpha_H}{I_{ds}}. \tag{3}$$

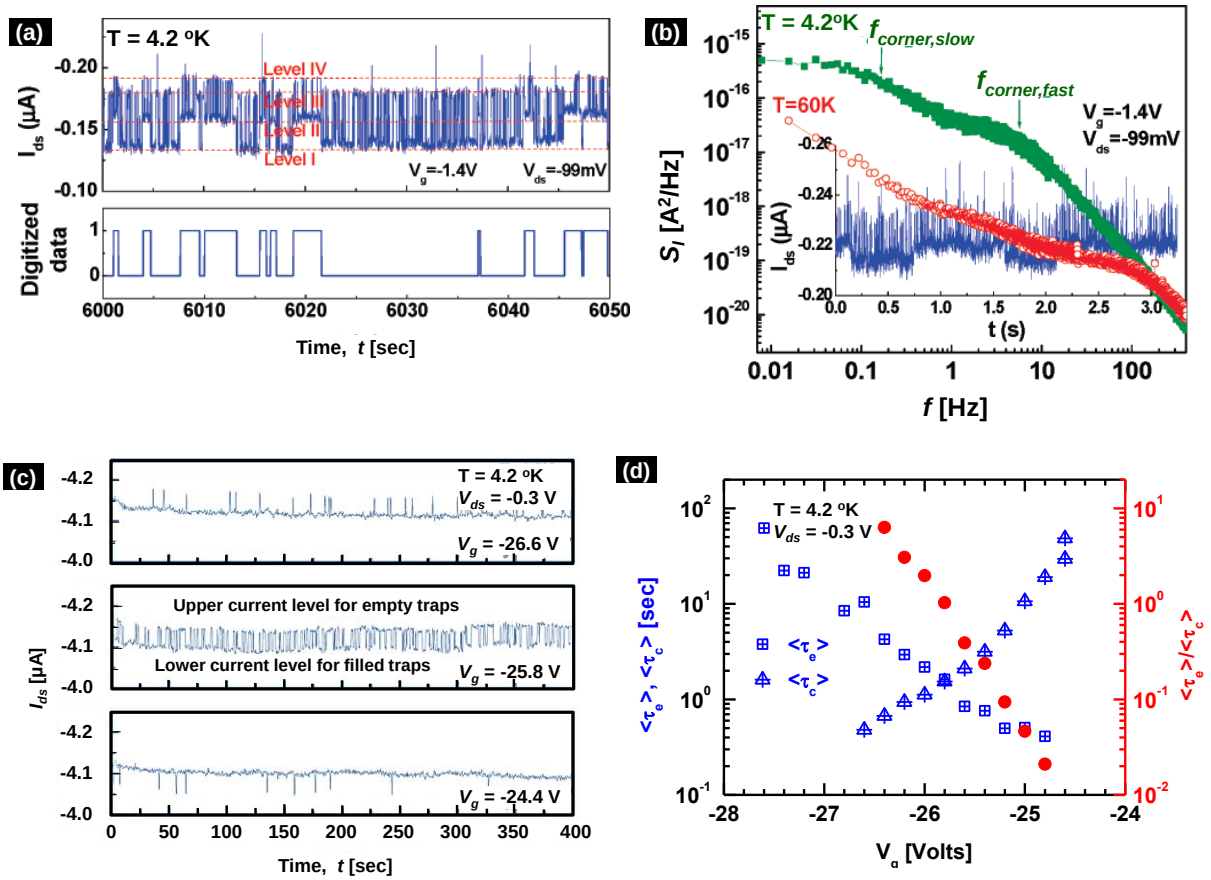
where α_H is a fitting parameter that varies from device to device. Equation (3) suggests a reduction in noise amplitude A with the increase in carrier number or I_{ds}, as measured for the p-type FET for different V_g (Figure 15b) [134].

Figure 15. (**a**) Flicker or 1/*f* noise measured for single s-SWCNT FET at different V_g. (**b**) Increase in V_g decreases I_{ds} and hence increases noise magnitude following Hooge's number fluctuation theory [140]. These figures are reprinted with permission from Ref. [134]; © 2006 American Chemical Society.



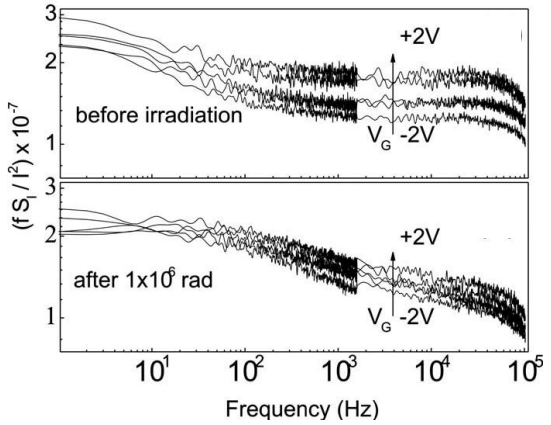
Noise measurements in cryogenic conditions reduce thermal noise and also freeze-off some of the defects that contribute to noise at higher temperatures. Responses from the remaining few oxide defects result in random telegraph noise (RTN) with stochastic variation in I_{ds} and discrete current levels [137,141–143]. Figure 16a shows RTN obtained from a SWNT-FET (measured at T = 4.2 ℃K) suggesting four major switching levels resulting from a slow switching defect (whose fluctuation is digitized in the bottom of Figure 16a) and a fast switching defect [142]. Corresponding power density spectrum for these fluctuations is shown in Figure 16b that suggests two overlapping Lorenzian spectrums with corner frequencies (f_c) at 0.2 Hz (for the slow defect) and 5.8 Hz (for the fast defect). At higher temperatures (T = 60 ℃K), however, responses from these two defects are mixed up (inset of Figure 16b) and noise from new defects (with higher f_c) shows up. Similar noise analysis at different V_g (Figure 16c) enables one to extract distributions of capture time τ_c (defined as the time required for a high to low transition in I_{ds}) and emission time τ_e (defined as the time required for a low to high transition in I_{ds}). These distributions are used to calculate the averages of capture and emission times ($<\tau_c>$ and $<\tau_e>$) at different V_g (Figure 16d) and, hence, the location of defect causing RTN from the slope of $\ln(<\tau_e>/<\tau_c>)$ *vs.* V_g plot [137].

Figure 16. (**a**) Random telegraph noise (RTN) measured in a SWCNT-FET at 4.2 ℃ with $V_g = -1.4$ V and $V_{ds} = -99$ mV shows four major switching levels (red dashed lines) due to the presence of one slow (with larger trapping/detrapping time) and one fast (with smaller trapping/detrapping time) defect. The digitized fluctuation for the slow defect is shown in the bottom graph. (**b**) Noise power spectral density of Figure 16a at 4.2 ℃ and also for the same device at 60 ℃. The inset shows the time domain current data at 60 ℃. Spectral density at 4.2 ℃ shows the cut-off frequencies designating the presence of slow and fast traps. Response from these defects disappears at higher temperatures. (**c**) Low temperature RTN measurements in another SWCNT-FET at different V_g. (**d**) Voltage dependence of average capture $<\tau_c>$, emission $<\tau_e>$ times and their ratios. (**a**,**b**) are reprinted with permission from Ref. [142]; © 2008 American Chemical Society and (**c**,**d**) are replotted using data from Ref. [137].



Though RTN analysis has not yet been employed to study the evolution of defects—*i.e.*, reliability in SWCNT-FETs—*1/f* noise has been used to study the radiation effects in such FETs [133]. An increase in 1/*f* noise after gamma radiation (Figure 17) suggests generation of defects within the oxide. The next section discusses the radiation effects on SWCNT-FETs in detail.

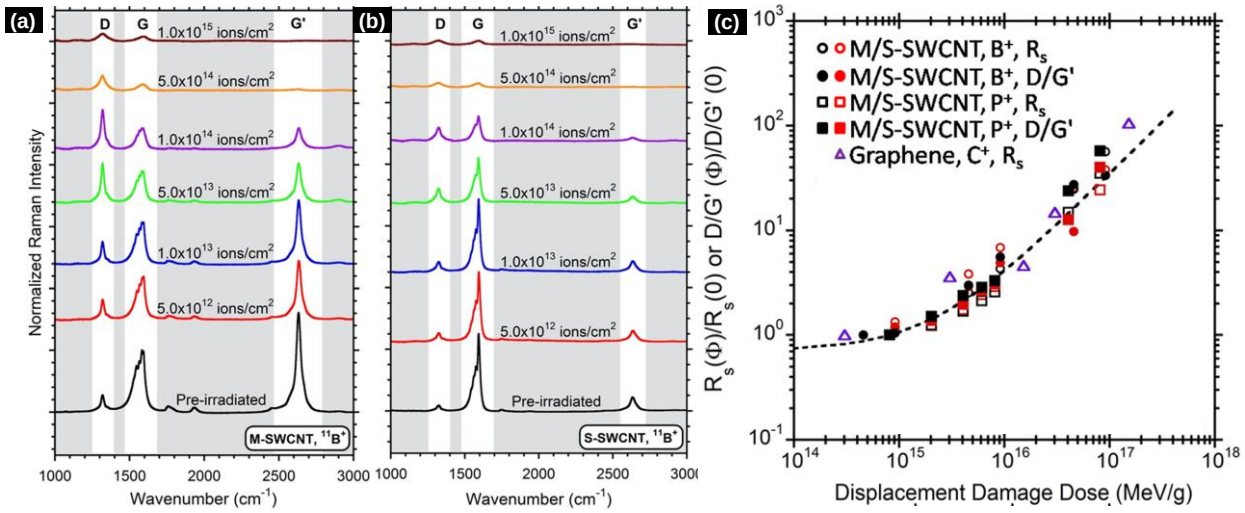
Figure 17. Measured noise power spectral density at different V_g before and after gamma radiation (reprinted with permission from Ref. [133]; © 2010, AIP Publishing LLC).



4.5. Radiation Damage in SWCNT-FETs

Promising performance parameters of SWCNTs have initiated studies to explore their potential in terrestrial and space-based applications [133,144–149]. In such niche applications, radiation tolerance is one of the key reliability parameters. In this regard, use of SWCNT as a channel showed significant advantages over its silicon-based predecessors. Small cross-sections of SWCNT make it less susceptible to incident radiation particles, unless radiation dose (termed as displacement damage dose, DDD) exceeds ~ 10^{13} MeV/g [150]. One can evaluate DDD for different types of particles (e.g., alpha, proton, ionized chemical species) by considering the number of particles striking SWCNTs per unit area (*i.e.*, fluence) and the efficiency of these particles in creating defects within the SWCNT lattice (which is quantified using the term non-ionizing energy loss [150]). Damage in SWCNT at high radiation dose (with DDD > 10^{13} MeV/g) can be monitored using Raman spectroscopy as an increase in intensity at the defect (D)-band wavenumber of ~ 1300 cm^{-1} [133,146–148,151] and also using electrical measurement as an increase in resistance [148,151]. Figure 18a,b show Raman spectra for m- and s-SWCNT-FETs measured at different amount of ionized boron irradiation. Radiation gradually introduces defects within the SWCNT lattice, therefore, increasing the ratio of Raman intensities measured for D- and G^+-bands or for D- and G'-bands. (G^+- Raman signal comes from the atomic vibration of carbon atoms along the axial direction of SWCNT and peaks at a wavenumber of ~1590 cm^{-1} with no diameter dependence. On the other hand, G'- Raman signal arises from a two-photon, inter-valley, second-order Raman scattering process and peaks at a wavenumber of ~2700 cm^{-1} with significant diameter dependence. Both G^+ and G' have no influence from structural defects in SWCNTs. (Dresselhaus *et. al* [152] provide an elaborate review of Raman signal and its origin in different types of SWCNTs.) Ratio of Raman intensities obtained using D- and G'-bands (D/G') are shown to be more sensitive in monitoring the effect of radiation that linearly depends on DDD (Figure 18c), when D/G' at a particular amount of radiation (Φ) is normalized to its value measured before radiation (Φ = 0) [148]. The same linear degradation law also holds for the radiation-induced resistance degradation in SWCNT and graphene.

Figure 18. Raman spectra for (**a**) m-SWCNT and (**b**) s-SWCNT thin-films irradiated with 150 keV $^{11}B^{+}$ ion. The pre-irradiated spectrum is given as a reference and the intensity of each irradiated sample is normalized to the G band intensity of the reference. (**c**) Changes in the normalized (with respect to pre-radiated sample) Raman D/G′ ratio and normalized sheet resistance (R_s) with displacement damage dose (DDD) for boron-ion (B^{+}) and phosphorous ion (P^{+}) irradiated m-SWCNTs and s-SWCNTs, and carbon-ion (C^{+}) irradiated graphene (Ref. [153]). The dashed line is a linear fit of all D/G' ratio and R_s values. Figures are reprinted with permission from Ref. [148]; © 2012, AIP Publishing LLC.



At radiation doses comparable to aerospace environments (*i.e.*, for DDD<10^{13} MeV/g), only the dielectric layer of SWCNT-FETs are damaged with no damage to the SWCNT lattice [133,146,154]. Radiation in such condition changes V_t of SWCNT-FETs with negligible change in mobility (Figure 19a), therefore, suggests negligible defect formation within the SWCNT. The behavior is also confirmed via Raman spectroscopy (Figure 19b) that shows negligible change in D-band and the radial breathing mode (RBM) Raman signals. (RBM signal comes from the atomic vibration of carbon atoms along the radial of SWCNT and has peaks at wavenumbers in the range of ~100–400 cm^{-1} with strong diameter dependence [152].) A decrease in V_t with increasing radiation for the p-type SWCNT-FET (Figure 19a) suggests creation of oxide defects that act as hole trapping sites. The situation improves significantly when a comparatively thinner (~23 nm) silicon oxynitride dielectric (grown via plasma-enhanced chemical vapor deposition) replaces the regularly used ~100 nm SiO_2 in making SWCNT-FETs for radiation testing [145]. Pre- and post-radiation I_{ds}-V_g measurements (Figure 20) suggest negligible change in FET parameters above threshold (*i.e.*, V_t and μ_{eff}). Creation of balanced hole and electron trapping sites within the dielectric [155] and use of thin dielectric that allows the escape of trapped charges [156] are presumed to be the origin of such radiation hardness in these devices. The sub-threshold behavior, on the other hand, shows degradation when the devices are exposed to a negative gate electric field of −1 MV/cm. The origin of such degradation has been attributed to the formation of electron trapping sites within the oxide or at the interface of SWCNT—which requires detailed future analysis. Overall, SWCNT-FETs with thin dielectric offer great potential for space electronics in the future.

Figure 19. (**a**) Transfer characteristics of an SWCNT-FET measured in vacuum for different doses of Co-60 gamma rays. (**b**) G-band and G'-band Raman spectra of SWCNTs (98% s-SWCNT enriched thin film) within the FET before (pre-) and after (post-) irradiation in vacuum. Inset shows the Raman spectra in the low wavenumber regime that suggests negligible change in radial breathing modes. These figures are replotted using data from Ref. [146].

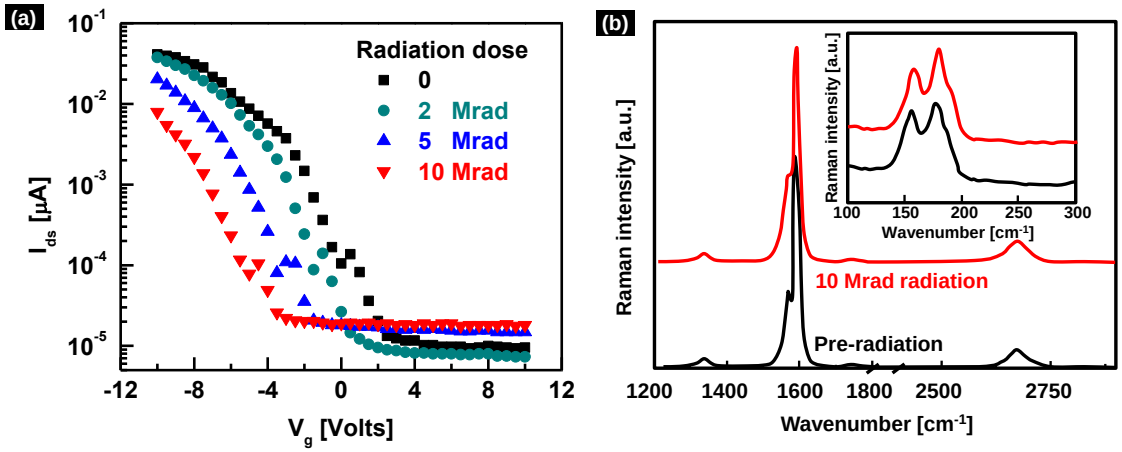
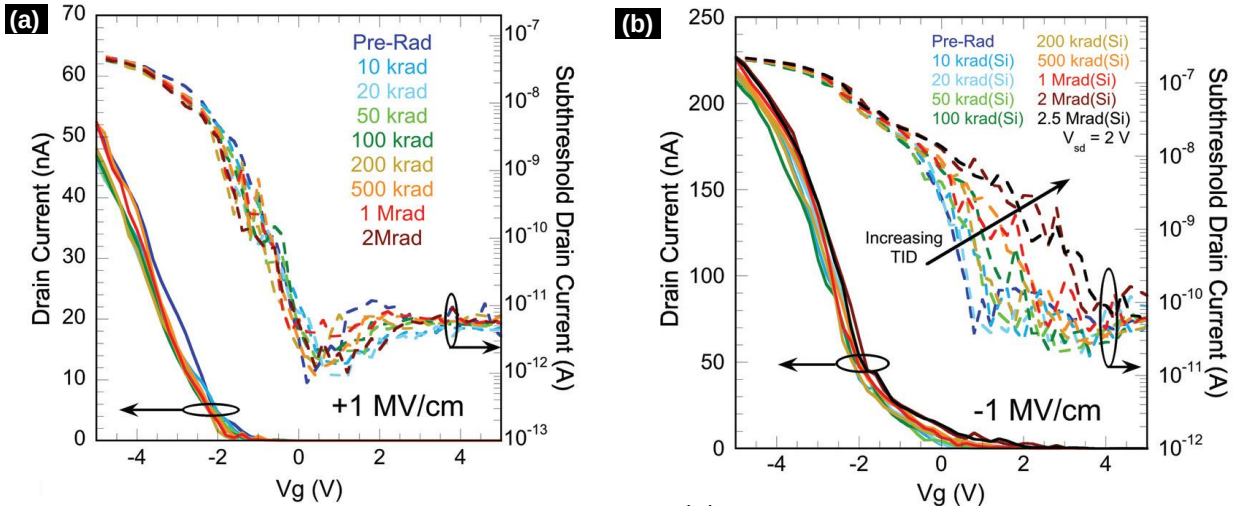


Figure 20. Transfer characteristics of an s-SWCNT FET fabricated with radiation-hard silicon oxynitride gate dielectric. Irradiation is conducted under vacuum with (**a)** positive, and (**b**) negative gate electric field of 1 MV/cm. Figures are reprinted with permission from Ref. [145] © Cambridge University Press 2011.



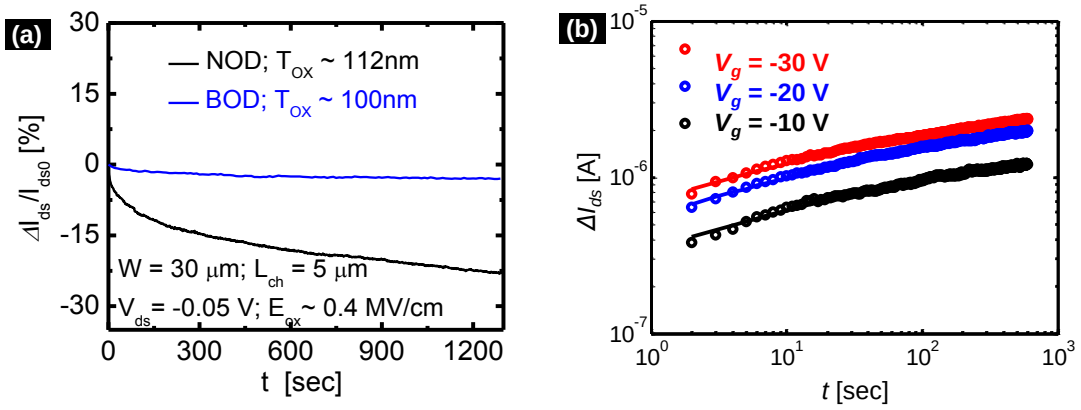
4.6. Performance Degradation in SWCNT-FETs

Performance degradation of transistor parameters over time is a critical reliability concern that dictates the determination of device lifetime. In transistor reliability literature, bias temperature instability [157] and stress-induced leakage current [109] are often used to monitor performance degradation and to probe the dynamics of defects in different regions of the FET. Though hysteresis and low-frequency noise has been widely used to study the nature of defects in SWCNT-FET, detailed analysis of performance degradation over longer time scales is still lacking. Studies of degradation up

to a few seconds [95,96] though provides critical information about the nature of some of the defects, projection of performance degradation up to an intended lifetime of 5–10 years requires accelerated tests (at voltages much higher than use condition) and for longer times (1000 s or more), which are widely used in conventional CMOS reliability studies [157].

Some of the recent long-term performance degradation studies in SWCNT-FETs [94] suggest oxide defect as the key contributor for the instability. SWCNT-FETs with a large amount of near-interface oxide defects show significant I_{ds} degradation (ΔI_{ds}; Figure 21a) and have a small time constant $\tau \sim 7 \times 10^4$ sec for the fitted stretched exponential forms according to $\Delta I_{ds} = I_{ds0}[1 - \exp(-t/\tau)^{\beta}]$ (where I_{ds0} is the magnitude of drain current at $t = 0$, t is the time at which degradation is measured, and τ, $\beta \sim 0.35$ are fitting parameters) [158]. On the other hand, devices with a small amount of bulk oxide defects have lower ΔI_{ds} and long $\tau \sim 2 \times 10^7$ s (with $\beta \sim 0.35$). Moreover, the nature of trapping into oxide defects remains the same at different accelerated stress conditions, as seen from the measured ΔI_{ds} at different gate biases (Figure 21b). All these degradation curves can be fitted with a fixed β and a voltage dependent τ (higher for higher V_g) that suggests more and deeper oxide defects are accessible at higher stress biases. Therefore, by using τ as a voltage dependent parameter, one can project reliability of these SWCNT-FETs at different use conditions. Detailed analysis of such degradation by understanding the trapping dynamics (which may require the use of one or multiple time constants [95]) is still lacking.

Figure 21. (**a**) Percentage change in I_{ds} (ΔI_{ds}) relative to its initial value (I_{ds0}) as a function of time (t) for two SWCNT-FETs, one having a large amount of near-interface oxide defects (NOD) and the other having a small amount of bulk oxide defects (BOD). The figure is taken from Ref. [94]; © 2012 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. (**b**) Drain current degradation measured at different gate stress bias V_g. All the degradation curves can be fitted (lines) using a single expression: $\Delta I_{ds} = I_{ds0}[1 - \exp(-t/\tau)^{\beta}]$ with fixed β and voltage dependent τ (higher for higher V_g).



5. Summary and Outlook

We have discussed different sources of variability and reliability that controls the change in time-zero and time-dependent performance parameters in SWCNT-FETs. Variability in SWCNT FETs performance is mainly attributed to the distributions of SWCNTs' diameter across the wafer and the presence of hydroxyl-group related interface defects in SWCNTs' surroundings. The removal of

m-SWCNTs and the tightening of diameter distribution for s-SWCNTs via chiral-selective growth [159] or post-processing [50,54], and complete passivation of SWCNTs via removal of hydroxyl groups [83,94] are necessary for controlling variability. Removal of hydroxyl groups from SWCNTs' surfaces will also be the key to having a reliable SWCNT FET that will operate with reduced performance degradation over its lifetime. In addition, oxide defects keep playing a dominant role in controlling reliability parameters, like low-frequency noise, radiation damage, and long-term performance degradation. Therefore, solutions in terms of having reliable gate dielectrics with less defects [111,160] will not only help current CMOS scaling, but will also assist with the introduction of beyond CMOS devices with SWCNT-based FET.

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Conflicts of Interest

The authors declare no conflict of interest.

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