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An Ultra-Low-Power 65 nm Single-Tank 24.5-to-29.1 GHz G_m-Enhanced CMOS LC VCO Achieving 195.2 dBc/Hz FoM at 1 MHz

Abdullah Kurtoglu [1,*], Amir H. M. Shirazi [2], Shahriar Mirabbasi [2] and Hossein Miri Lavasani [1,*]

[1] Department of Electrical, Computer, and Systems Engineering, Case Western Reserve University, Cleveland, OH 44106, USA
[2] The Department of Electrical and Computer Engineering, The University of British Columbia, Vancouver, BC V6T 1Z4, Canada; amirms@ece.ubc.ca (A.H.M.S.); shahriar@ece.ubc.ca (S.M.)
* Correspondence: axk1214@case.edu (A.K.); sxm1243@case.edu (H.M.L.); Tel.: +1-216-368-4436 (A.K.)

Abstract: A low-power single-core 24.5-to-29.1 GHz CMOS LC voltage-controlled oscillator (VCO) is presented. The proposed VCO uses an innovative differential cross-coupled architecture in which an additional pair is connected to the main pair to increase the effective transconductance, resulting in lower power consumption and reduced phase noise (PN). The proposed VCO is fabricated in a 1P9M standard CMOS process and sustains oscillation at 29.14 GHz with power consumption as low as 455 µW (650 µA from a 0.7 V supply), which is ~20% lower than a conventional CMOS LC VCO without G_m-enhanced differential pairs built through the same process (700 µA from 0.8 V supply). When consuming 880 µW (1.1 mA from 0.8 V), the proposed VCO exhibits a tuning range of 4.6 GHz (from 24.5 GHz to 29.1 GHz). Moreover, it exhibits a measured phase noise (PN) better than −106.5 dBc/Hz @ 1 MHz and −132.0 dBc/Hz @ 10 MHz, with figure-of-merit (FoM) results of 195.2 dBc/Hz and 200.3 dBc/Hz, respectively.

Keywords: low power; g_m-enhanced; voltage-controlled oscillator; 5G; Ka-band; mm-wave

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1. Introduction

The demand for faster wireless communication is growing exponentially across the globe, requiring larger allocated spectrums for a user. However, the successful implementation of this technique is becoming increasingly difficult in a highly congested sub-6 GHz spectrum, necessitating wireless transceivers operating at higher frequencies, particularly in the millimeter wave (mm-Wave) [1,2]. High performance voltage-controlled oscillators (VCOs) are critical components of any advanced mm-Wave wireless communication transceiver [3–5]. With the never-ending push to conserve energy, VCO power consumption should be minimized. CMOS technology is commonly used for radio frequency integrated circuit (RFIC) designs due to its simplicity, low cost, reliability, and ease of integration with the digital circuits [3,6,7]. Despite these benefits, the functionality and performance of circuits built using CMOS technology is negatively affected as the frequency increases, forcing the designers to increase the power consumption to achieve the desired performance, especially at mm-Wave frequencies [6,8]. Therefore, designing low power mm-Wave VCOs in CMOS technology is very challenging. While advanced non-planar CMOS fabrication technologies (such as FinFET) help to reduce the power [9], the cost is very high for many low-power-consuming applications. Even then, the power savings achieved by using these advanced nodes is usually insufficient for emerging technologies such as 5G new radio (NR) where mm-Wave operation is desired, requiring modifications to the VCO design or topology. Low-power LC VCO designs typically call for maximizing the inductance of the LC tank as well as minimizing the output amplitude [10]. However, these goals are not easily achievable due to the deterioration in the transistor performance

and the increased substrate at mm-Wave frequencies [11]. A few innovative topologies, which mostly focus on improving the quality factor (Q) of the LC tank, are used to create high-performance mm-Wave CMOS LC VCOs suitable for 5G applications [12–15]. The Q of the LC tank relies heavily on the quality of the metallic layers available in the technology, as well as the substrate loss [16]. To tolerate degradations of the implementation technology, especially CMOS, new approaches and design techniques are demanded. For example, researchers have used implicit common-mode resonance [12], the transformer coupling of varactors [13], transformer feedback [14], and Resistor–Inductor–Capacitor Mutual Inductance [15] to improve the phase noise performance. However, these techniques result in higher power consumption, larger on-chip area, and reduced tuning range (TR). Alternatively, the designers can focus on the VCO core to arrive at a lower-power solution. In this approach, the VCO core is modified such that the required negative resistance needed to sustain the oscillation is generated at a lower power consumption, e.g., by boosting the transconductance (G_m) of the cross-coupled pair.

To lower the power consumption of mm-Wave VCOs in widely accessible planar CMOS processes with minimal penalty on PN, area, and TR, the conventional cross-coupled topology should be enhanced/modified. To achieve this goal, innovative topology which takes advantage of undesired intrinsic parasitics of a device is used to generate larger effective G_m at mm-Wave frequencies, thereby presenting a similar negative resistance to the LC tank and sustaining the oscillation at lower power consumption (Figure 1). The proposed G_m-enhanced architecture utilizes an auxiliary cross-coupled CMOS pair which is connected to the main cross-coupled pair in such way as to increase its effective G_m at high frequencies. Considering the high frequency small signal model (SSM) of a MOS device, the signal coupling to the auxiliary devices through parasitic capacitances such as the C_{gd} can be substantial at mm-Wave frequencies, presenting a larger negative resistance to the tank, and could potentially allow for lower overall power consumption [7,17]. For the first prototype, this paper presents a novel low-power 24-to-29.2 GHz LC VCO which uses G_m-enhanced cross-coupled CMOS pairs to reduce the power consumption and improve the PN performance with minimal impact on the TR (Figure 1a). The remainder of this paper is structured as follows: Section 2 briefly introduces the G_m enhancement concept and provides more details about the design of the proposed low-power G_m-enhanced CMOS LC VCO. The VCO measurement results are presented in Section 3 and compared with the simulation as well as the state-of-the-art LC VCOs in a similar frequency range. Section 4 provides the concluding remarks.

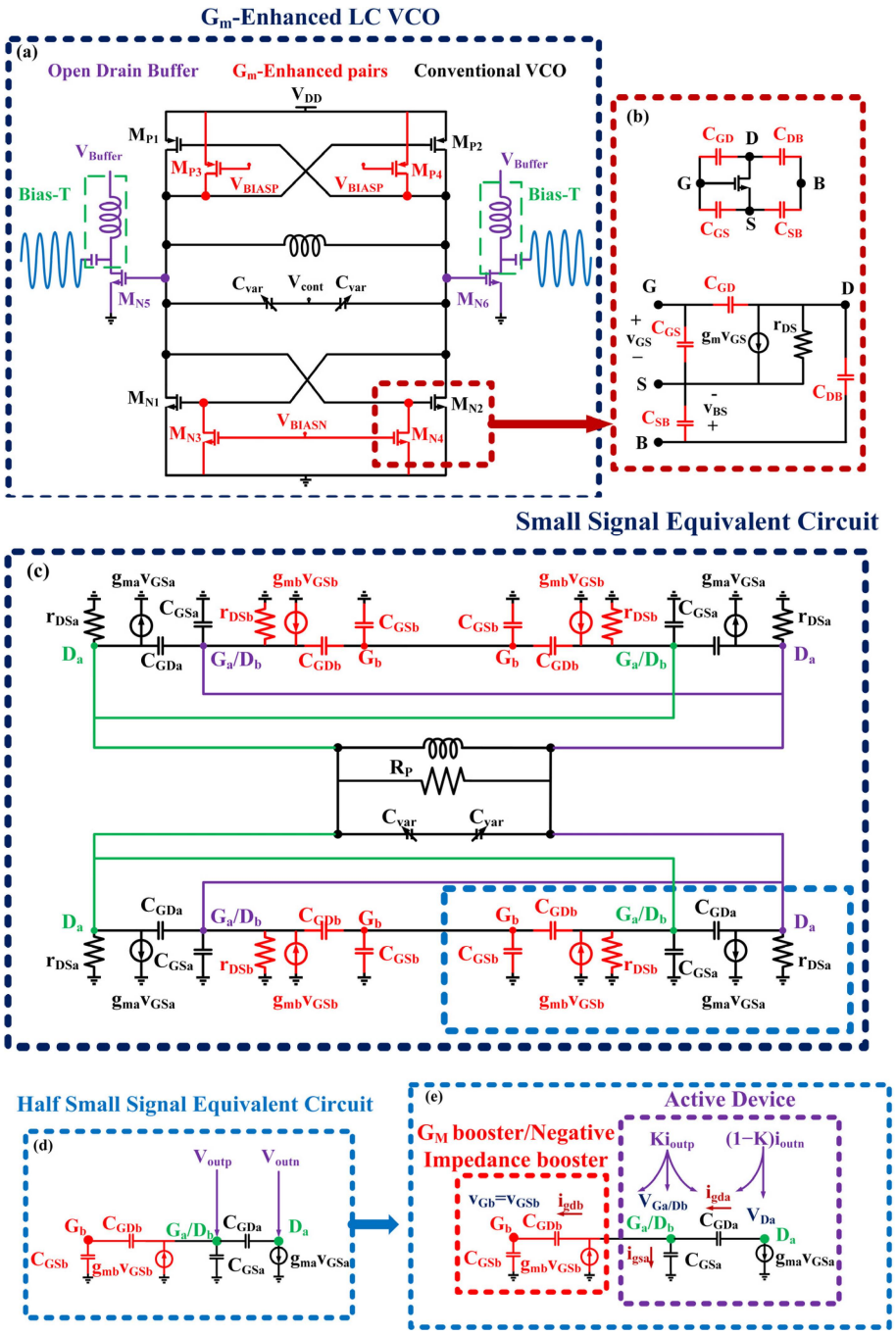

Figure 1. Schematic diagram of (**a**) the proposed G_m-enhanced CMOS LC VCO, along with the small-signal equivalent circuit (SSEC) models of the (**b**) MOSFET [7,17] and (**c**) proposed VCO. The simplified half-circuit models used for (**d**) the effective G_m and (**e**) negative impedance calculation are also shown.

2. G_M-Enhanced LC VCO Design

The proposed G_m-enhanced LC VCO uses a complimentary (i.e., CMOS) cross-coupled topology without a tail current source to maximize the output swing as shown in Figure 1a. A conventional CMOS LC VCO (CVCO) is also implemented in the same technology and characterized for performance comparison with the proposed G_m-enhanced CMOS LC VCO. Figure 1a shows the schematic of both VCOs with highlights showing their differences. Both designs use open drain buffers to interface with the measurement equipment. The power consumption, PN, and TR of an LC VCO rely heavily on the g_m of CMOS pairs

because the g_m of NMOS and PMOS cross-coupled pairs must satisfy the start-up condition of LC VCO designs, as shown below:

$$G_m \geq \frac{1}{R_P}, \tag{1}$$

where R_P is the equivalent parallel resistance of the LC tank used in the VCO, and G_m is the total transconductance of the VCO core. To save power, the G_m is usually set to a minimum needed to start and sustain the oscillation. Minimizing G_m is also important in lowering the PN, since the device noise (particularly the flicker) is directly impacted by the device g_m [6,8,10,18–20]. In fact, Hajimiri et al. [20] have shown that a lower PN requires lower g_m from active devices due to the effect of flicker noise on the PN at low offset frequencies. High G_m is also problematic for the TR as it necessitates using large devices when the supply voltage is limited, increasing the parasitic capacitance of the tank and further limiting the TR [6,8,10]. Therefore, transistor g_m optimization is critical to ensure optimum VCO performance in both voltage-limited and current-limited designs [18]. In addition to the g_m of NMOS and PMOS cross-coupled pairs, the LC tank plays a key role in the power consumption, PN, and TR performance of an LC VCO, requiring a careful design of tank components, particularly the inductance. On the one hand, increasing the output swing, which directly helps the phase noise, calls for large inductors with the highest quality factor (Q), since the output voltage is proportional to $Q_{tank} \times L_{tank} \times \omega_{osc}$. On the other hand, the PN is proportional to $(L_{tank})^2$ [18], suggesting that a low inductance is preferred. The Q variations across the TR should be considered as well, and minimized to limit the PN deterioration across the TR, favouring small inductors at mm-Wave. Moreover, TR is inversely proportional to the L_{tank}, further incentivizing the use of a small inductor in the tank. Hence, a careful trade-off between the inductance and capacitance of the tank is performed for both VCOs. To further increase the inductor Q and save chip area, the VCOs use differential inductors with a floating center tap [21]. The geometry of planar inductors is optimized by considering optimization methods in the literature [22]. The 410 pH inductor designed for the CVCO exhibits a Q of 15.2 near 28 GHz with 69.2 GHz self-resonance frequency (SRF), while the 350 pH inductor designed for the G_m-enhanced LC VCO shows a Q of 16.8 near 28 GHz with SRF > 80 GHz. Figure 2 shows the Q and inductance of the inductors used in the CVCO and G_m-enhanced VCO tanks.

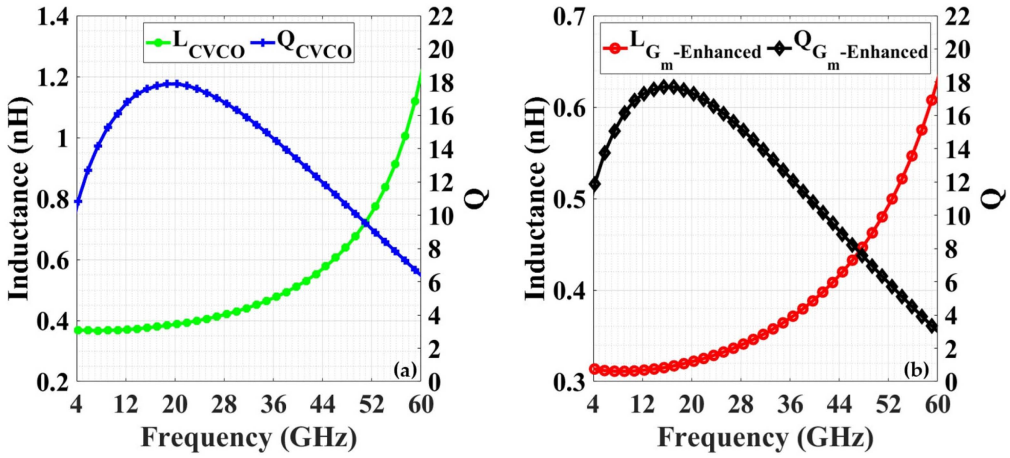

Figure 2. Q and L of inductors used in (**a**) CVCO and (**b**) G_m-enhanced VCO.

In addition to the LC tank, the choice of biasing impacts the power consumption. A popular approach in low-power VCOs is to bias the cross-coupled pair in class C to reduce the VCO power consumption [23]; however, this power reduction comes at the cost of potential start-up failure across process, voltage, and temperature (PVT) corners due to the low gate bias voltage [23,24]. In many cases, the requirements for start-up put stringent limitations on the biasing, preventing maximum oscillation amplitude, and

hence negatively impacting the PN performance. While dynamic biasing may help to solve this problem, it requires auxiliary voltage detection stages [23,24] whose power consumption cannot be ignored in low-power (sub-mW) VCOs. The additional metallic wirings connecting these auxiliary circuits to the main VCO core are also problematic for mm-Wave application as they introduce additional fixed parasitics and limit the TR of the VCO. To avoid these problems, both VCOs presented here avoid class-C biasing.

2.1. Differential G_m-Enhancement Technique

G_m-enhancement (or boosting) techniques are generally categorized into two groups: direct and indirect G_m-enhancement techniques [6–8]. Direct G_m-enhanced techniques utilize additional devices that control the current passing through the devices to increase the total G_m. Examples include adaptive current mirrors [7], negative gain stage [25], and g_m-boosting amplifiers [26,27]. Direct g_m-boosting techniques generally require additional circuitry with active devices to control the current or amplify the signals. On the other hand, indirect G_m-enhanced techniques benefit from the feedback concept, which could consist of only passive devices if desired [8]. There are two main approaches for indirect G_m-enhanced techniques: capacitive coupling and magnetic/inductive coupling [28]. The proposed design employs a hybrid G_m-enhanced structure that aims to share the AC current among multiple devices, at mm-Wave frequencies, to generate larger effective G_m without increasing the power consumption (Figure 1a). The enhanced G_m is then used to generate the required negative resistance needed to sustain the oscillation.

To understand the operation mechanism of the proposed G_m-enhancement technique, a Small Signal Equivalent Circuit (SSEC) of the proposed VCO is developed (Figure 1b,c). Considering the symmetric nature of the design, half-circuit analysis with differential connection is used (Figure 1d). The total current, i_{ds}, is shared between the main devices, i.e., M_{N1} and M_{N2}, and g_m-booster devices, i.e., M_{N3} and M_{N4}. Considering the shared drain (D) and gate (G) connection of these devices, $v_{GSa} = v_{G_a/D_b} = -v_{D_a}$, $v_{GSa} = V_{outp}$, and $v_{D_a} = V_{outn}$ where v_{GSa} is the voltage between G and S of the active device, v_{G_a/D_b} is the voltage at G of the active device or D of the g_m-booster device, and v_{D_a} is the voltage at D of the active device. Then, the equivalent circuit can be simplified to Figure 1e, and analyzed using conventional network theory:

$$(1-K)i_{outn} = (K-1)i_{outp} = i_{gda} + g_{ma}v_{GSa}, \tag{2}$$

$$Ki_{outp} = i_{gdb} - g_{mb}v_{GSb} + i_{gsa} - i_{gda}, \tag{3}$$

$$v_{GSb} = i_{gdb} \times X_{C_{GSb}}, \tag{4}$$

$$v_{G_a/D_b} = v_{GSa} = i_{gsa} \times X_{C_{GSa}}, \tag{5}$$

$$i_{gdb} = \frac{v_{GSa} - v_{GSb}}{X_{C_{GDb}}} = \frac{v_{GSb}}{X_{C_{GSb}}} = \frac{v_{GSa}}{X_{C_{GDb}} + X_{C_{GSb}}}, \tag{6}$$

$$v_{GSb} = v_{GSa} \times \frac{X_{C_{GSb}}}{X_{C_{GDb}} + X_{C_{GSb}}} = v_{GSa} \times X_{eq}, \tag{7}$$

where K is the ratio of the active device current and the total current of the active and the g_m-booster devices, i_{gda} is the current between G and D of the active device, g_{ma} is g_m of the active device, i_{gdb} is the current between G and D of the booster device, g_{mb} is the g_m of the booster device, i_{gsa} is the current between G and S of the active device, $X_{C_{GSb}}$ is the impedance of C_{GS} of the booster device, $X_{C_{GSa}}$ is the impedance of C_{GS} of the active device, $X_{C_{GDb}}$ is the impedance of C_{GD} of the booster device, and X_{eq} is unitless and ~1/3 since C_{GD} is considered ~half of the C_{GS} in strong inversion. To facilitate the design and optimization process, the overdrive voltage (V_{ov}) that is equal to V_{GS}-V_{TH} is set to be roughly the same for both active and g_m-booster devices. The AC currents are defined according to the direction and the device type (active or booster), while the impedances of junction capacitors are defined only based on the device type (active or booster). The

parameter K is defined as the ratio of the g_m-booster current, i_{db}, to the total branch current passing through both drains, i_{dTotal} (Figure 1e):

$$\mathrm{K} = \frac{i_{db}}{i_{dTotal}}, \tag{8}$$

$$i_{dTotal} = i_{outn/outp} = i_{db} + i_{da} \tag{9}$$

where i_{db} and i_{da} are the total AC drain currents of the booster and active devices that share the same drain current, respectively, and they can be expressed as

$$i_{db} = Ki_{outn/outp} = i_{gdb} + g_{mb}v_{GSb} + i_{gsa} - i_{gda}, \tag{10}$$

$$i_{da} = (1-K)Ki_{outn/outp} = g_{ma}v_{GSa} + i_{gda}. \tag{11}$$

From Equations (8)–(11), it is clear that K is a function of the W/L ratio of active and g_m-boosting devices and the frequency, since AC currents are affected by the reactance generated by the devices' parasitic capacitances. Using Equations (2)–(7), Equations (10) and (11) can be further simplified and written in terms of the angular frequency, ω, and device parasitic capacitances. K is heavily dependent on the i_{gdb} since it generates the v_{GSb} needed for the g_m-booster device, as shown in Equation (6). i_{gsa}, i_{gda}, and i_{gdb} can be expressed as follows:

$$i_{gda} = 2j\omega v_{GSa}C_{GDa}, \tag{12}$$

$$i_{gsa} = j\omega v_{GSa}C_{GSa}, \tag{13}$$

$$i_{gdb} = \frac{j\omega v_{GSa}C_{GSb}C_{GDb}}{C_{GSb}+C_{GDb}}, \tag{14}$$

where C_{GSa} and C_{GDa} are the gate-source and gate-drain capacitances of the active device and C_{GSb} and C_{GDb} are the gate-source and gate-drain capacitances of the g_m-booster device, respectively. Assuming C_{GSa}~$2C_{GDa}$ in strong inversion, Equations (10) and (11) can be rearranged as:

$$i_{db} = i_{gdb} + g_{mb}i_{gdb}X_{C_{GSb}} = i_{gdb}\left(1 + \frac{g_{mb}}{j\omega C_{GSb}}\right), \tag{15}$$

$$i_{da} = g_{ma}v_{GSa} + 2j\omega v_{GSa}C_{GDa}. \tag{16}$$

i_{gdb} is directly proportional to the frequency, resulting in K~0 at very low frequencies due to the very small AC current flowing through the C_{GDb}. Choosing proper gate biasing for the g_m-booster device and ignoring the channel-length modulation, K can be rewritten based on critical device parameters:

$$\mathrm{K} = \frac{i_{gdb}\left(1 + \frac{g_{mb}}{j\omega C_{GSb}}\right)}{i_{gdb}\left(1 + \frac{g_{mb}}{j\omega C_{GSb}}\right) + g_{ma}v_{GSa} + 2j\omega v_{GSa}C_{GDa}}. \tag{17}$$

From Equation (14), it is clear that $i_{gdb} \to 0$ when $\omega \to 0$, leading to $K \to 0$. Equation (17) also shows that K is maximized at very high frequency when the reactance of the C_{GS} and C_{GD} capacitances of the device are made very small and create shorting. At such high frequencies, the maximum value for K (K_{max}) can be found as the ratio of the parasitic capacitances of the active and g_m-boosting devices, which is representative of the W/L ratio:

$$K_{max} = \frac{1}{1 + (2C_{GDa}/C_{Ts})}, \tag{18}$$

where $C_{Ts} = \frac{C_{GSb}C_{GDb}}{C_{GSb}+C_{GDb}}$. As evident in Equations (8)–(17), the critical user-defined parameter in the design of the proposed g_m-boosting pair is K since it determines the current sharing ratio between the active and g_m-booster devices.

2.2. Proposed G_m-Enhanced LC VCO Design

To sustain oscillation in a cross-coupled CMOS VCO, the loss in the LC tank should be compensated with the negative resistance produced by the cross-coupled pairs (Figure 1a). As such, the total G_m of a complimentary cross-coupled LC VCO should satisfy the start-up condition shown in Equation (1). In this work, an innovative topology is proposed to increase the effective G_m via g_m-booster pairs (Figure 1a), which is then used to generate the required negative resistance to sustain the oscillation. With the increased G_m, the proposed cross-coupled pair is capable of sustaining oscillation at a lower power consumption with a similar tank, compared to a CVCO. Figure 3 shows the half-circuit equivalent circuit model used to calculate the effective G_m of the proposed VCO. Using Equation (2) through Equation (7), which show the relationship between v_{gs} of the active devices and those of the g_m-boosters, the negative impedance can be found. Since G and D terminals of active and g_m-booster devices are shared, impedances of C_{GSb}, C_{GDb}, and C_{GSa} can be grouped into Z_{eq}:

$$Z_{eq} = \frac{X_{C_{gsa}}\left(X_{C_{gsb}} + X_{C_{gdb}}\right)}{X_{C_{gsa}} + X_{C_{gdb}} + X_{C_{gsb}}}, \tag{19}$$

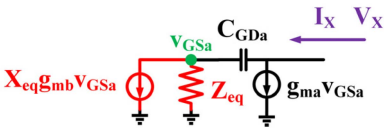

Figure 3. Negative impedance model for the proposed design.

Analyzing the circuit shown in Figure 3, I_X and V_X can be found:

$$V_X = v_{GSa}\left(\frac{1}{Z_{eq}} + \frac{1}{X_{C_{gda}}} + g_{mb}X_{eq}\right), \tag{20}$$

$$I_X = g_{ma}v_{GSa} + \frac{V_X - v_{GSa}}{X_{C_{GDa}}}. \tag{21}$$

Then, the equivalent output impedance, Z_X, can be found as:

$$Z_X = \frac{1 + \left(\frac{Z_{eq}}{X_{C_{GDa}}}\right) + X_{eq}Z_{eq}g_{mb}}{g_{ma}Z_{eq} + X_{C_{GDa}} + Z_{eq} + X_{eq}g_{mb}Z_{eq}X_{C_{GDa}} - Z_{eq}X_{C_{GDa}}}. \tag{22}$$

Once the real and imaginary components of Z_X have been separated and g_{mb} has been expressed in terms of K and g_{ma} using Equation (17), the effective G_m of the proposed design can be approximated as:

$$G_m \cong g_{ma} + g_{mb} \cong g_{ma}\left(1 + \frac{K}{(1-K)}\right) = \frac{g_{ma}}{(1-K)}. \tag{23}$$

From Equation (23), it is clear that the proposed structure produces higher G_m at high frequency when consuming similar power, compared to a conventional cross-coupled pair used in the CVCO. Figure 4 provides a conceptual view of how the required G_m for the oscillation start-up is generated in the proposed VCO compared to the CVCO. As demonstrated in Equation (23), the effective G_m is significantly larger at high frequencies compared to at low frequency. Ideally, the expected K_{max} = 0.5 gives the highest effective G_m when the W/L ratio of the g_m-booster and active devices are equal. Assuming equal length for the devices, $C_{GSa} = C_{GSb}$, $C_{GDa} = C_{GDb}$, and $2C_{GD} \sim C_{GS}$ in strong inversion when $W_a = W_b$. In this case, $K_{max} \sim 0.25$ at high frequency (near the transition frequency, f_T),

resulting in ~33% higher effective G_m. However, the effective K will be smaller for our application where f~30 GHz << f_T (~200 GHz) of the process. Moreover, the width of the g_m-boosting devices is usually chosen to be smaller than those of the width of the active device in low-power design to reduce parasitics and conserve energy. For this design, K~0.2 is chosen, resulting in a maximum G_m enhancement of ~25%.

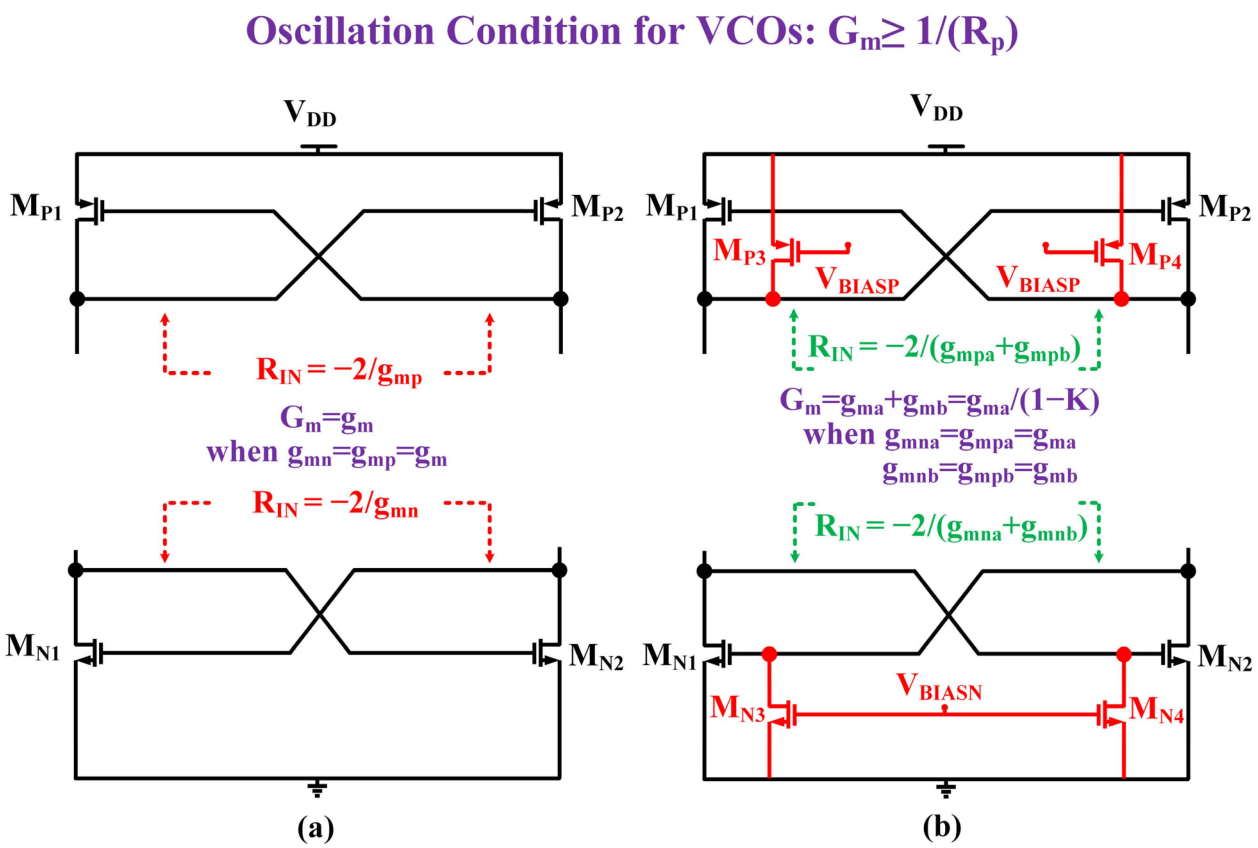

Figure 4. Approximation of the negative resistance and the condition of oscillation for (**a**) CVCO and (**b**) gm-enhanced VCO.

To observe the improvement in the effective G_m compared to the CVCO, several sets of simulations are performed in Cadence and the results are plotted in Figure 5. In these simulations, the impedance of the proposed G_m-enhanced cross-coupled pair (i.e., input impedance) is discovered and compared with those of the standard cross-coupled pair used in the CVCO. Then, the real and imaginary parts of the input impedance are calculated to find the effective G_m in both cases (Figure 5a–c). The estimated G_m calculated from the first-order theoretical analysis given above is also shown in the same plot for the comparison. The effect of frequency on increasing the effective G_m in the proposed G_m-enhanced cross-coupled pair is clearly seen in the plots. For K_{max}~0.2, the proposed G_m-enhanced cross-coupled pair shows a ~19% higher effective G_m at ~30 GHz compared to the standard cross-coupled pair with similar power consumption (Figure 5c). The results exhibit K~0.16 at ~30 GHz for the proposed VCO.

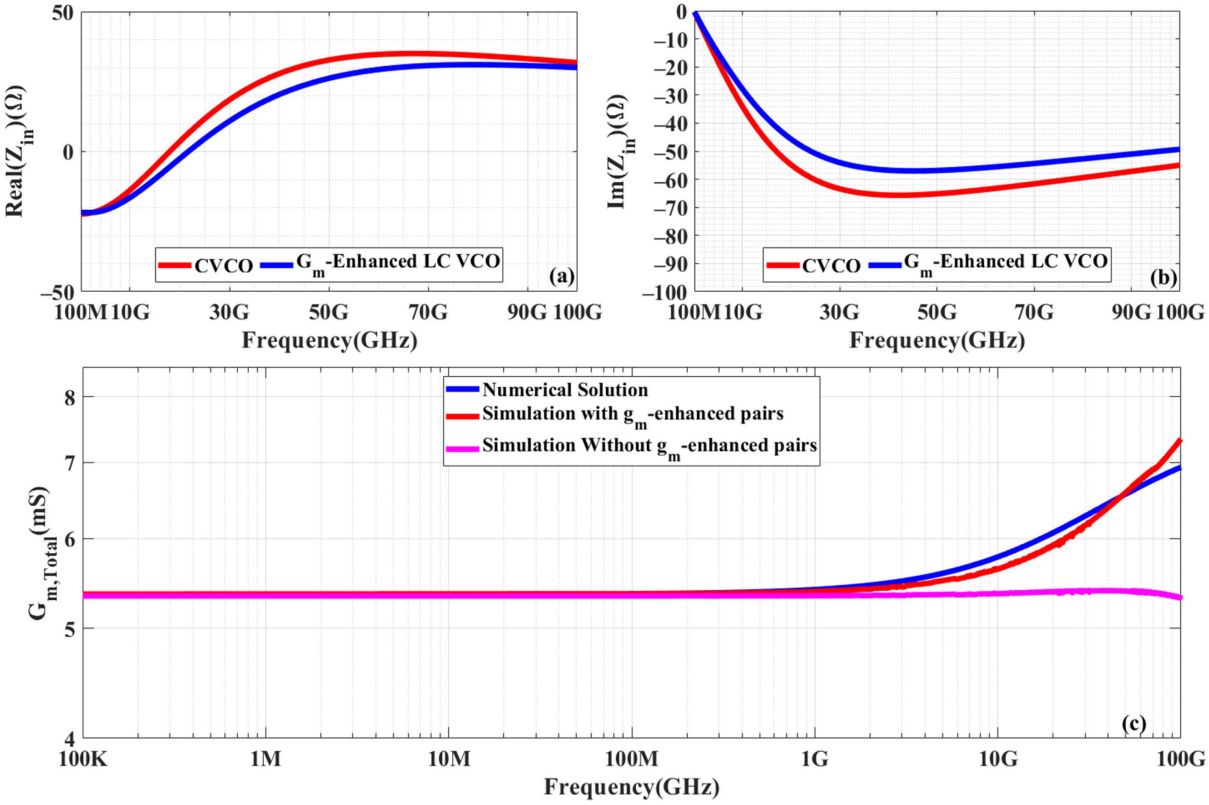

Figure 5. Comparison of the (**a**) real and (**b**) imaginary parts of the input impedance along with (**c**) the effective G_m ($G_{m,Total}$) for the proposed cross-coupled pair with those of the standard cross-coupled pair across the frequency.

3. Characterization Results

The proposed G_m-enhanced VCO is implemented in a 1P9M 65 nm standard CMOS process along with an on-chip open-drain NMOS buffer (connected to GSG pads) used for interfacing with the measurement equipment (Figure 6). A CVCO with a similar inductor design is also included on the same die for performance comparison (Figure 6a). To enable accurate performance measurement for these mm-Wave VCOs, both VCOs are characterized using RF probes with external bias-Ts, facilitating the connection to the supply. This way, the loss associated with external components (such as the cables) can be de-embedded from the measurement results. A general view of the test setup is shown in Figure 6c. Both the G_m-enhanced LC VCO and CVCO dies measure 580 µm × 455 µm. For the proposed design, the VCO core occupies 92 µm × 164 µm (≈0.015 mm^2). The VCO core is slightly larger in the CVCO (due to the larger inductor) and measures 99 µm × 182 µm (≈0.018 mm^2). A Keysight PXA N9030A signal analyzer is used to monitor the output signal and measure the PN performance across the TR. Both VCOs are characterized under similar conditions to allow for accurate comparison. Measurement results show that the proposed G_m-enhanced VCO can sustain oscillation with a power consumption as low as 455 µW (650 µA from 0.7 V supply), while the CVCO burns ≈ 608 µW (760 µA from 0.8 V supply) to sustain the oscillation, clearly showing the power advantage of the proposed VCO. Moreover, the superior PN performance of the G_m-enhanced VCO can be observed when comparing both designs at similar output power ~−11 dBm (Figure 7a). The proposed G_m-enhanced VCO exhibits measured PN performance ~−106.5 dBc/Hz and −132.0 dBc/Hz at 1 MHz and 10 MHz, respectively, @24.5 GHz when the V_{DD} is set to 0.8 V (P_{DC}~880 µW). On the other hand, CVCO achieves a measured PN~−97.1 dBc/Hz and −122.6 dBc/Hz at 1 MHz and 10 MHz, respectively, at a similar frequency (~25 GHz) when the V_{DD} is set to 1 V (P_{DC}~1.5 mW). The PN floor for both designs reaches ~−140 dBc/Hz (Figure 7). The proposed VCO's PN performance

is relatively stable across the tuning range, with negligible deterioration (<2 dBc/Hz) at the upper end of the tuning range. In this case, the PN measures ~−104.7 dBc/Hz and −131.4 dBc/Hz at 1 MHz and 10 MHz, respectively (Figure 7b).

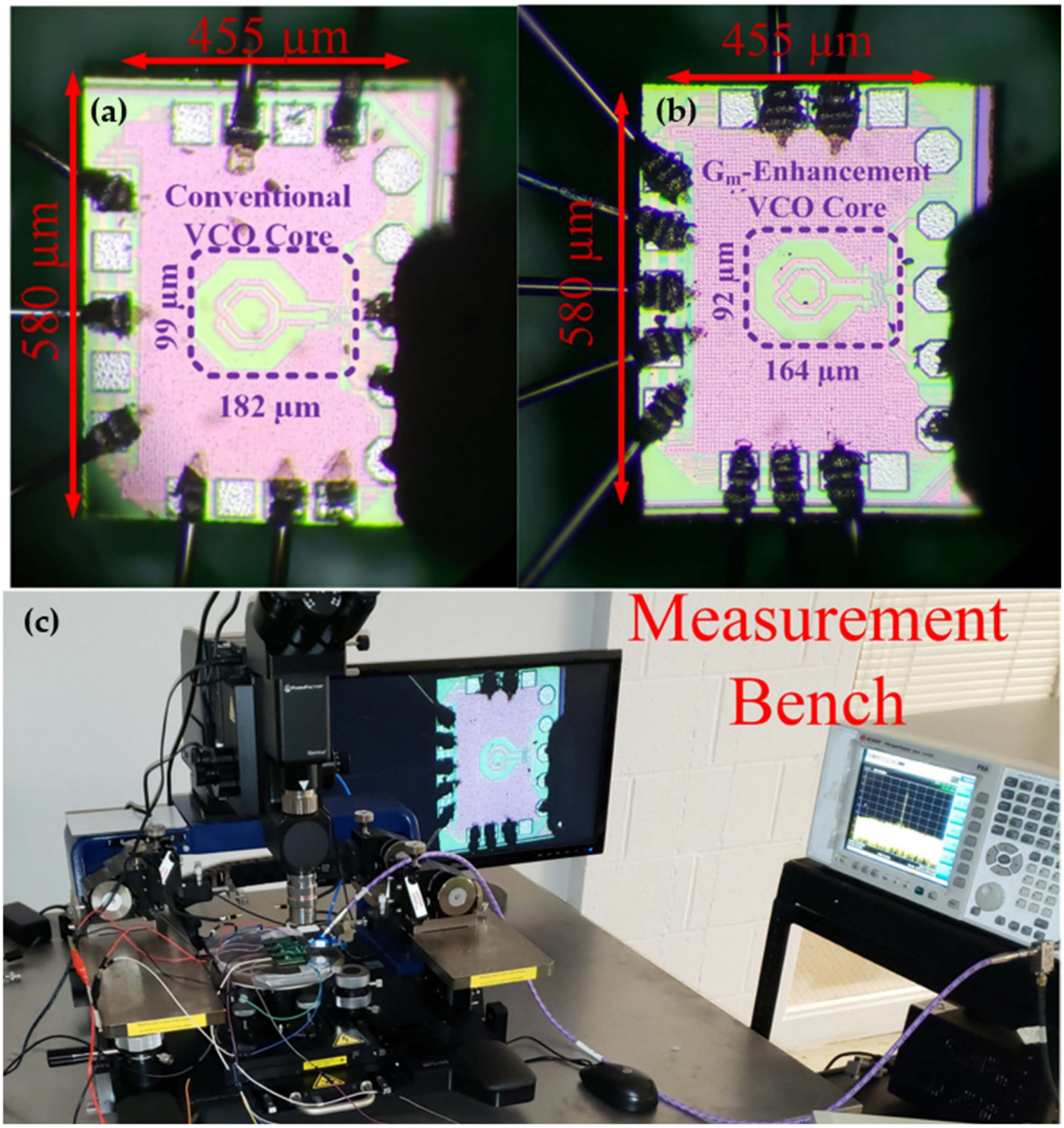

Figure 6. Chip micrograph of CVCO (**a**) and G_m-enhanced VCO (**b**), along with the measurement setup (**c**).

At V_{DD} = 0.8 V (P_{DC}~880 µW), the oscillation frequency changes from ~24.5 GHz to ~29.1 GHz for the G_m-enhanced VCO, demonstrating a TR of 4.6 GHz (~17.8%) (Figure 8). On the other hand, the CVCO oscillation frequency changes from ~25 GHz to ~31.2 GHz at V_{DD} = 1 V (P_{DC}~1.5 mW), demonstrating a TR of 6.2 GHz (~24.5%) (Figure 8). Some PN variations across TR are expected due to the change in the Q of the tank across the frequency range. However, the PN performance is relatively stable (±5 dB) across the TR at 1 MHz and 10 MHz offset. Considering the ~1 GHz shift between the simulated and measured oscillation frequency, the measured PN is also in good agreement with the simulation (Figure 9).

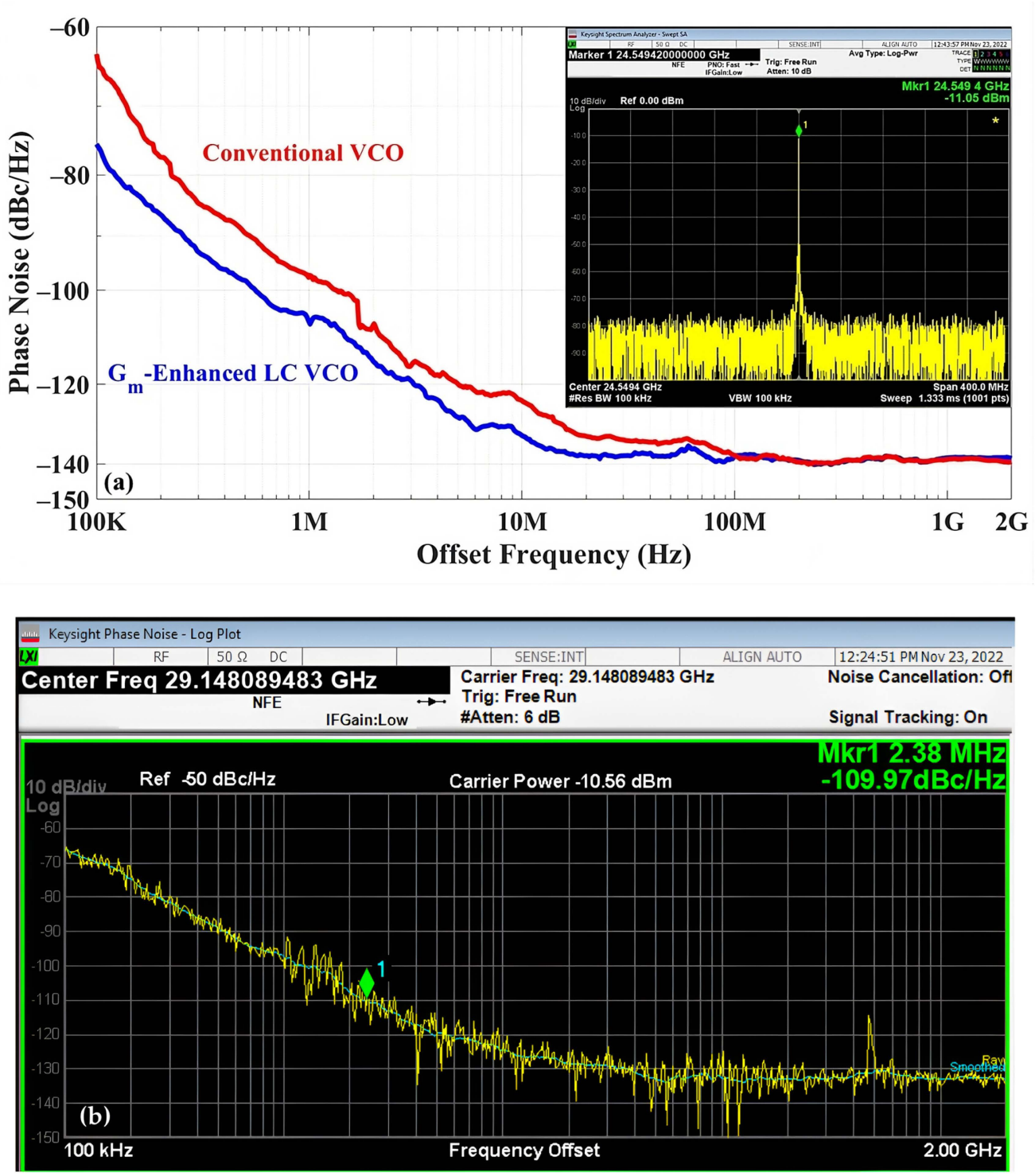

Figure 7. (**a**) The measured PN at the lower end of the tuning range for the Gm-enhanced VCO and CVCO after de-embedding, and the frequency spectrum of the Gm-enhanced VCO, along with (**b**) the measured PN performance of the Gm-enhanced VCO at the upper end of the tuning range before de-embedding.

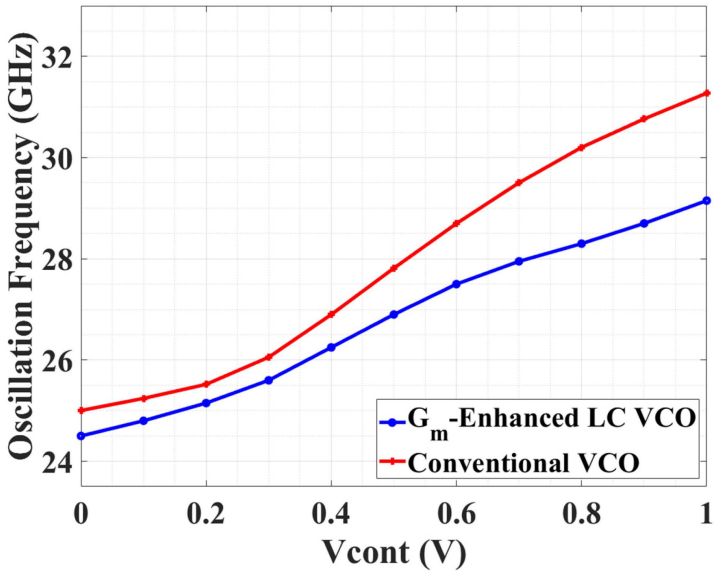

Figure 8. TR performances of CVCO and Gm-enhanced LC VCO.

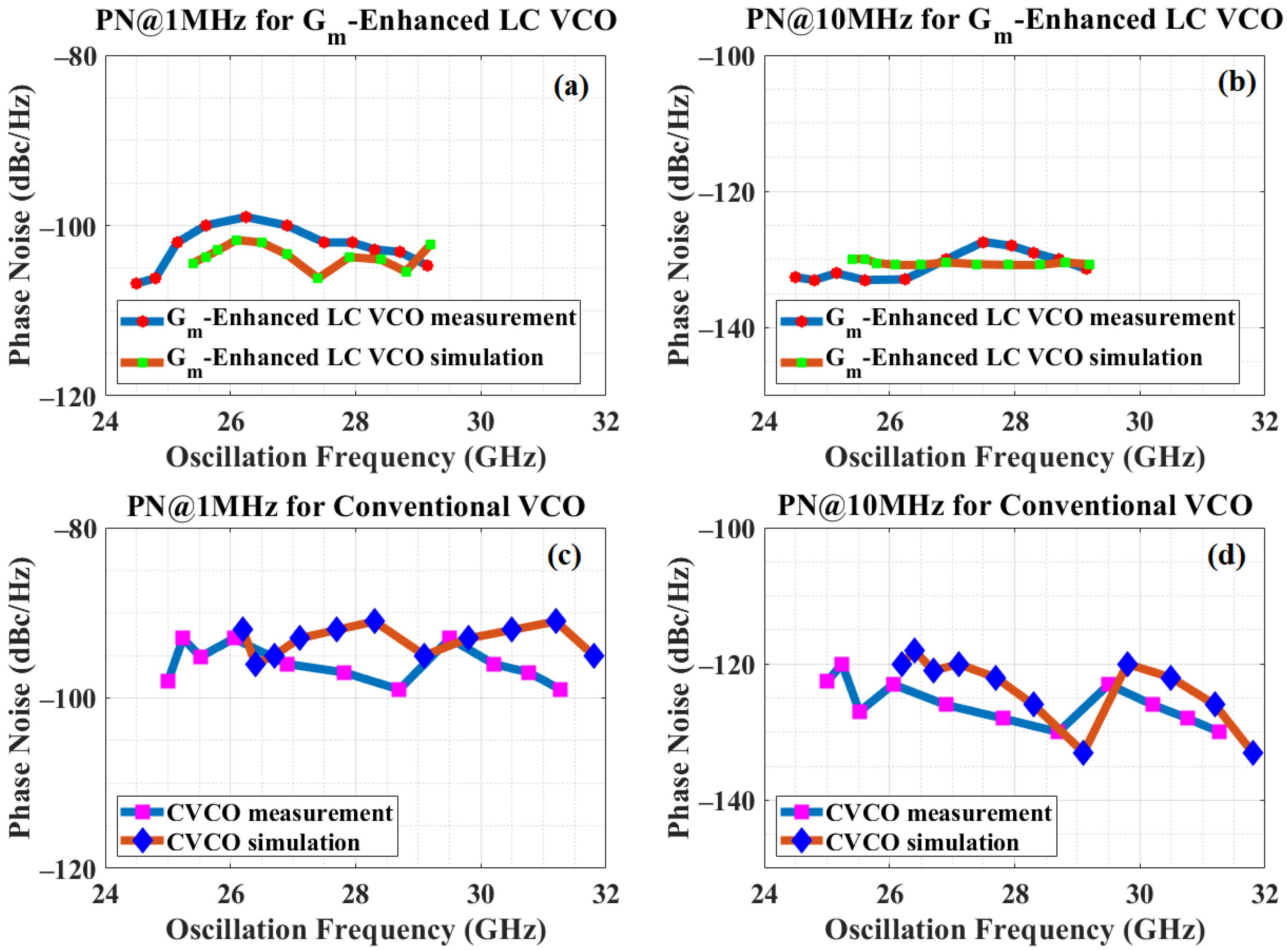

Figure 9. Measured and simulated PN of the Gm-enhanced LC VCO across the TR at (**a**) 1 MHz and (**b**) 10 MHz offset, along with the PN of the CVCO at (**c**) 1 MHz and (**d**) 10 MHz offset frequencies.

The deterioration in the TR of the proposed VCO is due to the extra capacitance resulting from parasitics of additional cross-coupled pairs and additional metal wiring in

the layout. However, the slight closed-in PN improvement (esp. $f_{offset} < 1$ MHz) in the proposed VCO compared to the CVCO requires a more detailed analysis.

Different PN models for LC VCOs are presented in the literature [19,20,29]. The proposed design shows significantly improved PN performance for low offset frequency, with the Flicker noise dominant area with $1/f^3$ slope [19]. As such, Hajimiri's PN model [20] is preferred. Hajimiri's model aims to accurately predict the PN of an LC VCO in the $1/f^3$ and $1/f^2$ regions. For accurate predictions, this model needs impulse sensitivity function (ISF), which is a periodic and dimensionless function. ISF is a periodic function, so Fourier coefficients can be used to represent the ISF function:

$$\Gamma(\omega\tau) = \frac{\Gamma_0}{2} + \sum_{n=1}^{\infty} (\Gamma_n \cos(n\omega_o \tau + \theta_n)), \tag{24}$$

where Γ_0 is the first coefficient of the ISF, and is equal to $2\Gamma_{DC}$, the coefficients (Γ_n) are real values, and θ_n is the phase of the nth harmonic. θ_n is small and can be ignored at random input noise [20], and the coefficients can be estimated analytically or calculated from the simulation. To calculate the coefficients from the simulation, HB and HBnoise simulations of the Cadence Spectre engine provide the perturbation projection vector (PPV) that represents the sensitivity of the per cycle jitter variance to current perturbations at the nodes of the oscillator [29], and can be used to estimate the ISF changes [20,29].

In this work, PPV results can be obtained from the HB and HBnoise simulations (Figure 10). HB PPV results are presented in V and HB noise PPV results are shown in 1/V. Then, the PN model for the $1/f^3$ region can be defined as:

$$L(\Delta\omega)_{1/f^3} = 10 \times \log\left(\frac{\Gamma_0^2}{q_{max}^2} \times \frac{\overline{i_n^2}/\Delta\omega}{8.\Delta\omega^2} \times \frac{\omega_{1/f}}{\Delta\omega}\right), \tag{25}$$

where $\overline{i_n^2}/\Delta f$ is the total noise current, $\overline{i_R^2}/\Delta f + \overline{i_d^2}/\Delta f$. The term $\overline{i_d^2}/\Delta f$ is the power spectral density of the noise of active devices and $\overline{i_R^2}/\Delta f$ is the power spectral density (PSD) of the thermal noise current due to R_p; q_{max} is the maximum charge displacement across the equivalent output capacitance where the impulse was injected, and $\omega_{1/f}$ is $1/f$ corner frequency. At low offset frequencies, the flicker noise of the MOS device will be the dominant component among these two; hence, $\overline{i_n^2}/\Delta f$ can be expressed as $K_F g_m^2/(C_{OX} \cdot W \cdot L \cdot \Delta f)$, where K_F is the flicker noise fitting parameter, C_{OX} is the gate oxide capacitance per unit area, and W and L are the transistor width and length, respectively. Assuming that the thermal and flicker noises are uncorrelated, their impact on the PN can be studied separately:

$$L(\Delta\omega)_{flicker} = 10\log\left(\frac{\Gamma_0^2 \pi K_F g_m^2}{8 q_{max}^2 C_{ox} W \cdot L \Delta\omega^3}\right), \tag{26}$$

$$L(\Delta\omega)_{thermal} = 10\log\left(\frac{kT\pi^2}{I_{DD}^2}\left(\frac{1}{R} + \gamma g_m\right)\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right), \tag{27}$$

where k is the Boltzman constant, T is the temperature in Kelvin, I_{DD} is the RMS current consumption of the VCO, γ is the fitting parameter for the noise of MOSFET, Q is the quality factor of the inductor, and ω_0 is the oscillation frequency, respectively. For a design scenario with a given device size, Q, R, and a fixed current consumption budget, the flicker noise contribution to the PN, shown in Equation (26), can be minimized when the PPV is minimized and q_{max} is maximized. In this work, the simulation results reveal that the proposed G_m-enhanced VCO exhibited significantly smaller PPV compared to the CVCO; the use of HB simulations revealed Γ_0~0.0071 V and 0.0536 V for the differential output of the proposed VCO compared to Γ_0~−0.0533 V and 0.1539 V for the differential outputs of the CVCO. Similarly, Γ_0~0.3707 1/V and −0.2356 1/V was obtained for the differential

outputs of the proposed VCO from the HB noise simulation, while Γ_0~1.2306 1/V and −1.1028 1/V for the differential outputs of the CVCO (Figure 10). The minimum ratio within Γ_0 for the two VCOs is ~2.9×, which amounts to ~9 dB improvement in the close-in PN for the proposed G_m-enhanced VCO. Moreover, the proposed VCO inevitably has larger q_{max} compared to the CVCO due to larger parasitic capacitors from the additional cross-coupled pairs and the resulting on-chip metal wiring. This larger q_{max} further improves the close-in PN performance of the proposed VCO. The measured PN results presented in Figure 7 reveal an up to ~11 dB improvement in the PN at 100 kHz offset for the proposed VCO compared to the CVCO. As the frequency increases, the effect of the flicker noise diminishes, and the thermal noise of active devices and the LC tank parameters (Q and R) become the dominant factors affecting the PN [10,18]. Considering equation (27), it can be seen that the thermal component of the PN is mostly affected by the circuit parameters. Given a similar Q for the tank and the output power, the difference in PN for the two VCOs is primarily determined by the difference in the effective G_m, which is relatively small (~20%). As such, the difference between the PN of two VCOs gradually narrows until it becomes negligible at high offset frequencies near the PN floor.

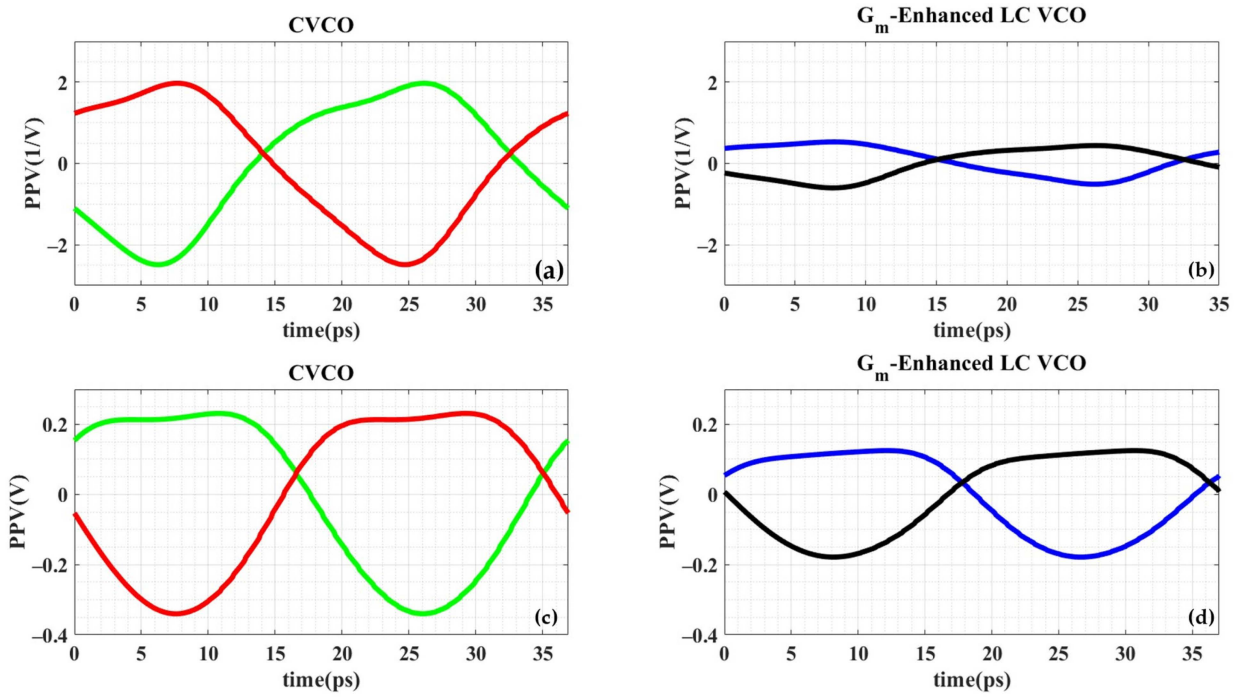

Figure 10. PPV results for differential outputs (green and red for CVCO, blue and black for G_m-enhanced LC VCO): HBnoise results for (**a**) CVCO and (**b**) Gm-enhanced LC VCO; HB results for (**c**) CVCO and (**d**) Gm-enhanced LC VCO.

Figure of merit (FoM) and figure of merit with TR (FoM_T) are important metrics in benchmarking the performance of VCOs. The G_m-enhanced LC VCO measurement results reveal competitive FoM and FoM_T performance. The G_m-enhanced LC VCO shows a FoM of 195.2 dBc/Hz and 200.3 dBc/Hz at 1 MHz and 10 MHz offset, respectively, with a FoM_T reaching 200.4 dBc/Hz and 205.2 dBc/Hz at respective offset frequencies, a significant improvement over those of the CVCO. Compared to the state-of-the-art LC CMOS VCOs [4,12,14,15,30] operating at a similar frequency range and fabricated in a similar process node, the G_m-enhanced LC VCO provides comparable performance while burning less power (Table 1).

Table 1. Summary of the measured performances of the VCOs and comparison with the state-of-the-art mm-Wave CMOS VCOs.

	This Work (CVCO/G_m-Enhanced VCO)	[12]	[14]	[15] *	[4]	[30]
VDD	1/0.8	0.9	0.9	0.48 V	0.95	0.3 V
P_{DC} (mW)	1.5/0.88	3.4	10.8	3.8	16.05	1.4–1.64
f_{osc} (GHz)	25/24.5	27.45	26.5	25.48 (12.74)	25	14.94
Tuning Range (GHz)	25–31.2/24.5–29.1	26.1–29.9	25.7–29.7	25.48–29.92	23–29.9	12.11–14.94
PN@1 MHz (dBc/Hz)	−97.1/−106.5	−105.7	−105.8	−115.27	−110	−105.6
PN@10 MHz (dBc/Hz)	−122.6/−132.0	−127.5	−130	−134	N/A	−131.8
FoM@1 MHz (dBc/Hz)	183.3/195.2	189.15	184	191.6	187	187.6
FoM_T@1 Mz (dBc/Hz)	190.2/200.4	191.7	N/A	195.7	195.3	194.0
FoM@10 MHz (dBc/Hz)	188.8/200.3	191	188	190.3	N/A	193.8
FoM_T@10 Mz (dBc/Hz)	195.7/205.2	193.4	N/A	194.4	N/A	200.2
Core Area (mm^2)	0.018/0.015	0.038	0.022	0.08	0.103	0.153
Technology	65 nm/65 nm	65 nm	65 nm	65 nm	40 nm	40 nm-SOI

FoM = |PN| + 20log10 (fo/Δf) − 10log10 (Pdc/1 mW); FoMTT = FoM + 20log10 (TR/10). *: Measured after on-chip divide-by-2.

4. Conclusions and Future Works

An innovative and compact single-core 24.5 GHz-to-29.1 GHz CMOS LC VCO which employs G_m-boosting cross-coupled pairs is presented. Fabricated using a 1P9M 65 nm standard CMOS process, the proposed VCO consumes lower power compared to a conventional CMOS LC VCO operating at similar frequency with the same output power. The close-in PN performance is also improved for a given power consumption. The performance of the proposed design is also compared against published state-of-the-art CMOS VCOs operating in the similar frequency range, showing competitive FoM and FoM_T while consuming low power and occupying a small silicon area. The proposed G_m-boosting technique can be useful in developing future low-power VCOs used in next generation (6G and beyond) wireless standards where the oscillation frequency is further increased beyond 100 GHz.

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