Article

A New Control for Improving the Power Quality Generated by a Three-Level T-Type Inverter

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Abstract: A new controller based on a fractional-order synergetic controller (FOSC) is proposed for a three-level T-type inverter using a shunt active power filter (SAPF). The SAPF is designed to compensate for the reactive power and eliminate the current harmonics caused by non-linear loads, in cases of distorted or unbalanced source voltages. The proposed FOSC technique with the designed parameters and defined macro-variable is a robust control technique that operates well in both transient and steady-state scenarios, ensuring fast convergence and closed-loop system stability. The FOSC technique utilizes a phase-locked loop (PLL) technique on a self-tuning filter (STF) to enhance the SAPF's ability to compensate current harmonics and reactive power in all situations involving non-linear loads and source voltage variations according to IEEE Std. 519. The proposed control was implemented and verified using Matlab software, where the obtained results were compared with the results of the conventional control based on proportional-integral (PI) controllers in different operating conditions. The results indicate that the proposed FOSC technique outperformed the traditional control in terms of DC voltage tracking and the minimization of the total harmonic distortion of the current.

Keywords: fractional-order synergetic control; phase-locked loop technique; shunt active power filter; self-tuning filter; three level T-type inverter

1. Introduction

Traditionally, power generation systems are among the systems that are given great importance in the industrial field because of the urgent need for electrical energy to operate electrical machines continuously and permanently. Therefore, it is necessary to search for new energy sources to generate electric power without causing environmental pollution. In addition to energy sources, electric power generation systems must be researched and developed to overcome the problems and defects found in traditional generation systems, which include problems with the current and power quality. These two factors are of great importance in the industrial field in terms of reducing periodic maintenance and increasing the life of electrical appliances.

Harmonics are electrical waveform distortions with frequencies that are multiples of the fundamental frequency of the power system [1]. They can be caused by non-linear loads and can result in various negative effects on the power system, such as decreased efficiency, increased losses, reduced power factor, and equipment damage [2].

To mitigate the negative effects of harmonics on an electrical network, several solutions have been proposed; one common solution is the use of harmonic filters, which are designed to minimize the levels of harmonics in the system [3,4]. These filters can be installed at the point of common coupling (PCC), where the harmonic-producing loads are connected to the system, or directly at the source of the harmonics. Passive harmonic filters use passive components to reduce the harmonics in electrical networks [5]. However, they have downsides, such as being less effective in certain applications and creating resonance conditions that damage the equipment [6]. On the other hand, active filters use power electronics to inject a current into the network and cancel out the harmonics, providing several advantages, such as flexibility, improved power factor and efficiency, and reduced equipment damage. However, they require a power source and can generate their own harmonics if not properly designed and controlled [7,8]. In addition to the filter, control strategies can be used or relied upon as a solution to improve the power quality and reduce the harmonic value of the current. In [9], the author concludes that current and power quality can be significantly improved by using hybrid controllers. In addition, smart and nonlinear controls are among the best solutions that have been used in the field of renewable energies to improve energy quality [10,11].

The evolution of active filter topology has undergone several stages of development. The first generation of active filter topology utilized a single-phase bridge rectifier and a DC link capacitor to store energy. It used a second-order low-pass filter to remove high-frequency components and was only suitable for low-power applications with high costs [12]. The second generation of active filters used a three-phase bridge rectifier and a DC link capacitor, which could handle higher power and was more efficient than the first generation. The filter also used pulse width modulation (PWM) techniques to generate compensating currents, which resulted in better harmonic elimination [13]. The third generation of active filters uses cascaded H-bridge inverters instead of three-phase bridge rectifiers, resulting in higher power capacity and efficiency [14]. H-bridge inverters also allow for the more precise control of the compensating current waveform, leading to a better elimination of harmonics [15]. The fourth generation of active filters utilizes multilevel inverters, such as the neutral point clamped (NPC) inverter, which has more voltage levels than traditional inverters and generates a more sinusoidal waveform with lower harmonic distortion [16]. This technology has the potential to further improve the harmonic elimination, reduce the size and cost of the filter, and has higher efficiency due to requiring fewer voltage transitions and lower voltage stress across the switches. The three-Level NPC is scalable and adaptable to different power levels and loads [17,18]. However, it has some disadvantages related to power losses, such as conduction losses and switching losses, which can reduce its efficiency. Moreover, the complexity of the inverter and the need for voltage balancing can increase the manufacturing costs and reduce its reliability [19].

The T-type-inverter-based SAPF is a versatile solution for energy quality improvement in various applications [20]. It operates with high efficiency, reducing its energy consumption and operating costs. The T-type inverter produces a high-quality output voltage waveform with low total harmonic distortion (THD), improving its AC load performance and reducing electromagnetic interference. The power filter can compensate for a wide range of energy quality problems, such as voltage sags, swells, flicker, THD, and reactive power [21,22]. The T-type-inverter-based SAPF is a efficient solution for power quality improvement in various applications. It produces a high-quality output voltage with a low THD value and can compensate for a wide range of power quality problems [23]. To fully realize its benefits, a control strategy must be designed that is capable of providing accurate and rapid compensation for power quality issues, adapting to variations in the power system and load changes. The control strategy involves detecting harmonics, calculating the reference compensating current waveform, and generating the compensating current waveform accordingly [24]. Different modulation strategies, such as space vector modulation (SVM) [25], the PWM technique [26], the neural SVM technique [27], neural PWM [28], and the modified SVM technique [29], can be used to generate control pulses in

the IGBTs of the three-level inverter. These strategies are of great importance in improving the quality of the current and in reducing the cost and complexity of the systems. In [30], the modified SVM technique provides very satisfactory results in terms of current ripples for a three-phase inverter compared to the PWM, SVM, and neural SVM techniques. Therefore, it is necessary to choose the most suitable type of control to be used in order to generate control pulses in the inverter.

Classical controllers, such as the proportional-integral (PI) controller, may not be optimal for all power electronics applications [31], especially when nonlinear systems require strict precision and dynamic characteristics. Nonlinear and intelligent strategies, such as the sliding mode controller (SMC) [32,33], backstepping controller (BC) [34], and high-order SMC techniques [35–39], have been effective in reducing current ripples and improving the power quality, but can be complex and difficult to apply. Fractional-order PI controllers (FOPI) have emerged as viable alternatives due to their extra design parameters and simplicity [40]. Synergetic control (SC) is known for its effectiveness in regulating nonlinear uncertain systems in disturbed environments and has been popular among researchers in various studies [41,42]. The SC technique is among the nonlinear controllers that have emerged as an alternative to SMC control as it is highly efficient in reducing the problem of chatter and in significantly improving the system performance. Its simplicity and ease of implementation are two of the biggest advantages of this strategy. In addition, this strategy can be applied to complex systems with ease, making it the best solution in the field of controlling complex systems. In addition, the SC strategy is not related to the mathematical form of the system under study, meaning it provides satisfactory results in cases of changing the system parameters [41].

This paper suggests the use of the fractional-order synergetic control (FOSC) with a PLL technique as the optimal solution to regulate the SAPF based on a three-phase three-level T-type inverter, as well as when the source voltages are unbalanced and/or distorted. This control strategy is chosen for its simplicity, robustness, and easy implementation, and aims to enhance the current quality and decrease the total system cost. Furthermore, the proposed FOSC approach is employed to regulate the DC voltage and acquire the reference value of the active power. The control proposed in this work is different from several other works [43–45] in terms of its simplicity, principle, ease of implementation, and the results presented. The control described in this work is purely analytical and founded on a nonlinear model. The objective of this control strategy is to increase the stability of the system to cope with the load changes, which are improved under conditions where the efficiency and dynamic characteristics are maintained or even increased compared to the traditional linear control methods. Thus, the main contributions refer to:

- Minimizing the THD value of the current;
- Increasing the durability of the filtration system;
- Improving the dynamic response of the filtering system;
- Improving the power quality under unbalanced and distorted voltage conditions.

This paper is structured as follows: the three-level T-type-inverter-based SAPF is described and modelled in the next section, along with the presentation of its control principle. In Section 3, the SC strategy is theoretically outlined, and its application to the active filter control is presented in Section 3.2. The proposed FOSC strategy with the SVM technique used to control the SAPF is detailed in Section 4. The main results, including those for the case of unbalanced and distorted source voltages, are given in Section 5, and discussed comparatively to the traditional strategy based on a PI controller. Finally, the paper concludes in Section 6 by presenting the main findings and the next research to be conducted.

2. SAPF Configuration and Control

Figure 1 illustrates the overall diagram of the three-level SAPF, designed to mitigate the harmonic currents and reactive the power of the nonlinear load, represented by a three-phase diode rectifier in this study. The proposed system is characterized by its durability,

simplicity, ease of installation, and low-cost maintenance. The three-level T-type inverter employs two DC-bus capacitors to effectively stabilize the DC bus voltage; the SAPF is connected to the distribution system in a PCC through an (Lf-R_f) coupling filter.
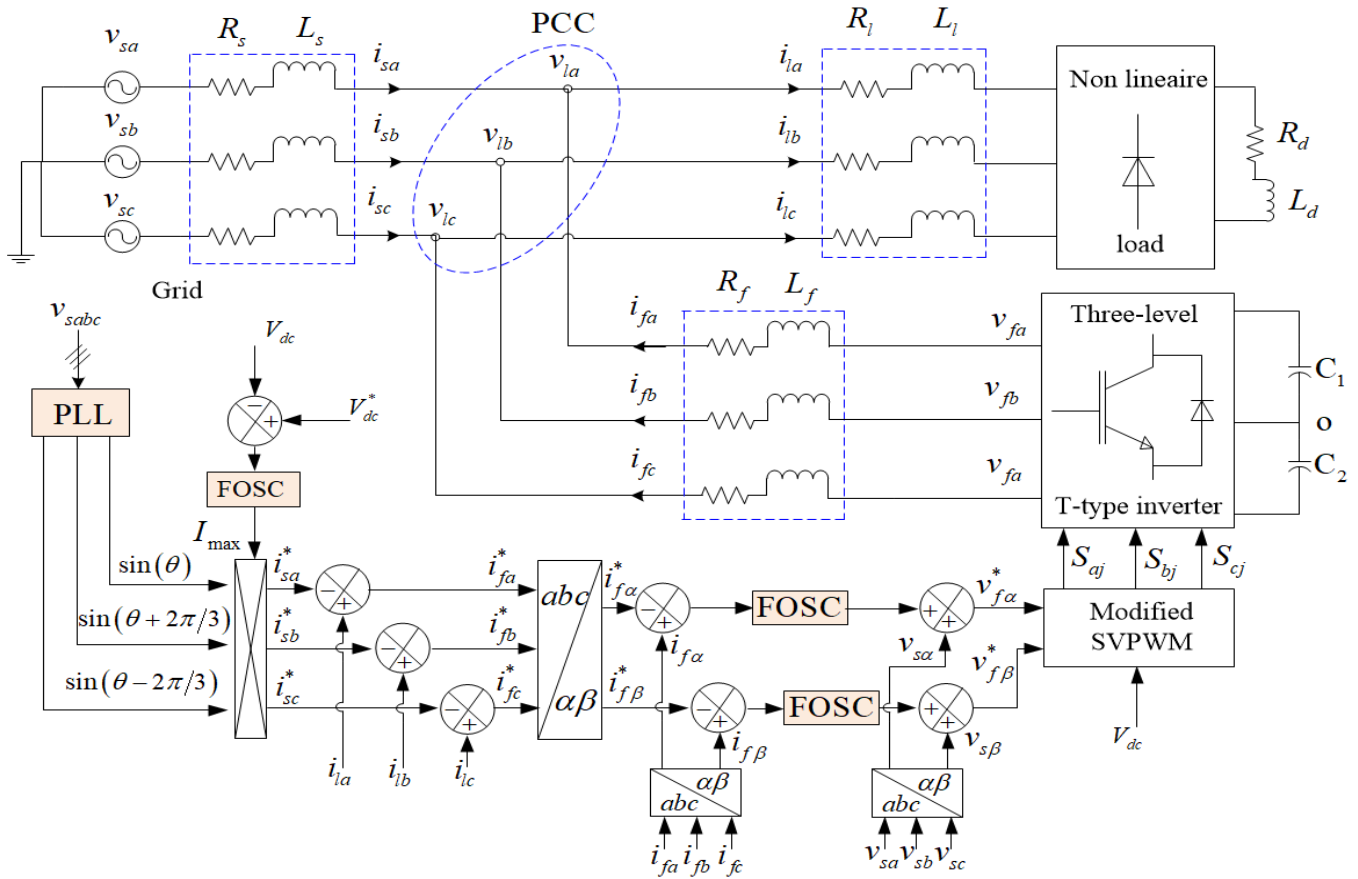

Figure 1. Schematic block of the 3-phase SAPF.

The dynamic model in the $\alpha\beta$ axes, presented below, can be utilized to illustrate the interplay between the active filter and the grid, as the active filter absorbs current i_f from the PCC.

$$\begin{cases} \frac{di_{f\alpha}}{dt} = -\frac{R_f}{L_f}i_{f\alpha} - \frac{1}{L_f}v_{s\alpha} + \frac{1}{L_f}v_{f\alpha} \\ \frac{di_{f\beta}}{dt} = -\frac{R_f}{L_f}i_{f\beta} - \frac{1}{L_f}v_{s\beta} + \frac{1}{L_f}v_{f\beta} \end{cases} \tag{1}$$

The expression for the relationship between the current and voltage in the *dc*-link is given by:

$$C_{dc}\frac{dV_{dc}}{dt} = i_{dc} \tag{2}$$

The active filter controller needs to synthesize the reference currents to eliminate undesirable components. This is achieved by estimating the reference source current and subtracting the load current to calculate the inverter reference current. The FOSC controller uses the power filter's DC bus voltage and reference voltage to determine the maximum source current, which is multiplied by the unit sinusoidal vector in the phase with the source voltages [46,47]. The reference current is obtained by multiplying the current vector of three unities, where Figure 1 illustrates a block diagram of the control algorithm. This approach also takes care of losses in the active filter circuit.

$$\begin{cases} I_{u1} = \sin(\theta) \\ I_{u2} = \sin\left(\theta + \frac{2\pi}{3}\right) \\ I_{u3} = \sin\left(\theta - \frac{2\pi}{3}\right) \end{cases} \tag{3}$$

Using the proposed PLL technique, the angle θ is extracted from the main voltage waveform to maintain a unity power factor, resulting in a balanced current that is free from harmonics and reactive power [47]. The reference source currents are as follows:

$$\begin{cases} i_{sa}^* = I_{max}^* \sin(\theta) \\ i_{sb}^* = I_{max}^* \sin\left(\theta + \frac{2\pi}{3}\right) \\ i_{sa}^* = I_{max}^* \sin\left(\theta - \frac{2\pi}{3}\right) \end{cases} \tag{4}$$

Therefore, the reference currents for the active filter can be expressed as:

$$\begin{cases} i_{fa}^* = i_{la}^* - i_{sa}^* \\ i_{fb}^* = i_{lb}^* - i_{sb}^* \\ i_{fc}^* = i_{lc}^* - i_{sc}^* \end{cases} \tag{5}$$

2.1. PLL-Based STF Technique

The enhanced PLL-based STF (Self Tuning Filter) technique uses the PLL technique to monitor the phase and frequency of the STF signal. The PLL generates a voltage-controlled oscillator (VCO) output that is synchronized with the frequency of the incoming STF signal [48]. The VCO output is then employed to demodulate the STF signal, giving an estimation of the channel impulse response. The STF is a feedback control circuit that is nonlinear and is used to extract the fundamental components of any periodic signal [49]. In addition, the use of the PLL technique increases the system's robustness and stability and greatly improves its dynamic response while improving the power quality. Figure 2 depicts the structure of the PLL technique, which is an improved version of the PLL-technique-based STF and PI controller.
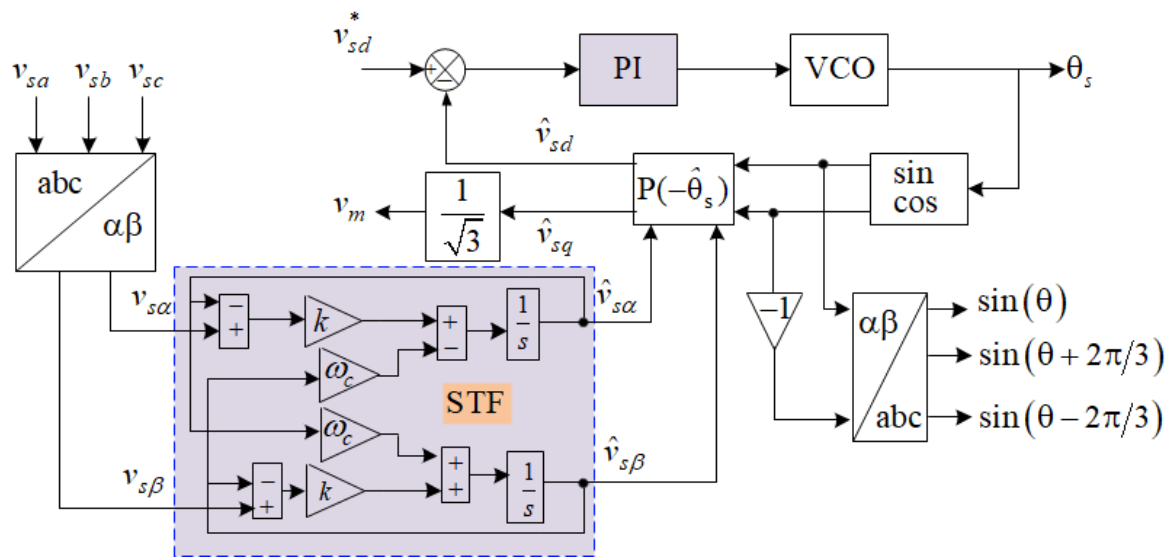

Figure 2. Block diagram of PLL-PI based on STF.

The transfer function that represents the STF can be expressed as follows:

$$G(s) = \frac{V_{xy}(s)}{U_{xy}(s)} = k_e \frac{(s+k) + j\omega_c}{(s+k)^2 + \omega_c^2} \tag{6}$$

The expressions for the continuous components in the stationary reference frame are presented as follows:

$$\begin{bmatrix} \hat{X}_\alpha(s) \\ \hat{X}_\beta(s) \end{bmatrix} = \frac{k}{s} \begin{bmatrix} X_\alpha(s) - \hat{X}_\alpha(s) \\ X_\beta(s) - \hat{X}_\beta(s) \end{bmatrix} + \frac{\omega}{s} \begin{bmatrix} -\hat{X}_\beta(s) \\ \hat{X}_\alpha(s) \end{bmatrix} \tag{7}$$

2.2. 3-Level T-Type Inverter

Studies have shown that the T-type inverter is an active power converter in SAPF systems. Compared to the typical NPC inverter, the T-type inverter requires fewer clamping diodes per phase leg, as it connects the DC-link voltage neutral point using two active bidirectional switches [50]. This results in fewer conduction losses and a smaller implementation size, allowing for a third output voltage level without the need for clamping diodes. Moreover, each bidirectional switch only needs to supply half of the DC-link voltage to the neutral point, which enables the use of power components with a lower voltage [51]. Figure 3 illustrates the power circuit diagram of a three-level T-type converter, comprising four IGBT active switches labeled T_1 to T_4, forming the shape of a T. Two capacitors, C_1 and C_2, are utilized on the DC side to divide the DC input into two voltages and generate the neutral point o. In Figure 3, this inverter is different from the traditional inverter in terms of the number of IGBTs used, the structure, and the ease of implementation. The control signals used in the proposed inverter are different from the control signals used in the conventional inverter. In addition, using this inverter gives better results in terms of the current ripples and THD value.
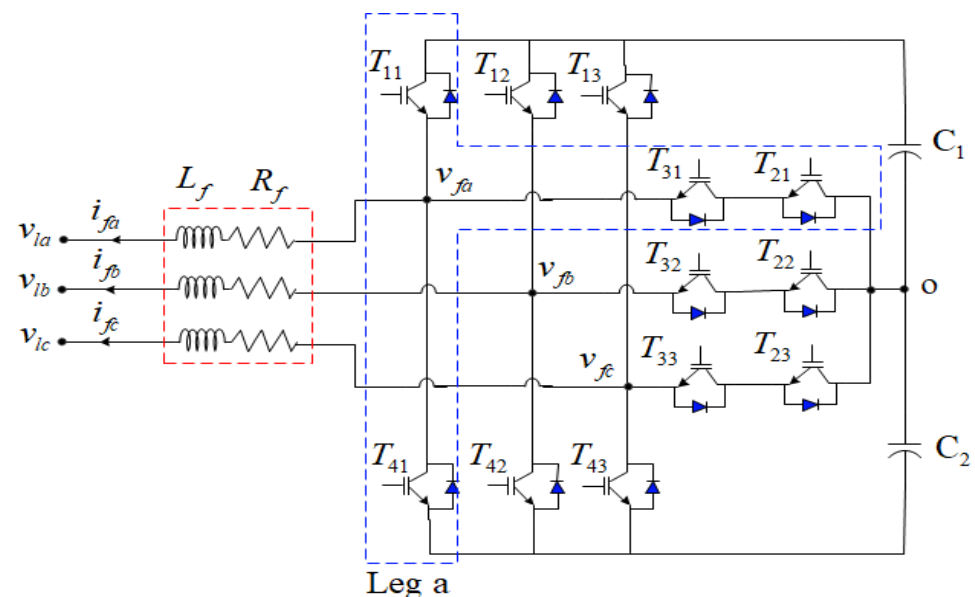

Figure 3. 3-level T-type inverter.

The switching combinations required to attain each of the three potential states—[P], [O], or [N]—for each leg of a T-type inverter are presented in Table 1.

Table 1. Switching state for 3-level T-type inverter.

States	Status of Switching Devices (x = 1, 2, 3) (1 = ON, 0 = OFF)				Voltage
	Tx1	**Tx2**	**Tx3**	**Tx4**	
P	1	1	0	0	$Vdc/2$
O	0	1	1	0	0
N	0	0	1	1	$-Vdc/2$

The T-type inverter has a complementary behavior among the switching components of the same leg. When one component is turned ON, the other must be turned OFF, and both cannot be ON or OFF simultaneously. Additionally, the T-type inverter avoids dynamic voltage-sharing problems by prohibiting transitions between the P and N states. The T-type inverter's output voltage step changes have a magnitude of Vdc/2, which is half the size of classical inverters, resulting in reduced voltage stress.

3. Control Strategy

3.1. Fractional Differentiation and Integration

The Riemann-Liouville fractional derivative is the basis for defining fractional differentiation and integration, which are employed in constructing fractional control systems [52–54].

- The Riemann-Liouville fractional integral of order $\mu \in R+$ is defined as [55]:

$$I_{la}^{\mu} f(t) = \frac{1}{\Gamma(\mu)} \int_{l_a}^{t} (t-\tau)^{\mu-1} f(\tau) d\tau \tag{8}$$

- The initial time is taken to be zero.
- The Riemann-Liouville fractional derivative of order μ as:

$$_{I_a}^{RL} D_t^{\mu} = \frac{1}{\Gamma(s-\mu)} \frac{d^s}{dt^s} \int_{I_a}^{t} (t-\tau)^{s-\mu-1} f(\tau) d\tau \tag{9}$$

where the Euler Gamma function is defined as:

$$\Gamma(s-\mu) = \int_{0}^{\infty} v^{s-\mu-1} e^{-v} dv \tag{10}$$

3.2. SC Design

The SC technique is among the most reliable controls in the field of power system control due to its robustness, simplicity, high efficiency, and ease of implementation. This strategy does not require knowledge of the mathematical form of the system and the dynamic response can be easily adjusted due to the presence of a small number of parameters.

The basis for designing a SC technique is the analytical design of aggregated regulator (ADAR) approach, as described in references [56–58]. We will consider a nonlinear dynamical system with n dimensions, governed by the following equation:

$$\frac{dx(t)}{dt} = f(x, u, t) \tag{11}$$

In the first step of SC design, a macro-variable or system state variable function is chosen, such as:

$$\psi = \psi(x, t) \tag{12}$$

In this case, $\psi(x, t)$ is a user-defined function based on the system state variable, while ψ represents the macro-variable (MV). The characteristics of the MV can be determined based on factors such asthe control parameters, response time, command limitations, and so forth.

The objective of the SC technique is to direct the system to a manifold where the value of the MV is zero [59]. The desired behavior of the MV is defined by the following equation:

$$T\dot{\psi} + \psi = 0; \quad T > 0 \tag{13}$$

The above equation incorporates T as a design parameter that determines the speed of convergence of the closed-loop system towards the manifold, while $\dot{\psi}$ represents the derivative of the aggregated MV.

The above differential equation can be solved to obtain the function for $\psi(T)$, which is given by:

$$\psi(t) = \psi_o e^{-\frac{t}{T}} \tag{14}$$

The function ψ_o tends to move towards $\psi(T)$ from any initial state $\psi = 0$. This phenomenon can be explained as follows:

$$\dot{\psi} = \frac{d\psi}{dx}\frac{dx(t)}{dt} \tag{15}$$

By incorporating Equations (11), (13) and (15), we can derive the following expression:

$$T\frac{d\psi}{dx}f(x, u, t) + \psi = 0 \tag{16}$$

After solving (16) for u, we can express the control law as:

$$u = g(x, \psi(x, t), T, t) \tag{17}$$

The control rule, as shown in Equation (17), is dependent not only on the system state variables, but also on the MV and the control parameter T. To define the characteristics of the controller, the designer can choose a suitable MV and a specific command parameter T.

The stability analysis of a system can be conducted using the Lyapunov function, which operates as follows [60]:

$$V = \frac{1}{2}\psi(x, t)^2 \tag{18}$$

This function's derivative can be expressed as:

$$\dot{V} = \dot{\psi}(x, t)\psi(x, t) = -\frac{1}{T}\psi(x, t)^2 < 0 \quad if \quad T > 0 \tag{19}$$

Equation (19) implies that the stability of the closed-loop system towards the attractor remains unaffected by the system model's nonlinearity, and it remains stable even if the value of parameter T is increased.

4. Fractional-Order Synergetic Control

To mitigate harmonics and address reactive power in the grid, the three-level T-type-inverter-based SAPF is operated using the proposed FOSC approach in the study. This control guarantees a dependable closed-loop system and effective tracking control [61]. To enhance the controller's degree of freedom, the fractional-order MV is defined using the following equation:

$$\psi_{\omega fr} = K_p(x^* - x) + K_i I_a^\mu(x^* - x) \tag{20}$$

Therefore, K_p and K_i are the proportional and integral factors of the fractional-order MV, while x^* and x represent the actual controlled and reference values. Additionally, μ refers to the order of the fractional integral.

4.1. Design of a Dc-Link Voltage Controller

The aim of the voltage fractional-order synergetic controller is to regulate the DC-link voltage and follow a reference profile. Specifically, the DC-link controller's goal is to track the DC voltage reference, as follows:

$$e_{vdc} = V_{dc}^* - V_{dc} \tag{21}$$

The fractional-order MV is expressed as:

$$\psi_{dcfr} = K_{p_{vdc}}e_{vdc} + K_{ivdc}I^{\mu_{vdc}}e_{vdc} \tag{22}$$

By substituting Equations (21) and (22) into Equation (13), the dynamics can be expressed as:

$$T\left(K_{p_{vdc}}\left(\dot{V}_{dc}^* - \dot{V}_{dc}\right) + K_{i_{vdc}}I^{\mu_{vdc}-1}(V_{dc}^* - V_{dc})\right) + K_{p_{vdc}}e_{vdc} + K_{i_{vdc}}I^{\mu vdc}e_{vdc} = 0 \tag{23}$$

After substituting Equation (2) into Equation (23) and rearranging the fractional-order SC technique law, we obtain:

$$i_{dc} = I_{max} = \frac{C_{dc}}{TK_{p_{vdc}}} \left(TK_{p_{vdc}} \dot{V}^*_{dc} + TK_{i_{vdc}} I^{\mu_{vdc}-1} e_{vdc} + \psi_{vdc} \right) \tag{24}$$

4.2. Design of Current Control

The objective of the current controller is to generate the SVM technique input for the inverter switching signals. The difference between the currents can be represented as follows:

$$\begin{cases} e_{if\alpha} = i^*_{f\alpha} - i_{f\alpha} \\ e_{if\beta} = i^*_{f\beta} - i_{f\beta} \end{cases} \tag{25}$$

Thus, two fractional-order MVs are chosen as:

$$\begin{cases} \psi_{i_{f\alpha}fr} = K_{p\alpha} e_{if\alpha} + K_{i\alpha} I^{\mu_\alpha} e_{if\alpha} \\ \psi_{i_{f\beta}fr} = K_{p\beta} e_{if\beta} + K_{i\beta} I^{\mu_\beta} e_{if\beta} \end{cases} \tag{26}$$

Here, $K_{p\alpha}$, $K_{i\alpha}$, $K_{p\beta}$, and $K_{i\beta}$ represent the proportional and integral parameters of the fractional-order MVs for the current components.

After substituting Equation (26) into Equation (13), the dynamics are expressed as follows:

$$\begin{cases} T_\alpha \left(K_{p_\alpha} (\dot{i}^*_{f\alpha} - \dot{i}_{f\alpha}) + K_{i\alpha} I^{\mu_\alpha-1} (\dot{i}^*_{f\alpha} - \dot{i}_{f\alpha}) \right) + K_{p_\alpha} e_{if\alpha} + K_{i\alpha} I^{\mu_\alpha} e_{if\alpha} = 0 \\ T_\beta \left(K_{p_\beta} (\dot{i}^*_{f\beta} - \dot{i}_{f\beta}) + K_{i\beta} I^{\mu_\beta-1} (\dot{i}^*_{f\beta} - \dot{i}_{f\beta}) \right) + K_{p_\beta} e_{if\beta} + K_{i\beta} I^{\mu_\beta} e_{if\beta} = 0 \end{cases} \tag{27}$$

The process of synthesizing Equations (1) and (27) allows for the calculation of the control outputs, which can be expressed in the following manner:

$$\begin{cases} T_\alpha K_{p_\alpha} \dot{i}^*_{f\alpha} - T_\alpha K_{p_\alpha} \left(-\frac{R_f}{L_f} i_{f\alpha} - \frac{1}{L_f} v_{s\alpha} + \frac{1}{L_f} v_{f\alpha} \right) + T_\alpha K_{i\alpha} I^{\mu_\alpha-1} e_{if\alpha} + \psi_{if\alpha} = 0 \\ T_\beta K_{p_\beta} \dot{i}^*_{f\beta} - T_\beta K_{p_\beta} \left(-\frac{R_f}{L_f} i_{f\beta} - \frac{1}{L_f} v_{s\beta} + \frac{1}{L_f} v_{f\beta} \right) + T_\beta K_{i\beta} I^{\mu_\beta-1} e_{if\beta} + \psi_{if\beta} = 0 \end{cases} \tag{28}$$

Once Equation (28) is simplified, it is possible to express the input of SVM control in the following manner:

$$\begin{cases} v^*_{f\alpha} = \dfrac{L_f \left(T_\alpha K_{p_\alpha} \dot{i}^*_{f\alpha} + T_\alpha K_{p_\alpha} \left(\frac{R_f}{L_f} i_{f\alpha} + \frac{1}{L_f} v_{s\alpha} \right) + T_\alpha K_{i\alpha} I^{\mu_\alpha-1} e_{if\alpha} + \psi_{if\alpha} \right)}{T_\alpha K_{p_\alpha}} \\[4mm] v^*_{f\beta} = \dfrac{L_f \left(T_\beta K_{p_\beta} \dot{i}^*_{f\beta} + T_\beta K_{p_\beta} \left(\frac{R_f}{L_f} i_{f\beta} + \frac{1}{L_f} v_{s\beta} \right) + T_\beta K_{i\beta} I^{\mu_\beta-1} e_{if\beta} + \psi_{if\beta} \right)}{T_\beta K_{p_\beta}} \end{cases} \tag{29}$$

The parameters of this control were determined through trial and error, while considering factors such as the quality of adjustment, filtering, and the system ability to withstand load variations. In addition to the FOSC technique, the SVM technique is used for inverter control.

The SVM technique is a highly promising modulation technique for operating multi-level inverters, offering a 15% larger range of modulation, 15% greater flexibility in the gate driving signal, and lower current harmonic distortion compared to conventional sinusoidal PWM, as reported in [62]. In this study, the SVM technique plays a vital role in selecting the switching states and sequences, as well as determining the dwell periods. Although the updated algorithm is not the primary focus, readers can refer to the overview provided for a general understanding of this approach, while more details on the algorithm can be found in [63–65].

Figure 4a shows the hexagonal SVM diagram, which is divided into six sectors (A–F) and has a total of 27 switching states spread over four regions. When V_{ref} is in the first

sector, the reference vector is generated using the three closest vectors (V_1, V_2, and V_8). The dwell time is computed using the following steps:

$$\begin{cases} \vec{V}_{ref}T_s = \vec{V}_1 t_a + \vec{V}_8 t_b + \vec{V}_2 t_c \\ T_s = t_a + t_b + t_c \end{cases} \tag{30}$$
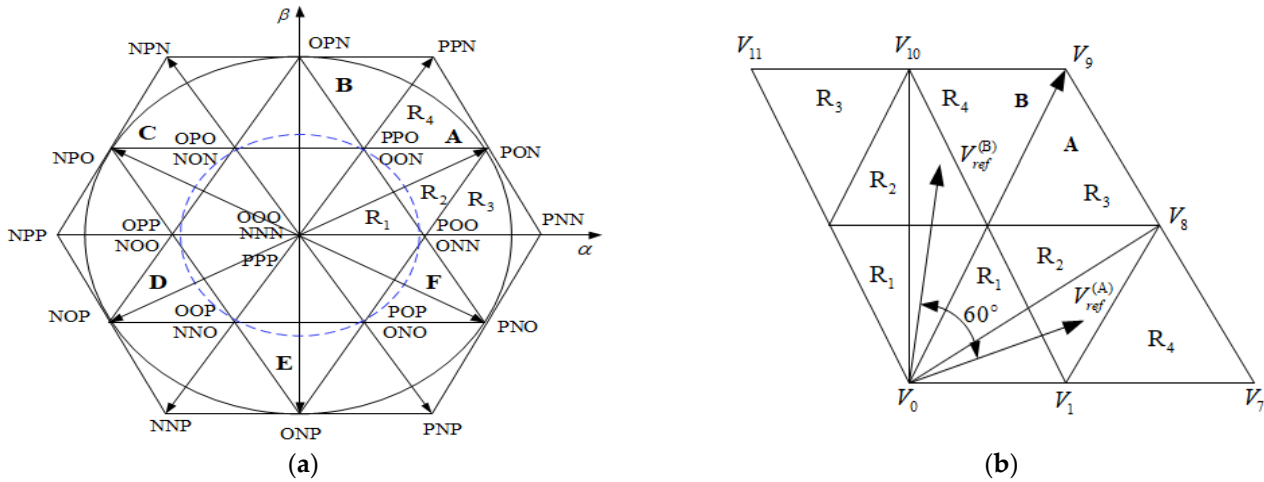

Figure 4. (**a**) Space-vector diagram of the 3-level converter, (**b**) Two vectors with 60° shifting in sectors A and B.

The ON-time during the sampling period (T_s) for voltage vectors V_1, V_8, and V_2 is represented by t_a, t_b, and t_c, respectively.

The instantaneous voltage in the $\alpha\beta$ frame, obtained through Clark's transformation, is represented by a magnitude and angle, and is denoted as $\vec{V}_{ref}$, as shown below:

$$\left| \vec{V}_{ref} \right| = \sqrt{v_\alpha^2 + v_\beta^2}, \quad \theta = \tan^{-1}\left(\frac{v_\beta}{v_\alpha} \right) \tag{31}$$

A similar procedure can be used to calculate the dwell time in other sectors of sector A. After setting the ON-time, the switching sequence should be determined, taking into account the redundant switching states of the converter. The goal is to minimize the THD value.

The six sectors of the hexagon in the SVM technique exhibit geometrical symmetry, which results in a strong correlation between the ON-time calculations and the ON-time arrangement. This means that adjustments can be made more easily as a single computation performed on the first sector can be extended to the other sectors [66]. For instance, the reference vector B can be obtained by rotating the reference vector A counter-clockwise by 60 degrees, as shown in Figure 4b, when the reference vector A is in area 2 of sector A. Therefore, the following equation can be used to express the reference vector V_{ref}^B:

$$V_{ref}^{(B)} = V_{ref}^{(A)} * e^{\frac{j\pi}{3}} = \frac{2}{3}\left(-V_b - V_c e^{\frac{j2\pi}{3}} - V_c e^{-\frac{j2\pi}{3}} \right) \tag{32}$$

In cases where the reference vector is situated in a different sector, it will be rotated to sector A by $n\pi/3$, where n ranges between 1 and 6.

5. Results

This section describes the outcomes of implementing the three-level T-type-inverter-based SAPF using a fractional-order SC technique and a PLL technique based on a STF in Matlab software. The filter is depicted in Figure 1, and its key parameters are listed in Table 2 [67]. The simulation tests are conducted under three conditionsto verify the robustness of the (FOSC): source voltage balanced, source voltage unbalanced, and source

voltage distorted, with a load change introduced at $t = 0.3$ s in all cases. The simulation findings are compared to those of the traditional PI control approach.

Table 2. Simulated system parameters.

Parameter	Value
Source voltage and frequency	220 V, 50 Hz
R_f, L_f	5 mΩ, 3 mH
$R_s, \ L_s$	0.1 Ω, 3 mH
R_d, L_d	40 Ω, 10 mH
R_L, L_L	1.2 mΩ, 0.2 mH
C_{dc}	4 mF
Total DC-bus voltage reference	700 V

A.   Source voltage balanced

The following test was conducted with a balanced source voltage and a load change introduced at $t = 0.3$ s for both the FOSC and PI controls. Figure 5 illustrates the main results obtained from this test, including the waveforms for the mains voltage, source current, load current, active filter current and its reference (Phase a), and voltage and current in Phase a for both controls. It can be observed from the figure that as soon as the active filter is connected at the PCC, the compensating current quickly tracks its reference and precisely follows it during the steady-state period. Furthermore, when the load change occurs at $t = 0.3$ s, the active filter current responds as efficiently as the reference current, resulting in a sinusoidal source current with a perfectly in-phase sinusoidal current and voltage, leading to zero reactive power and a unity energy factor on the grid side. While the results may initially appear similar for both controls, differences between the two will become apparent in the subsequent results.
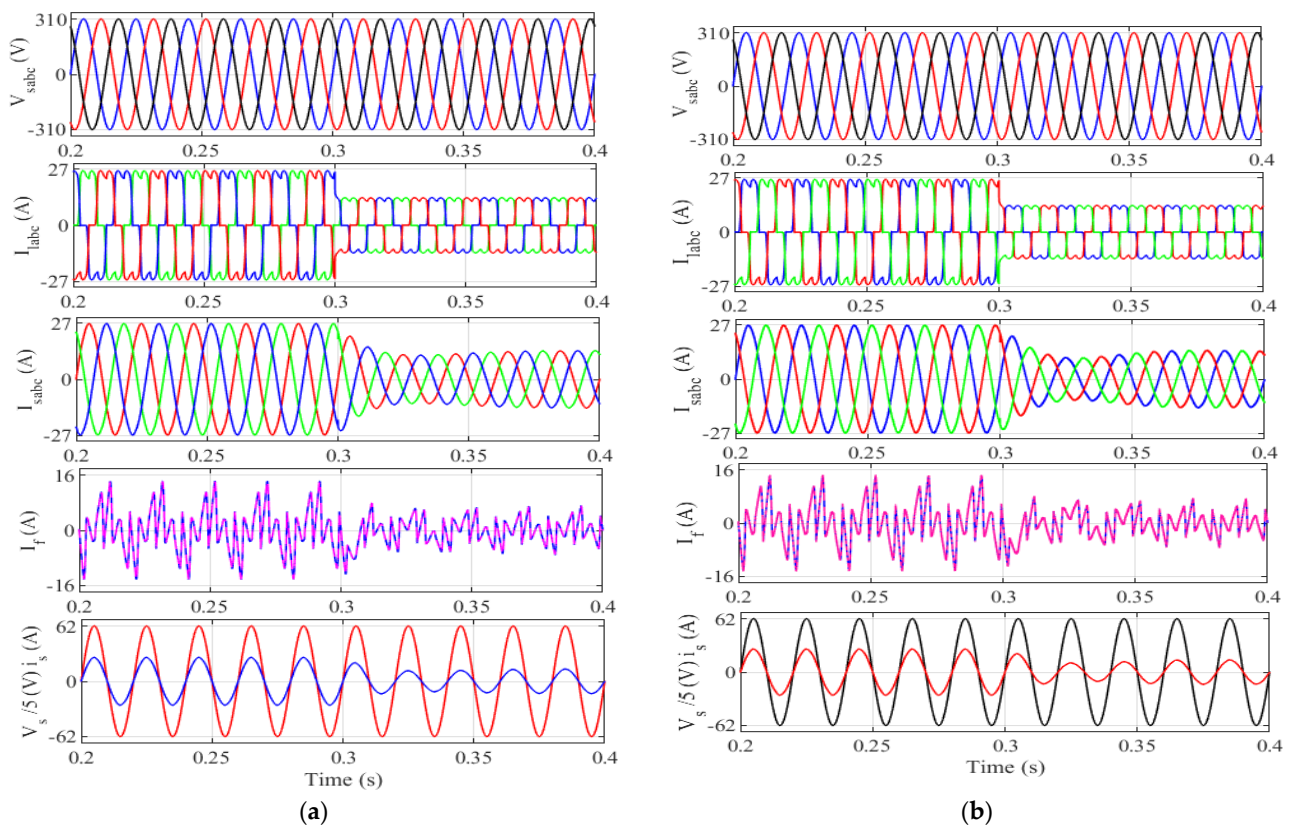

Figure 5. Performance of SAPF under source voltage balanced, and load change at $t = 0.3$ s: (**a**) using FOSC, (**b**) using PI.

Figure 6 provides additional clarification by displaying the source current (after filtering) for each of the controls. The distinction between the controls can be observed through the variation in the current ripples, with control PI displaying more ripples. This confirms that the suggested control method diminishes the ripples, resulting in fewer current harmonics in comparison to control PI.
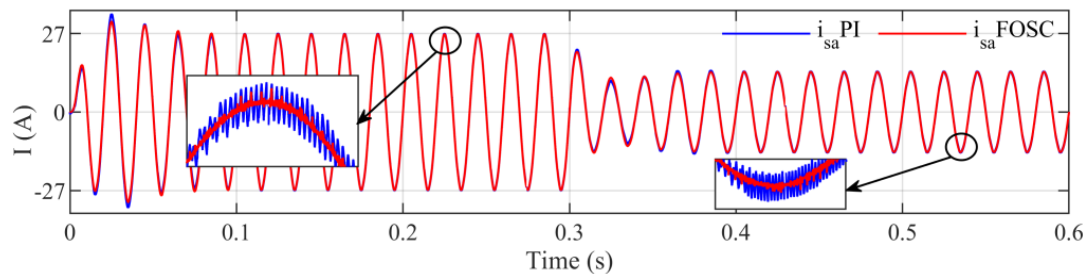

Figure 6. Source current after filtering using PI and FOSC (Phase a).

Figure 7 illustrates the harmonic spectrums of the source current before filtering and after load change, with corresponding values of 25.11% and 26.67%. By using the PI controller, the THD of the source current is minimized from 1.32% and 2.12%, respectively, as represented in Figure 8. However, when implementing the designed nonlinear control, the THD of the source current is further reduced to 0.85% and 0.77%, as represented in Figure 9, demonstrating that the designed control produces lower THD compared to the conventional PI controller. As shown in Figures 8 and 9, the two controls used in this work provide equal results in terms of the amplitude value of the fundamental signal (50 Hz) of the current before and after the load change.
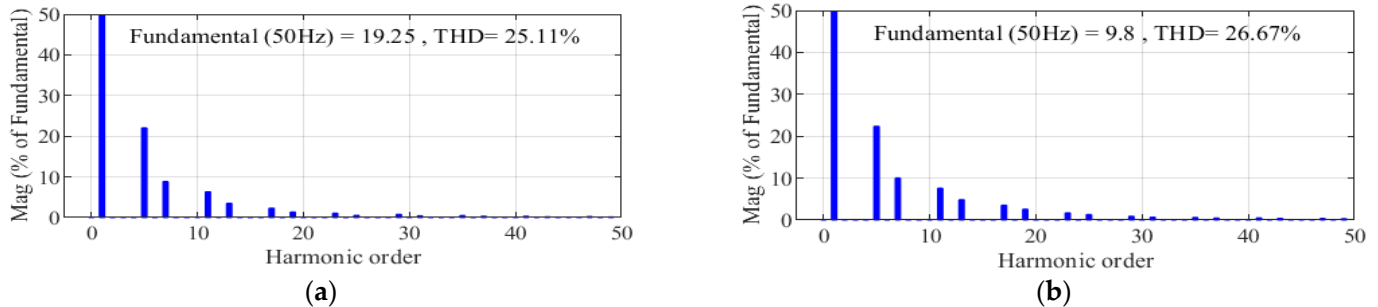

Figure 7. Source current harmonic spectrum before filtering: (**b**) After load change, (**a**) Before load change.
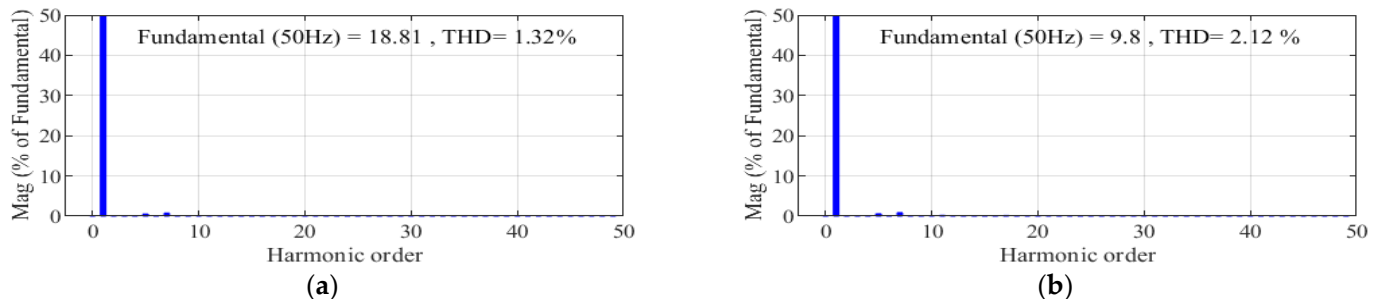

Figure 8. Source current harmonic spectrum after filtering using (PI): (**a**) Before load change, (**b**) After load change.

Figure 10 depicts the DC-bus voltage for both the proposed control and the conventional PI control. It can be observed that the designed control achieves the desired voltage level quickly, without any overshoot, immediately after the active filter is connected to the grid. Furthermore, a fast response is also observed following a load variation. In

contrast, the PI control exhibits a slow response and surpasses the reference value after the filter is connected, as well as a slow response after the load change. Moreover, the proposed controller provided a lower DC-bus voltage overshoot value compared to the conventional controller based on a PI controller. These results suggest that the designed control outperforms the traditional control in terms of the response time and stability.
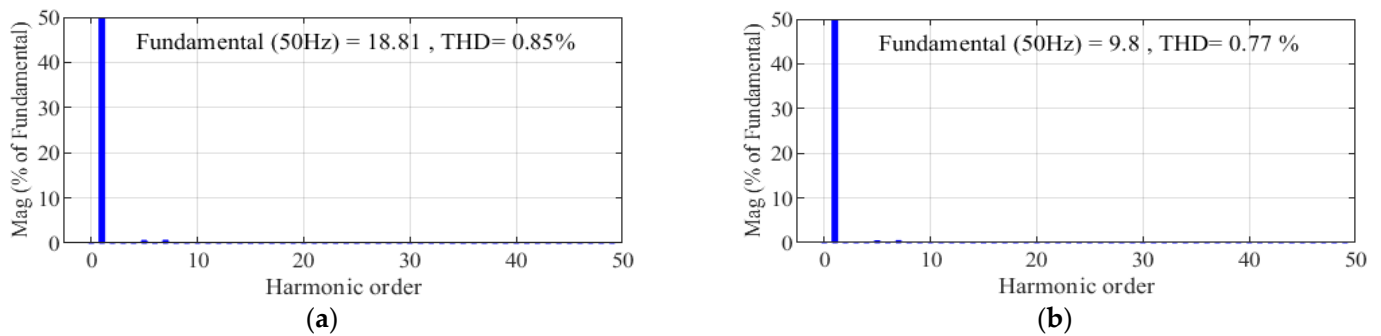

Figure 9. Source current harmonic spectrum after filtering using (FOSC): (**a**) Before load change, (**b**) After load change.

Figure 10. DC-bus voltage for both controls.

In Figure 11, the waveforms of the instantaneous real and imaginary power at the source site are depicted. It is evident from the figure that the proposed control method yields a superior dynamic performance and fewer power oscillations during steady-state operation. With the use of FOSC control, the real power profile exhibits almost continuous behavior, with slight oscillations, during steady-state operation. Additionally, the imaginary power profile remains continuous and very close to zero throughout the simulation, which affirms the active filter's compensating role for reactive power in the grid. However, when a PI controller is employed, there are more significant oscillations in both the real and imaginary powers. Once again, this confirms that the proposed control is more effective in improving the energy quality compared to the PI control.
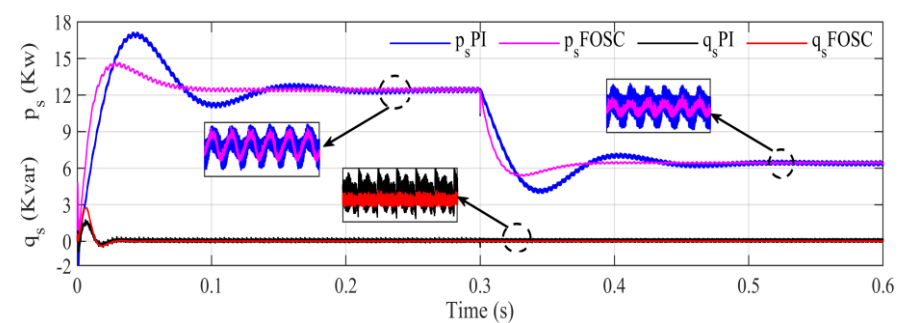

Figure 11. Real and imaginary powers in the source using PI and FOSC.

B.   Source voltage unbalanced

This test was conducted with an unbalanced source voltage and a load change introduced at $t = 0.3$ s for both the FOSC and PI controls.

The aim of these tests is to investigate the performance of the SAPF and the PLL-technique-based Self-Tuning Filter (PLL$_{STF}$) in scenarios where the source voltage is unbalanced, as well as to minimize harmonic currents and achieve a unity power factor. The main outcomes of this test are depicted in Figure 12, which displays, for both controls, various waveforms, such as an unbalanced mains voltage, load current, source current, active filter current, as well as current and voltage in Phase a for both controls.

Figure 12. Performance of SAPF under source voltage unbalanced, and load change at *t* = 0.3 s (**a**) using FOSC; (**b**) using PI.

The figure depicts that once the active filter is connected at the PCC, the compensating current immediately follows its reference and accurately tracks it during the steady-state period, demonstrating the effectiveness of the reference current harmonic identification method based on the PLL technique. Moreover, when a load change occurs at *t* = 0.3 s, the active filter current responds with the same efficiency as the reference current, resulting in a sinusoidal source current with a perfectly in-phase sinusoidal current and voltage, leading to zero reactive power and a unity power factor on the grid side.

Figure 13 depicts the filtered source current for each control method, providing further explanation. By analyzing the current ripples, the difference between the control methods becomes apparent. Control PI exhibits greater current ripples, confirming that the proposed control reduces ripples in the presence of unbalanced source voltage, resulting in fewer current harmonics compared to the traditional strategy based on PI controllers.

Figure 14 depicts the harmonic spectrums of the source current after filtering and after load change, in the case of an unbalanced source voltage. Using the PI controller, the THD of the source current is minimized from 25.11% and 26.67%, respectively, to 3.02% and 3.49%, as shown in the figure. However, the proposed nonlinear control results in even lower THD of the source current, reducing it from 25.11% and 26.67% to 2.17% and 2.23%, as illustrated in Figure 15. In addition, it is noted that the value of the fundamental amplitude (50 Hz) of the current in the cases before and after the load change is the same in the two

controls, which indicates that the proposed control is efficient in increasing the amplitude value of the fundamental signal (50 Hz). This demonstrates that the proposed control achieves lower THD compared to the conventional PI controller, within the parameters defined by IEEE Std. 519.
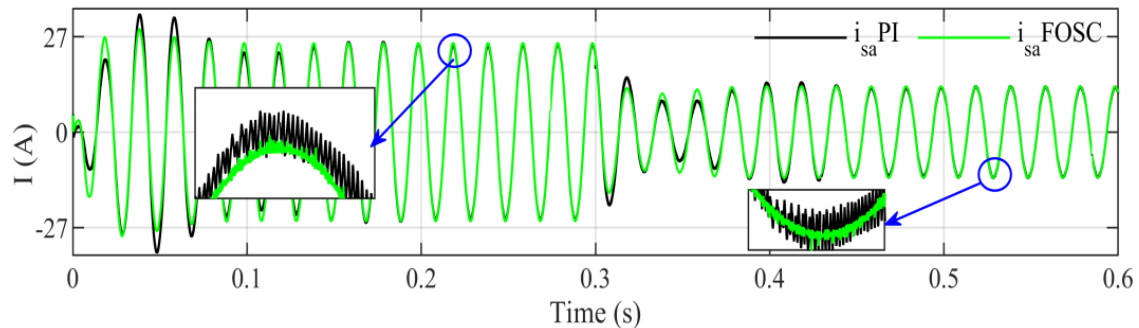

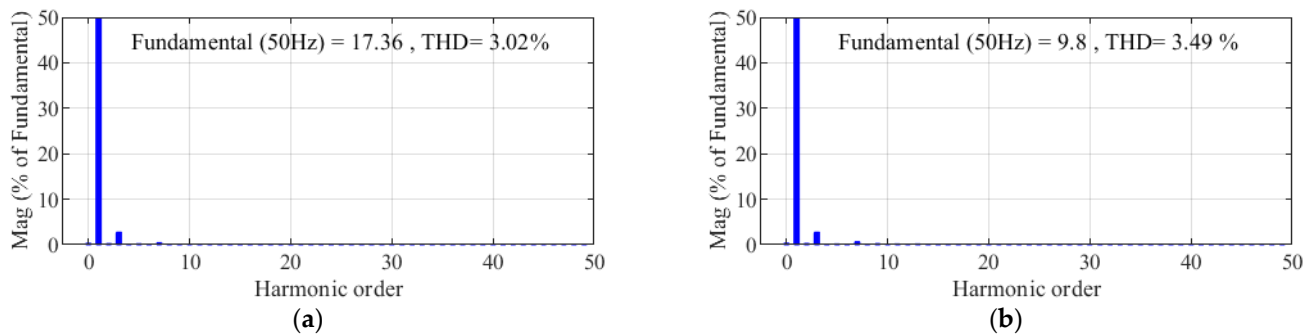**Figure 13.** Source current after filtering under source voltage unbalanced using PI and FOSC (Phase a).

Figure 14. THD Source current under source voltage unbalanced using (PI): (**a**) Before load change, (**b**) After load change.
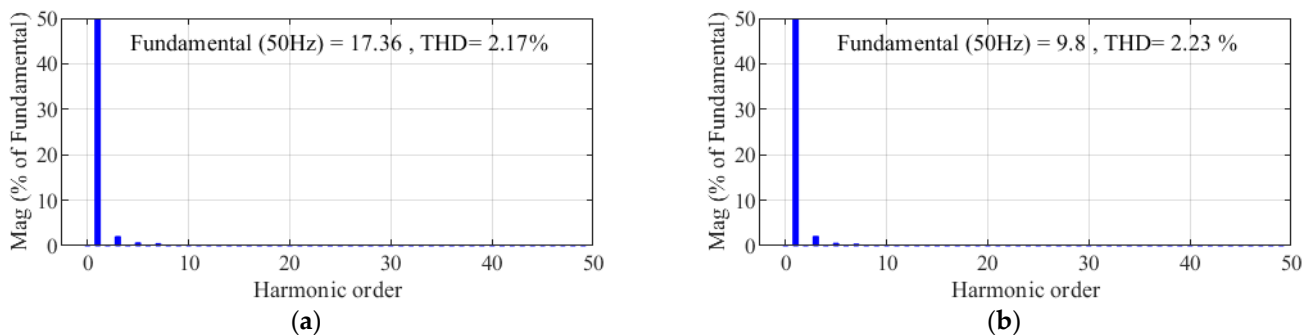

Figure 15. THD Source current under source voltage unbalanced using (FOSC): (**a**) Before load change, (**b**) After load change.

The DC-bus voltage for the proposed control and the conventional PI control is shown in Figure 16. It can be observed that the designed control achieves the desired voltage level quickly, without any overshoot, as soon as the active filter is connected to the grid. Additionally, it exhibits a fast response following a load variation. In contrast, the PI control shows a slow response and exceeds the reference value after the filter is connected. It also exhibits a slow response after the load change. These findings indicate that the designed control is superior to the classical control in terms of its stability and response time.

C.   Source voltage distorted

Typically, in an ideal scenario, the source is composed of a balanced three-phase power supply with sinusoidal voltage waves. However, the voltage of the source is often distorted,

and the systems linked to the PCC must be capable of withstanding such conditions. One of the primary disturbances is the existence of line voltage harmonics of orders 5, 7, and 11.
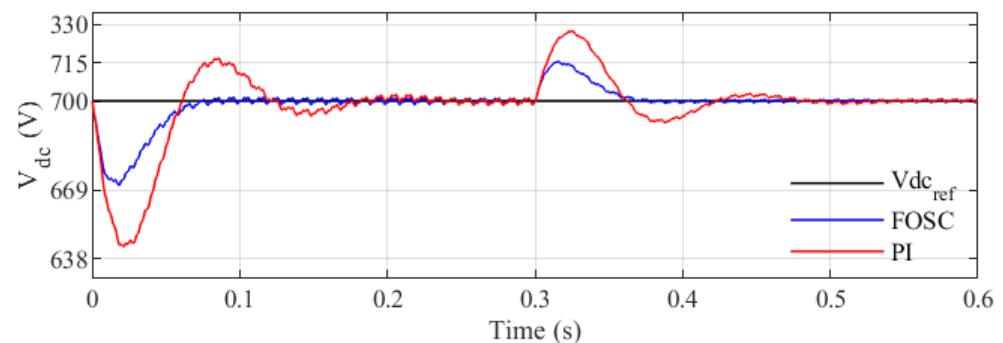

Figure 16. DC-bus voltage under source voltage unbalanced for both controls.

The performance of the SAPF was tested in the presence of a distorted source voltage and a load change at $t = 0.3$ s, using both the FOSC strategy and PI controllers. Both the FOSC strategy and PI controllers were utilized to test the performance of the SAPF and the PLL technique based on scenarios where the source voltage is distorted, as well as to minimize the harmonic currents and achieve a unity power factor. The test involved introducing a load change at $t = 0.3$ s.

The main results of the test are presented in Figure 17, which includes waveforms such as a distorted mains voltage, load current, source current, active filter current, and its reference (Phase a), as well as voltage and current in Phase a. Both controls are represented in the figure. Once the active filter is connected at the PCC, the compensating current immediately tracks its reference and accurately follows it during the steady-state period, indicating the effectiveness of the reference current harmonic identification method based on the PLL technique. Additionally, the active filter current responds to a load change at $t = 0.3$ s with the same efficiency as the reference current, resulting in a sinusoidal source current with a perfectly in-phase sinusoidal current and voltage, leading to zero reactive power and a unity power factor on the grid side.

In Figure 18, the filtered source current is shown for each control method, which helps to explain the differences between them. By examining the current ripples, it be-comes evident that the traditional control produces more significant ripples, indicating that the proposed control method decreases ripples when the distorted source voltage is present, resulting in fewer current harmonics than the traditional control based on PI controllers.

Figure 19 illustrates the harmonic spectra of the source current after filtering and load change under distorted source voltage. The utilization of the PI controller minimized the THD of the source current from 25.11% and 26.67% to 3.51% and 4.11%, respectively, as shown in the figure. However, as depicted in Figure 20, the suggested nonlinear control strategy resulted in significantly lower THD of the source current, decreasing it from 25.11% and 26.67% to 3.40% and 3.39%, respectively. In addition, it is noted in Figures 19 and 20 that the value of the fundamental amplitude (50 Hz) of the current in two cases, before and after the load change, is the same as the amplitude of the signal in the proposed and traditional controls, which leads to the conclusion that the proposed control has the efficiency to raise the value of the amplitude of the fundamental signal (50 Hz). These results suggest that the designed control outperforms the classical PI controller and achieves lower THD within the limits set by IEEE Std. 519.

Figure 21 shows the DC-bus voltage for the proposed control and the conventional PI control. The proposed control technique quickly achieves the desired voltage level without overshooting and responds rapidly to load changes. In comparison, the PI control has a slow response, exceeds the reference value, and reacts slowly to load changes. Therefore, the proposed control technique outperforms the traditional control in terms of its stability and response time.
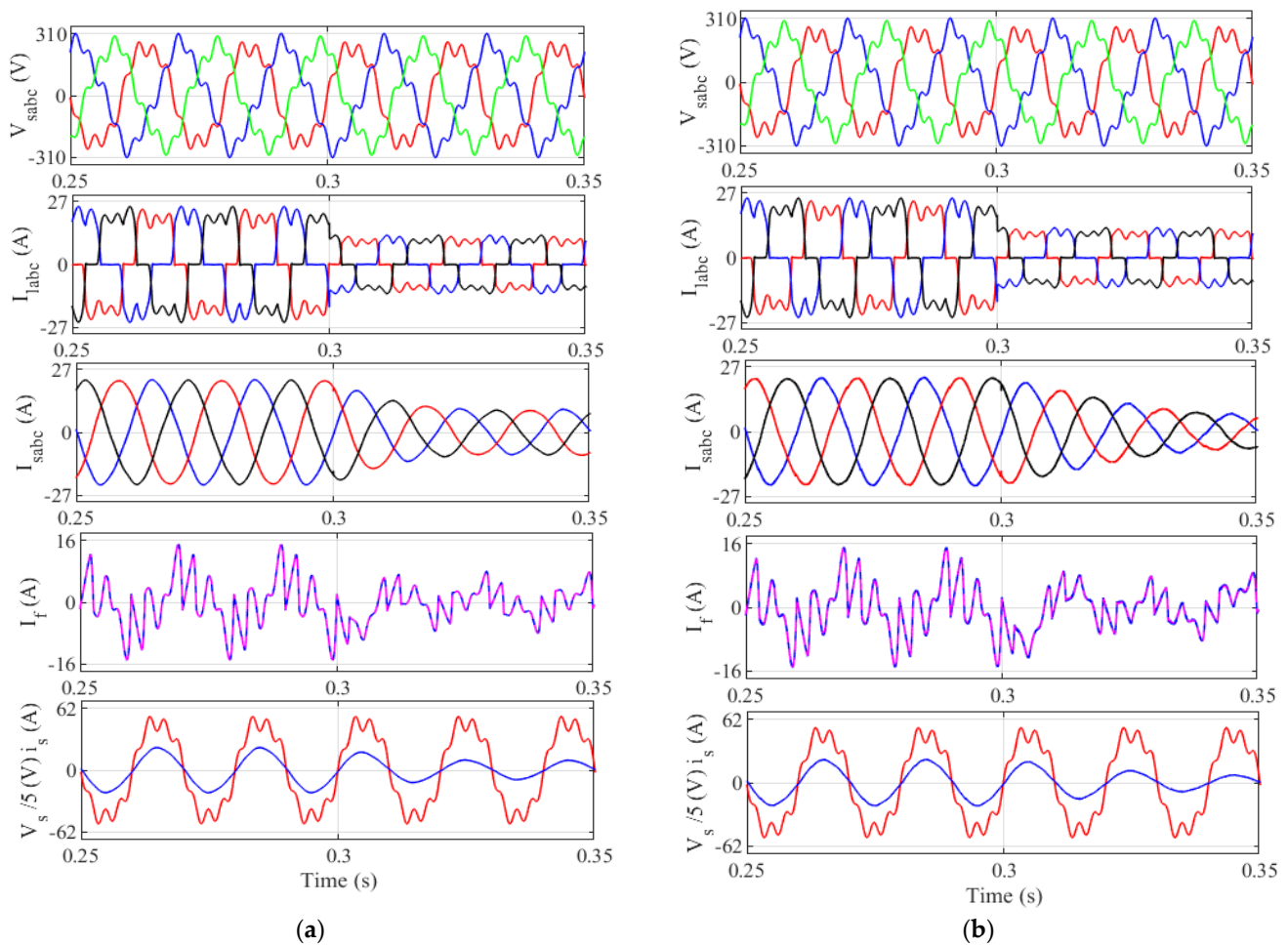
Figure 17. Performance of SAPF under source voltage distorted, and load change at $t = 0.3$ s (**a**) using FOSC; (**b**) using PI.
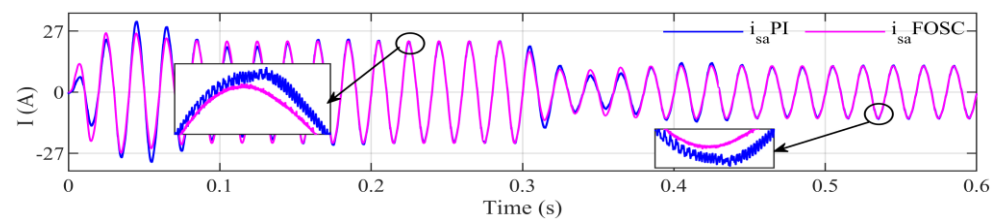

Figure 18. Source current after filtering under source voltage unbalanced using PI and FOSC (Phase a).
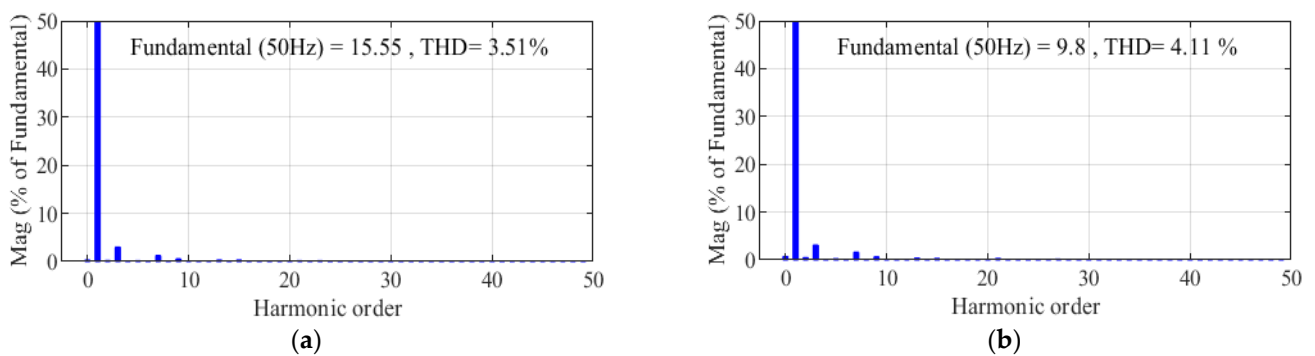

Figure 19. THD source current under source voltage distorted using (PI): (**a**) Before load change, (**b**) After load change.
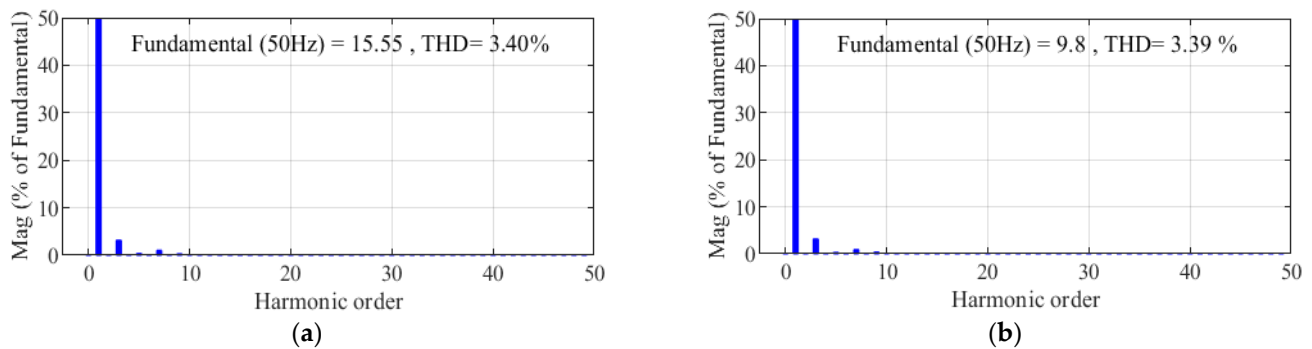
Figure 20. THD source current under source voltage distorted using (FOSC): (**a**) Before load change, (**b**) After load change.
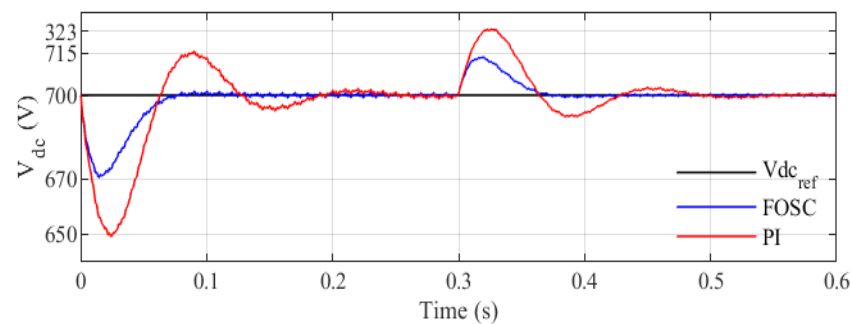

Figure 21. DC-bus voltage under source voltage distorted for both controls.

The comparative results between the designed FOSC control and the PI control are presented in Tables 3 and 4.

Table 3. Quantitative analysis for DC bus voltage.

Transient Time (s)	Settling Time (s)		Overshoot/Undershoot (%)	
	FOSC	PI	FOSC	PI
0	0.08	0.22	4.4	8.85
0.3	0.07	0.18	2.14	4.28

Table 4. Comparative of THD source current for three cases.

Source Voltages and Currents		Phases	FOSC		PI	
			t < 0.3 s	*t* > 0.3 s	*t* < 0.3 s	*t* > 0.3 s
Source current before filtering	THD (%)	Ph-1	25.11	26.67	25.11	26.67
Balanced	THD (%)	Ph-1	0.85	0.77	1.32	2.12
Source voltages	Unbalanced	THD (%)	Ph-1	2.17	2.23	3.02	3.49
			Ph-2	2.27	2.33	2.90	3.31
			Ph-3	1.78	1.93	2.70	3.42
	Distorted	THD (%)	Ph-1	3.40	3.39	3.51	4.11
			Ph-2	3.44	3.49	3.41	4.17
			Ph-3	2.90	3.04	3.23	4.25

6. Conclusions

This article presents a novel nonlinear strategy for a three-level T-type-inverter-based SAPF using a fractional-order synergetic controller with a PLL technique to improve the system performance in terms of the harmonics and DC bus voltage tracking. The proposed control strategy was designed to possess good tracking and robustness to parameter

change. The simulation results demonstrate that the proposed nonlinear control can handle balanced, unbalanced, and distorted voltage conditions in the grid and provide a sinusoidal source current with low THD that meets the IEEE-519 requirements.

The obtained results showed that the main objectives imposed for the control strategy proposed here were fulfilled. Additionally, the performance of the proposed nonlinear control was compared to that of the traditional control, based on the PI controller, to highlight its effectiveness. The use of the suggested fractional-order synergetic control is a well-established and robust control technique, and the results obtained validate the expected outcomes.

The main contributions of the proposed control are as follows:

- Improves the quality of the current and power;
- Minimizes the THD value of the current;
- Improvesthe settling time and reduces errors compared to traditional PI control.

Thus, the application of this control approach for multi-level power converters in power systems is an exciting prospect.

In future research, the proposed work will be carried out experimentally and the results obtained will be confirmed. In addition, new approaches that combine different types of nonlinear controls will be researched and explored. For example, one potential technique is to combine back-part system control to improve the power quality and robustness of the SAPF.

Abbreviations

PI	Proportional-integral
NPC	Neutral point clamped
FOSC	Fractional-order synergetic controller
PLL	Phase-locked loop
PWM	Pulse width modulation
STF	Self-tuning filter
SMC	Sliding mode control
SAPF	Shunt Active Power Filter
THD	Total harmonic distortion
DPC	Direct power control
SVM	Space vector modulation
VOC	Vector oriented control
PCC	Point of common coupling
MV	Macro-variable
BC	Backstepping controller
SC	Synergetic control
FOPI	Fractional-order proportional-integral

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