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Comparison between a Cascaded H-Bridge and a Conventional H-Bridge for a 5-kW Grid-Tied Solar Inverter

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Abstract: This paper compares the cost and efficiency of two inverter topologies for a 5-kW grid-connected solar inverter application: the Conventional H-Bridge Inverter (CHB) and the Cascaded H-Bridge Multilevel Inverter (CHBMLI). Emphasis is put on power switches and passive elements with a detailed study of the losses. Both designs respect the same constraints (cost, efficiency, and junction temperature of the transistors) to ensure a fair comparison between both topologies. The work highlights the important parameters when choosing the components (MOSFETs, capacitors, and magnetic cores for the inductors). The DC-link voltage ripple and the output AC current ripple are the key parameters for the design of the passive elements (capacitors and inductors). On top of that, the transistors MOSFETs are chosen, in both topologies, to limit the conduction losses (by selecting the $R_{ds_{on}}$) and the switching losses (by selecting the Q_{rr} and dv/dt). Real components are picked in order to make the comparison as complete as possible. Numerical simulations are performed using the MATLAB platform. All equations and parameters are provided. A CHBMLI prototype was built with eight independent H-Bridges to validate the proposed design with thermal and efficiency measurements.

Keywords: Cascaded H-Bridge Multilevel Inverter; solar panel; grid-tied inverter; solar inverter; losses; efficiency; passive elements; output filter

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1. Introduction

The energy crisis issue due to the need to reduce CO_2 emissions and the shortage of fossil fuels has led most countries around the world to consider the use of renewable energy (solar PV (photovoltaics), wind power, hydropower, biopower) for electricity production. In 2019, over 200 GW of renewable energy was installed worldwide, including 120 GW of solar PV [1].

The PV inverter represents 10 to 15% of the total cost of a grid-connected PV system [2]. It is used to convert DC power from solar panels into AC power to be fed into the grid. Many solar inverter configurations can be defined [3–5]. Among them, the Central/Conventional H-Bridge Inverter (CHB) [6] and the Cascaded H-Bridge Multilevel Inverter (CHBMLI) [7] are studied in this paper. A Central H-Bridge Inverter usually consists of two power stages: a DC−DC boost converter as the front stage to get sufficient DC-bus voltage [8] and obtain a wider input voltage tracking range; and an inverter as the second stage to generate the AC utility line voltage. As an alternative to the boost DC−DC converter, a step-up transformer can be used to reach the grid voltage. This topology can reach peak efficiencies of up to 96% [9,10].

A cascaded inverter consists of several converters connected in a series, and it has many advantages in medium and large grid-connected PV systems [7,11–14]. In the CHBMLI topology, those converters are H-bridges. A DC−DC converter can be added between the solar panel and the H-bridge [15]. This helps to stabilize the voltage at the H-bridge from temperature and irradiation variations and to perform local Maximum Power Point

Tracking (MPPT) [16–18]. On top of that, due to its stair-shaped output waveform, the CHBMLI provides low switching voltages, which greatly reduces the output filter [19,20].

Furthermore, control techniques, such as Selective Harmonics Elimination Pulse Width Modulation (SHE-PWM), can be used to remove current harmonics and reduce the Total Harmonic Distortion (THD) [21]. As the Conventional H-Bridge Inverter switches higher voltages (∼400 V), the output filter is costly and bulky [6]. However, the CHBMLI requires more transistors and drivers than the conventional H-bridge.

In the literature, CHBMLI prototypes have been developed and studied [13,22]. However, the number of modules is often limited (up to 5), and the switching frequency is also limited (up to 4 kHz). Those prototypes are, thus, not suited for a grid-tied solar application on the 230 V AC main grid. Most solar inverters on the market are based on the conventional H-Bridge topology. In a previous paper, the authors have demonstrated that, with a specific hardware architecture, it is feasible to control a CHBMLI with at least 8 modules (and up to 20) with a switching frequency of 20 kHz [23]. The prototype was built using low-cost local electronics on each H-Bridge without the need for isolated measurements and isolated drivers compared to other prototypes presented in the literature [24,25]. The prototype developed by the authors makes the CHBMLI suitable for a grid-tied solar application on the 230 V AC main grid.

Even though both topologies are quite familiar in the literature, there are no studies comparing, in detail, the design of both converters in terms of size and complete cost of passive elements and MOSFETs, with a 20 kHz switch and a high number of modules.

The aim of this paper is to present a comparison of the standard H-Bridge Inverter and the CHBMLI for solar applications under the same sizing constraints. For the study, we consider an output power of 5 kW without DC−DC converters for both topologies. For both topologies, a series of constraints (Table 1) is applied to the waveforms and the overall efficiency. First, the passive elements (DC-link capacitor C_{PV} and output inductor L_{grid}) are designed based on the DC-link voltage ripple ΔV_{PV} and the output AC current ripple ΔI_{grid}. The value of ΔV_{PV} is set to 4% of the optimum DC-link PV voltage V_{MPPT} in both topologies. The impact of this voltage ripple on solar power extraction is detailed in Section 2. The value of ΔI_{grid} is set to 10% of the peak output grid current $I_{out}\sqrt{2}$. Furthermore, the MOSFETs and the drivers are both chosen to limit the conduction losses $P_{conduction}$ (by selecting the $R_{ds_{on}}$) and the switching losses $P_{switching}$ (by selecting the Q_{rr} and dv/dt). Each loss is limited to 1% of the nominal output power P_{out}. In both cases, the junction temperature $T_{junction}$ of MOSFETs is studied, and a heatsink is selected to limit this value to 100 °C. The values of V_{MPPT}, I_{out}, and P_{out} are presented in the next paragraph. Finally, based on those constraints, a series of comparisons are made in terms of cost, volume, and overall efficiency. Experimental measurements of the temperature rise, efficiency, and waveforms of the CHBMLI prototype are performed.

Table 1. Design constraints for both topologies.

Design Constraints	Name	Value	Component
DC-link Voltage Ripple	ΔV_{PV}	4% of V_{MPPT}	Capacitor C_{PV}
Output Current Ripple	ΔI_{Grid}	10% of I_{out}	Inductor L_{grid}
Conduction Losses	$P_{switching}$	1% of P_{out}	MOSFET + Driver
Switching Losses	$P_{conduction}$	1% of P_{out}	MOSFET
Junction temperature of the MOSFETs	$T_{junction}$	<100 °C	Heatsink

Solar module, grid, and inverter parameters used in this paper are presented in Table 2. The two topologies presented in this study use LR460HPH365M solar panels placed in a series. When operating without a boost converter, the voltage of all the panels placed in a series must be higher than the maximum grid voltage. A 10% tolerance is considered. Furthermore, for a given temperature, the optimum voltage decreases when solar irradiation decreases. However, for low irradiation (under 100 W/m^2), the output power is less sensitive to voltage variation around the optimum point. Thus, the voltage to

maximize the power extraction when the irradiation is 10% of the nominal one is chosen as the minimum voltage panel for the design. On top of that, an extra panel is added to improve the overall robustness. According to that, the following equation gives the number of solar panels required for a grid-tied inverter:

$$n = 1 + \frac{V_{grid} \cdot \sqrt{2} \cdot \left(1 + \Delta V_{grid}\right)}{V_{MPPT_{min}}} \approx 13 \quad (1)$$

where n is the number of solar panels, V_{grid} is the RMS grid voltage (V), ΔV_{grid} is the grid voltage tolerance (%) and $V_{MPPT_{min}}$ is the minimum voltage required to ensure MPPT at 100 W/m^2 and 25 °C (V).

Table 2. Solar module, grid, and inverter parameters.

Solar Module (LR460HPH365M)	**Name**	**Value**
Rated Power	P_{MPPT}	362 W
Optimum voltage (1000 W/m^2, 25 °C)	V_{MPPT}	34.1 V
Optimum voltage (100 W/m^2, 25 °C)	$V_{MPPT_{min}}$	30.7 V
Optimum current (1000 W/m^2, 25 °C)	I_{MPPT}	10.6 A
Open-circuit voltage	V_{oc}	41.1 V
Grid parameters	**Name**	**Value**
RMS Grid voltage	V_{grid}	230 V
Grid voltage tolerance	ΔV_{grid}	10%
Inverter parameters	**Name**	**Value**
Number of solar panels	N	13
Output power	P_{out}	4706 W
RMS Output current	I_{out}	20.46 A

Section 2 describes the design of the conventional H-Bridge based on parameters presented in Table 2. Section 3 applies the same design scheme as the CHBMLI. Section 4 gives a comparison between the two topologies. Section 5 presents the CHBMLI prototype and experimental measurements. Section 6 concludes the work.

2. Design of the Conventional H-Bridge

2.1. Main Characteristics

The H-Bridge is a well-known topology that converts DC into AC voltage [6,20]. The complete converter can be done with an H-Bridge driver and four N-channel MOSFETs. An inductor is used to filter the output grid current, and capacitors placed on the DC link limit the voltage ripple. For a 5-kW application, these passive elements represent an important part of the overall cost and volume of the converter. As for the semiconductors, power losses and temperature rise must be taken into account.

The conventional H-Bridge grid-tied solar inverter is shown in Figure 1. The DC side of the H-Bridge converter is powered by an array of $N = 13$ photovoltaic (PV) panels in series. The PV voltage V_{PV} is stabilized by the capacitor C_{PV} connected in parallel. The AC side of the H-Bridge converter is connected to the single-phase grid V_{grid} through an L filter. The output current I_{grid} of the PV array and the output voltage of the H-Bridge converter can, respectively, be described by Equations (2) and (3):

$$I_{PV}(t) = I_C(t) + I_H(t) = C_{PV} \cdot \frac{dV_{PV}(t)}{dt} + I_H(t) \quad (2)$$

$$V_H(t) = V_L(t) + V_{Grid}(t) = L_{Grid} \cdot \frac{dI_{Grid}(t)}{dt} + V_{Grid}(t) \quad (3)$$

where $I_{PV}(t)$ and $V_{PV}(t)$ are, respectively, the output current and the output voltage of the PV array. $I_H(t)$ and $V_H(t)$ are, respectively, the input current and output voltage of the H-Bridge converter. $I_c(t)$ is the current through the capacitor C_{PV}, $V_L(t)$ is the voltage across the inductor L_{Grid}. $I_{Grid}(t)$ and $V_{Grid}(t)$ are, respectively, the grid current and the grid voltage.

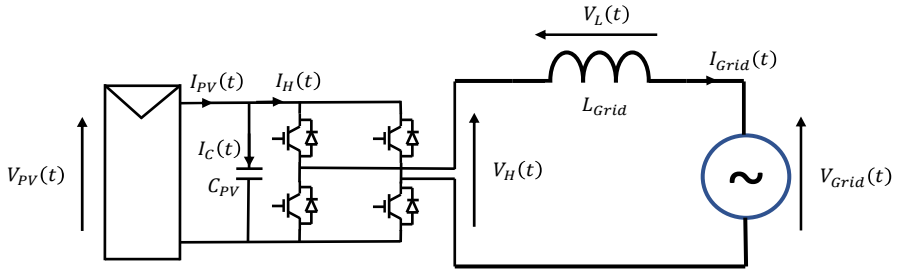


Figure 1. Configuration of the conventional H-Bridge grid-tied solar inverter.

In this paper, solar production is considered with a unity power factor. Thus, the grid current and grid voltage are in phase and are defined by Equations (4) and (5):

$$I_{Grid}(t) = I_{Grid} \cdot \sqrt{2} \cdot \sin(\omega_{Grid} \cdot t) \tag{4}$$

$$V_{Grid}(t) = V_{Grid} \cdot \sqrt{2} \cdot \sin(\omega_{Grid} \cdot t) \tag{5}$$

where $I_{Grid}(t)$ and $V_{Grid}(t)$ are, respectively, the grid RMS current and the grid RMS voltage. ω_{Grid} is the grid angular frequency.

2.2. Passive Elements

2.2.1. DC-Link Capacitor

The DC-link capacitor is the first passive element that needs to be properly sized. It is a compromise between volume/cost and voltage ripple on the DC side of the H-Bridge converter. The equation for sizing the capacitor is presented in [26]:

$$C_{PV} = \frac{I_{MPPT}}{2 \cdot \Delta V_{PV} \cdot \omega_{Grid}} \tag{6}$$

where I_{MPPT} is the optimum current (A), ΔV_{PV} is the 100 Hz voltage ripple (V) and ω_{grid} is the grid angular frequency (rad·s^{-1}).

When selecting the voltage ripple value ΔV_{PV}, it is important to consider its impact on PV power extraction. Figure 2 presents the evolution of the mean output power with the voltage ripple [23]. This figure was obtained considering the average output power of a single solar panel for a given voltage ripple around the optimum voltage and for a given solar irradiance. For the study conducted in this paper, we chose to limit the power drop to 1% of the Maximum Power Point. To achieve this, Figure 2 shows that the voltage ripple should not exceed 4%. To limit the voltage ripple to 4%, the filter capacitor must be at least:

$$C_{PV} \approx 950\ \mu\text{F} \tag{7}$$

For the capacitor voltage rating, a 30% tolerance is applied from the DC link optimal voltage. Thus, 600 V capacitors are used. Capacitors chosen for both topologies in this paper are TDK aluminum electrolytic capacitors. For 600 V capacitors, B43541 capacitors are considered. As 900 µF/600 V capacitors do not exist, several smaller capacitors are placed in parallel. Considering the characteristics of those capacitors, particularly their Equivalent Series Resistance (ESR), the design of the inverter must take into account the associated losses. It is important to notice that, in a power converter, the cost of the capacitors is proportional to the energy stored. Thus, for a given total capacitor and voltage values,

choosing many small capacitors has a similar cost as choosing a few big capacitors. Typical parameters of the capacitors are presented in Table 3.

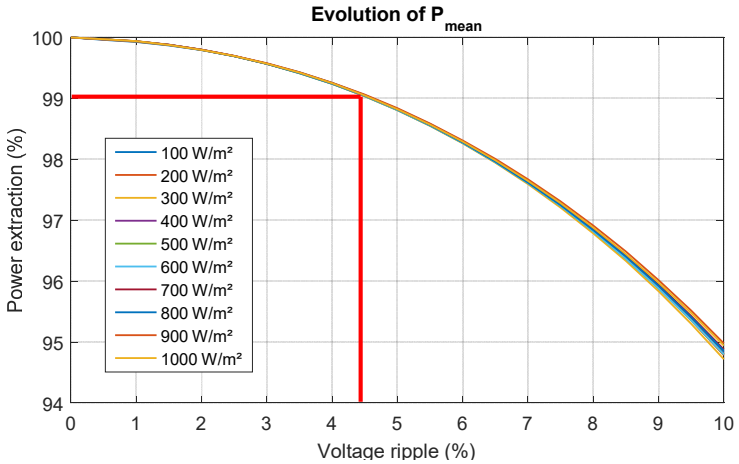


Figure 2. Power drop and voltage ripple [23].

Table 3. Capacitor parameters (TDK aluminum electrolytic, B43541).

Capacitor Value (100 Hz, 20 °C, µF)	Case Dimensions (mm)	ESR (100 Hz, 20 °C, mΩ)	Number of Capacitors in Parallel
47	25 × 25	2.47	21
56	25 × 30	2.07	17
68	25 × 35	1.70	14
82	25 × 35	1.42	12
100	25 × 40	1.16	10
120	25 × 50	0.97	8
150	25 × 55	0.77	7
180	30 × 45	0.64	6
220	30 × 55	0.53	5
270	35 × 50	0.43	4

The losses in the function of the capacitor value (equations are detailed further in the article) are shown in Figure 3. First, the figure shows that the total ESR (at $f_{sw} = 20$ kHz) of all capacitors placed in parallel for a given energy to store is independent of the number of parallel capacitors at the same global equivalent capacitor value: a high number of low-value capacitors or a low number of high-value capacitors. Indeed, for the same voltage rate, the ESR decreases as the capacitor value increases at the same rate. The second plot of Figure 3 highlights that whatever the configuration, total capacitor losses remain the same. However, losses per capacitor increase when the number of capacitors decreases. The temperature rise of each capacitor, which will greatly affect the lifespan of the inverter, increase when the number of capacitors decreases. Thus, 47 µF/600 V capacitors are the optimal choice, and 21 capacitors are placed in parallel. For both designs, the tolerance (20%) of the capacitor's value is not taken into account.

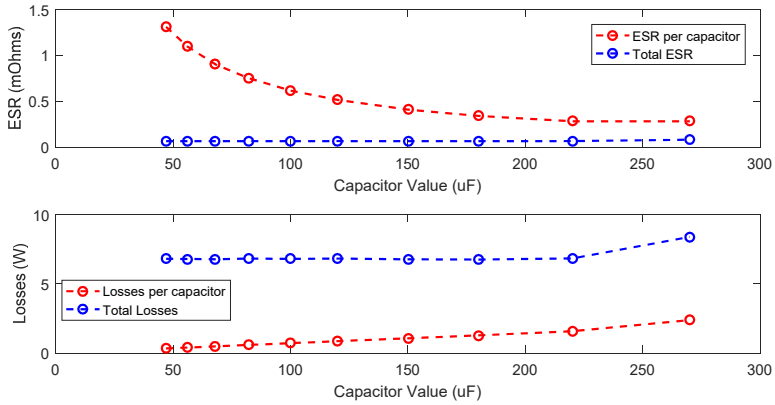


Figure 3. ESR and losses according to the capacitor value.

The capacitor losses are mostly due to the ESR.

$$P_{cap} = n_C \cdot R_C \cdot \left(\frac{I_{C_{RMS}}}{n_C} \right)^2 = \frac{R_C}{n_C} \cdot {I_{C_{RMS}}}^2 = 4.6\ W \tag{8}$$

where n_C is the number of capacitors placed in parallel ($n_C = 21$), R_C is the ESR at $f_{sw} = 20$ kHz of a single capacitor ($R_c = 1.3\ \Omega$) and $I_{C_{RMS}}$ is the RMS current through the capacitor at f_{sw}. Numerical simulations with MATLAB provide that: $I_{C_{RMS}} \approx 8.6$ A.

The capacitor losses lead to a temperature rise for each capacitor [27]:

$$\Delta T_c = \alpha \cdot \frac{P_{cap}}{\beta \cdot S \cdot n_c} = 12.7\ ^\circ\text{C} \tag{9}$$

where ΔT_c is the surface heat rise (°C), β is the heat radiation factor ($W^{-1} \cdot ^\circ\text{C} \cdot \text{cm}^2$) and $\beta = 0.0023 \times \text{S}^{-0.2}$, S is the surface area of the capacitor ($\approx$20 cm^2) and α is the factor of the temperature difference between the core and surface ($\alpha = 1.45$).

2.2.2. Output Inductor

The grid-tied solar inverter requires an output low-pass filter to eliminate the current ripple around the switching frequency. The values of the current ripple fundamental and its harmonics have to comply with the IEEE 1547 standards. The three main low-pass filters presented in the literature are the L-filter, the LC-filter, and the LCL-filter [28]. The LCL-filter is considered the most interesting due to its independence from the grid impedance and a better output response with the same inductance. However, designing such a filter has to consider many constraints, such as the resonance phenomenon or the capacitor's reactive power. As the aim of this paper is to compare two topologies, the same type of output filter is used. To ease the comparison, a classic L-filter will be designed for both topologies. It is important to note that elements of comparison (losses or size) are still relevant if an LC-filter or an LCL-filter is used for design.

The system has a unity power factor, and the control scheme adopted is a unipolar PWM. The inductance of the L-filter is given by the following formula [29]:

$$L_{Grid} = \frac{N \cdot V_{MPPT}}{4 \cdot \Delta I_{Grid} \cdot f_{sw}} = 1.9\ \text{mH} \tag{10}$$

where ΔI_{Grid} is the maximum current ripple (A) and f_{sw} is the switching frequency (Hz). The maximum current ripple is chosen as 10% of the peak-rated inverter current ($I_{out_{peak}} = 28.9$ A). A complete Fast Fourier Transform (FFT) analysis would normally be required to ensure that the grid-tied inverter complies with the IEEE 1547 standards for current harmonics. However, for comparison purposes, limiting the current ripple at the switching frequency is sufficient. Moreover, the switching frequency of a grid-tied solar

inverter with an output power of a few kW is often chosen within the range of 10 to 50 kHz. This choice is a compromise between the size of the output filter, the switching losses, the MCU performances, the leakage current etc. In this paper, the switching frequency (f_{sw}) is set to 20 kHz for both topologies.

The design of the inductor is done by using magnetic cores from the *Ferroxcube Data Handbook 2013* [30]. As there is no magnetic core big enough to design a 1.9 mH/30 A inductor, two 950 µH/30 A are placed in series. The magnetic core of a single inductor is made using two E cores with an air gap on both center legs, as presented in Figure 4. For a 20 kHz application, the 3C90 ferrite has the maximum saturation magnetic field (B_{sat} = 400 mT at T = 50 °C).

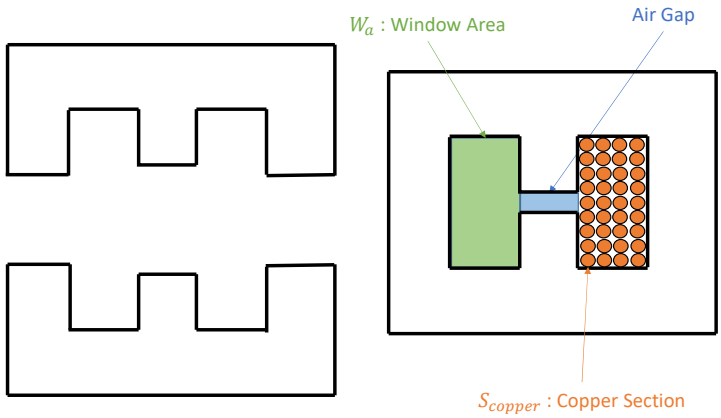


Figure 4. Magnetic core of the inductor.

In a 950 µH/30 A inductor, the energy stored W_{mag} (W) in the air gap is:

$$W_{mag} = \frac{1}{2} \cdot \frac{L_{Grid}}{2} \cdot I_{rms}^2 = 0.2 \text{ W} \tag{11}$$

The required air gap volume is:

$$V_{air\ gap} = \frac{2 \cdot W_{mag} \cdot \mu_0}{B_{sat}^2} \approx 3000 \text{ mm}^3 \tag{12}$$

where μ_0 is the vacuum permeability (H/m), B_{sat} is the saturation magnetic field of the chosen core (3C90).

The chosen magnetic core is E71/33/32 with a 3900 µm air gap. The effective area of the core is Ae = 683 mm^2. The datasheet of the core provides that the inductance factor is:

$$A_L = 315 \text{ nH}/turns^2 \tag{13}$$

The number of turns N_{turns} to reach a 950 µH inductance is:

$$N_{turns} = \sqrt{\frac{L_{grid}}{2 \cdot A_L}} \approx 55\ turns \tag{14}$$

Given that the wiring must fit within the window area of the magnetic core, the copper section (mm^2) is given by:

$$S_{copper} = \frac{W_a \cdot K}{N_{turns}} = 7 \text{ mm}^2 \tag{15}$$

where W_a is the window area (=569 mm^2) and K is the fill factor (=0.7). This copper section had no issue handling the 20.46 A_{rms} current.

The design of the coil must take into account the type of conductor chosen (litz wire or not). Indeed, for a cylindrical conductor with an alternating current, the current density

decreases exponentially from the surface toward the inside. This phenomenon, known as the skin effect, depends on the type of conductor and the frequency of the current [31]. It is characterized by the skin depth δ_θ at temperature θ, which must be higher than the radius of the conductor in order to minimize resistive losses.

$$\delta_\theta = \sqrt{\frac{p_\theta}{\mu_r \cdot \mu_0 \cdot \pi \cdot f}} \tag{16}$$

where p_θ is the resistivity (Ω·m) of the conductor at temperature θ, μ_r is the relative magnetic permeability of the conductor (1 for copper), μ_0 is the permeability of free space (H·m^{-1}) and f is the frequency of the current (Hz).

The copper resistivity depends on its temperature:

$$p_\theta = p_{\theta_0} \cdot (1 + \alpha_0 \cdot (\theta - \theta_0)) \tag{17}$$

where θ is the operating temperature (K), θ_0 is the reference temperature (K), α_0 is the temperature coefficient (K^{-1}), p_θ is the resistivity of the conductor at θ (Ω·m) and p_{θ_0} is the resistivity of the conductor at θ_0 (Ω·m).

For copper, $p_{20°C} = 1.68e^{-8}$ Ωm and $\alpha_0 = 4.04e^{-3}$ K^{-1}.

Thus:

$$p_{75°C} = 0.02 \ \mu\Omega\text{m} \tag{18}$$

$$\delta_{75°C} = \sqrt{\frac{p_{75°C}}{\mu_r \cdot \mu_0 \cdot \pi \cdot f}} = 10 \text{ mm} \tag{19}$$

The conductor used here has a much thinner radius (1.5 mm). There is no need to use litz wire for this application. Furthermore, the proximity effect is neglected in this topology due to the low frequency (50 Hz) of the AC current and the low RMS value of the high frequency (20 kHz) ripple (limited to 10% of the nominal current) [31].

Now that both the magnetic cores and the copper section have been designed, the copper and core losses of the two 950 µH inductors can be estimated:

$$\begin{aligned} P_{copper} &= 2 \cdot \frac{N_{turns} \cdot l_{turn} \cdot \rho_{copper}}{S_{copper}} \cdot I_{rms}^2 \\ &= 50 \text{ m}\Omega \times (20.46 \text{ A})^2 = 20.9 \text{ W} \end{aligned} \tag{20}$$

where l_{turn} is the average length of a turn (=160 mm) and ρ_{copper} is the copper resistivity (Ω·m) at 75 °C.

The core losses can be calculated as follow:

$$P_{core} = 2 \cdot P_{core_{20 \text{ kHz}}} = 2 \cdot V_e \cdot P_{density}(\Delta B, f_{sw}) \tag{21}$$

where $P_{core_{20kHz}}$ are the core losses (W) of the 20 kHz ripple curent ΔI_{grid}, V_e is the effective volume (m^3) of the magnetic core and $P_{density}(\Delta B, f)$ is the core losses density (kW/m^3) of the magnetic core for a given amplitude ΔB of the flux density B (T) and a given frequency f (Hz). The amplitude ΔB is calculated with the following formula [32]:

$$\Delta B = \frac{1}{2} \cdot \frac{\left(N \cdot V_{MPPT} - V_{grid}\right) \cdot \frac{V_{grid}}{N \cdot V_{MPPT}}}{N_{turns} \cdot A_e \cdot f_{sw}} = 73 \text{ mT} \tag{22}$$

The datasheet provides:

$$P_{density}(\Delta B, f) = k \cdot \Delta B^x \cdot f^y \tag{23}$$

With $x = 1.46$, $y = 2.75$ and $k = 57$.

Thus, the core losses are:

$$P_{core} = 700 \text{ mW} \tag{24}$$

The low core losses of the inductor are due to the low ripple current ΔI_{grid}. A higher ripple would lead to a higher amplitude of the flux density ΔB. The total losses in the inductor are:

$$P_{ind} = P_{copper} + P_{core} = 21.6 \text{ W} \quad (25)$$

The characteristics of passive elements for the conventional H-Bridge are summarized in Table 4.

Table 4. Conventional H-Bridge design.

Inverter Parameters	Name	Value	Reference	Series Resistance
L-Filter	L_{Grid}	1.9 mH/30 A	E71/33/32 (×4)	$R_L = 50$ mΩ
DC-link capacitor	C_{PV}	950 µF/600 V	B43541 (×21)	$R_c = 1.3$ Ω (of a single capacitor)
Switching frequency	f_{sw}	20 kHz		

2.3. MOSFET

The N-channel MOSFET chosen for this application must fulfill several requirements. First, a 25% tolerance is set for the maximum drain-to-source voltage based on the maximum DC-link voltage when all panels are at their open-circuit voltage. On top of that, a 25% tolerance is applied for the maximum drain current based on the maximum output current when all panels are at their optimum voltage under optimum weather conditions. Thus, the chosen MOSFET is at least a 650 V/35 A transistor.

In a grid-tied inverter with a conventional H-Bridge, the key power-loss contributors are the conduction losses, the switching losses, and the passive element (capacitors and inductors) losses. Indeed, the high maximum output current (∼30 A) contributes to the maximal conduction losses, and the high maximum DC-link voltage (∼500 V) contributes to the maximal switching losses. Most grid-tied solar inverters available on the market can reach a peak efficiency of around 97.5% at the nominal power level. For the design, it is decided that conduction and switching losses should not exceed 1% each of the total output power, and passive elements losses should not exceed 0.5% of the total output power. The efficiency at the nominal power point is thus set to be around 97.5%.

2.3.1. Conduction Losses

The conduction losses $P_{conduction}$ can be calculated using a MOSFET approximation with drain-source on-state resistance of R_{ds-on}. With a unipolar PWM, half of the transistors are on at any time. For each closed transistor, the complementary transistor is open. The conduction losses can be defined with the following formula:

$$P_{conduction} = 2 \cdot R_{ds-on} \cdot {I_{out}}^2 < 1\% \times P_{out} \quad (26)$$

Then R_{ds-on} (with a 100 °C junction temperature) is limited by the following equation:

$$R_{ds-on}(100\ ^\circ\text{C}) < 1\% \times \frac{P_{out}}{2 \cdot I_{out}^2} = 56 \text{ mΩ} \quad (27)$$

2.3.2. Switching Losses

The switching losses can be calculated as follow [33]:

$$P_{switching} = \left(E_{on_{MOSFET}} + E_{on_{Diode}} + E_{off_{MOSFET}} + E_{off_{diode}}\right) \cdot f_{SW} \quad (28)$$

where $P_{switching}$ are the switching losses, $E_{on_{MOSFET}}$ and $E_{off_{MOSFET}}$ are, respectively, the turn-on and turn-off energy for the MOSFET, $E_{on_{Diode}}$ and $E_{off_{Diode}}$ are, respectively, the turn-on and turn-off energy for the body diode during switching phases and f_{sw} is the switching frequency.

The worst-case turn-on losses in a power MOSFET can be calculated as the sum of the switch-on energy without considering the reverse recovery process and the switch-on energy caused by the reverse recovery of the freewheeling diode [33]:

$$E_{on_{MOSFET}} = N \cdot V_{MPPT} \cdot I_{rms} \cdot \frac{t_{rise\ I} + t_{fall\ V}}{2} + Q_{rr} \cdot N \cdot V_{MPPT} \tag{29}$$

where $t_{rise\ I}$ is the rising current time (s) and $t_{fall\ V}$ is the falling voltage time (s) during switching phase, Q_{rr} is the reverse recovery charge (C). The reverse recovery charge is selected for a 100 °C junction temperature and a dI_F/dt rating current of 100 A/µs. The datasheet of a transistor usually only provides the reverse recovery charge for a 25 °C junction temperature.

$$Q_{rr}\left(T_j = 100\ ^\circ\mathrm{C}\right) \approx 2 \cdot Q_{rr}\left(T_j = 25\ ^\circ\mathrm{C}\right) \tag{30}$$

The switch-off losses in the diode are normally neglected $\left(E_{off_{diode}} = 0\right)$ due to the low diode forward voltage compared to the DC-link voltage. The turn-on energy of the diode consists mostly of the reverse recovery energy:

$$E_{on_{Diode}} = \frac{1}{4} \cdot Q_{rr} \cdot N \cdot V_{MPPT} \tag{31}$$

The switch-off energy losses in the MOSFET can be calculated in the same way.

$$E_{off_{MOSFET}} = N \cdot V_{MPPT} \cdot I_{out} \cdot \frac{t_{fall\ I} + t_{rise\ V}}{2} \tag{32}$$

where $t_{fall\ I}$ is the falling current time (s) and $t_{rise\ V}$ is the rising voltage time (s) during switching phase.

By substituting (29), (31), and (32) into (28), the total switching losses are:

$$P_{switching} = N \cdot V_{MPPT} \cdot \left(\frac{I_{out}}{2} \cdot \left(t_{rise\ I} + t_{fall\ I} + t_{rise\ V} + t_{fall\ V} \right) + \frac{5}{4} \cdot Q_{rr} \right) \cdot f_{sw} \tag{33}$$

The rise time and fall time of the voltage are the only parameters that can be handled by external circuitry. Indeed, an external gate resistor is added between the driver and the gate of the MOSFET. It limits the noise and ringing in the gate drive path. However, increasing the rising and falling times leads to higher switching losses. On top of that, if transition times can no longer be neglected against the switching period $T_{sw} = 1/f_{sw}$, control issues may appear. For design purposes in this paper, the dv/dt of the transistor is limited to 4 V/ns:

$$t_{rise\ V} + t_{fall\ V} = 2 \cdot \frac{N \cdot V_{MPPT}}{dv/dt} = 221\ \mathrm{ns} \tag{34}$$

For information, the external gate resistor can be calculated based on the following equations [34]:

$$t_{fall\ V} = K_t \cdot \frac{C_{gd}(600\ \mathrm{V}) + C_{gd}(0\ \mathrm{V})}{2 \cdot (V_{driver} - V_{Miller})} \tag{35}$$

$$t_{rise\ V} = K_t \cdot \frac{C_{gd}(600\ \mathrm{V}) + C_{gd}(0\ \mathrm{V})}{2 \cdot V_{Miller}} \tag{36}$$

With:

$$K_t = \left(R_{gate}(ext) + R_{gate}(in)\right) \cdot \left(V_{MPPT} - R_{ds-on} \cdot I_{out}\right)$$

where $R_{gate}(ext)$ is the external gate resistor (Ω), $R_{gate}(int)$ is the internal gate resistor (Ω), V_{driver} is the voltage of the driver circuit (12 V), V_{Miller} is the Miller voltage (V), $C_{gd}(Voltage)$ is the gate-drain capacitor (F) for a given voltage (V).

2.3.3. MOSFET Choice

The transistor chosen for the conventional H-Bridge design that complies with these constraints is the NTHL040N65S3F. Table 5 provides the parameters of the NTHL040N65S3F that are used to calculate all remaining losses.

Table 5. Parameters of the NTHL040N65S3F.

Parameters of the NTHL040N65S3F			
$R_{ds-on_{100\ ^\circ C}} = 51\ m\Omega$	$Qrr_{100\ ^\circ C} = 1.5\ \mu C$	$V_{Miller} = 6.2\ V$	$Q_g = 158\ nC$
$t_{rise\ I} = 41\ ns$	$C_{gd}(400\ V) = 20\ pF$	$R_{gate}(int) = 2.4\ \Omega$	$V_{diode} = 1.3\ V$
$t_{fall\ I} = 29\ ns$	$C_{gd}(0\ V) = 2500\ pF$	$t_{Dr} = 41\ ns$	$C_{oss} = 140\ pF$
		$t_{Df} = 101\ ns$	

The conduction and switching losses are:

$$P_{conduction} = 43\ W \approx 1\%\ of\ P_{out} \tag{37}$$

$$P_{switching} = 43\ W \approx 1\%\ of\ P_{out} \tag{38}$$

The dead time losses depend on the body diode's forward voltage during phases when both transistors of a leg are off:

$$P_{deadtime} = V_{diode} \cdot I_{rms} \cdot \left(t_{Dr} + t_{Df}\right) \cdot f_{SW} = 70\ mW \tag{39}$$

where t_{D_r} and t_{D_f} are, respectively, the rising dead time (s) and falling dead time (s).

In unipolar PWM, gate charge losses for all the transistors are provided by the H-Bridge driver:

$$P_{gate} = 2 \cdot Q_g \cdot V_{driver} \cdot f_{sw} = 76\ mW \tag{40}$$

where Q_g is the gate charge (C).

The parasitic capacitance C_{oss} of the MOSFET is also responsible for extra losses:

$$P_{C_{oss}} = 2 \times \left(\frac{1}{2} \cdot C_{oss} \cdot (N \cdot V_{MPPT})^2 \cdot f_{sw}\right) = 550\ mW \tag{41}$$

Approximately 3 W (including the gate charge losses) are necessary for the control side of the converter (microcontroller, sensors, and relays):

$$P_{IC} = 3\ W \tag{42}$$

3. Design of the Cascaded H-Bridge Multilevel Inverter

3.1. Main Characteristics

The CHBMLI topology consists of several H-Bridge converters in a series. Each DC link is fed by a single solar panel. A capacitor, placed in parallel with the panel, is required to store the energy during phases when the H-Bridge's module output is bypassed [13]. The topology is presented in Figure 5.

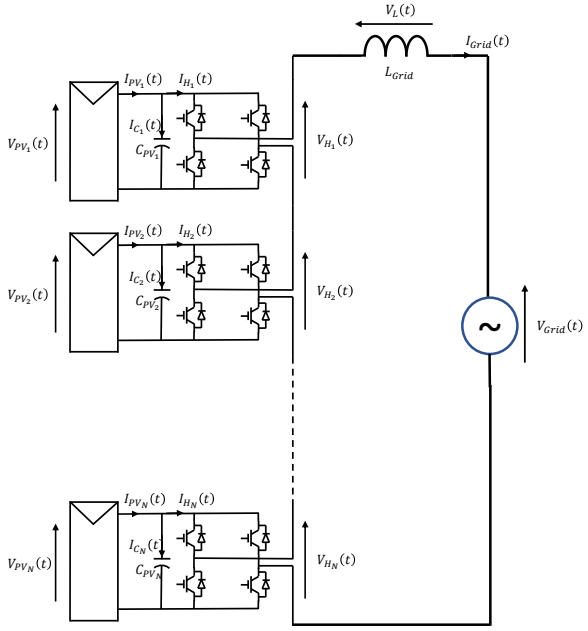


Figure 5. Cascaded H-Bridge Multilevel Inverter (CHBMLI) configuration.

3.2. Passive Elements

3.2.1. DC-Link Capacitor

The process of selecting the capacitor value is based on limiting the voltage ripple to 4% (the same limit as for the conventional H-Bridge). On the multilevel topology, the voltage ripple ΔV_{PV} is calculated from the voltage of a single solar panel at MPP (Maximum Power Point): $\Delta V_{PV} = 4\% \times V_{MPPT}$. The value of the capacitor per H-Bridge is calculated with the following formula:

$$C_{PV} = \frac{I_{MPPT}}{2 \cdot \Delta V_{PV} \cdot \omega_{Grid}} = 12.4 \text{ mF} \tag{43}$$

For 50 V capacitors, B41505 capacitors are considered (aluminum electrolytic capacitors from TDK). The capacitor C_{PV} is made by paralleling four 3300 µF capacitors ($n_c = 4$).

The capacitor losses are mostly due to the ESR. The total capacitor losses are the sum of the capacitor losses per H-Bridge. On top of that, the ESR of those capacitors is estimated with an RMS capacitor current $I_{C_{rms}}$ at the switching frequency $f_{sw} = \frac{20 \text{ kHz}}{N} = 1.5$ kHz of each H-Bridge.

$$P_{cap} = N \cdot \left(\frac{R_c}{n_C} \cdot I_{rms}^2 \right) = 8.7 \text{ W} \tag{44}$$

where R_C is the total ESR of the four ($n_C = 4$) capacitors at $f_{sw} = 1.5$ kHz ($R_c = 36$ mΩ) and $I_{C_{RMS}}$ is the RMS current through the capacitor. Numerical simulations with MATLAB provide that: $I_{C_{RMS}} \approx 8.6$ A.

The capacitor losses lead to a temperature rise for each capacitor:

$$\Delta T_c = \alpha \cdot \frac{P_{cap}}{\beta \cdot S \cdot n_c \cdot N} = 6.9 \text{ °C} \tag{45}$$

where ΔT_c is the surface heat rise (°C), β is the heat radiation factor $\left(\text{W}^{-1} \cdot \text{°C} \cdot \text{cm}^2 \right)$ and $\beta = 0.0023 \times S^{-0.2}$, S is the surface area of the capacitor (≈30 cm^2) and α is the factor of the temperature difference between the core and surface ($\alpha = 1.45$).

3.2.2. Output Inductor

As for the conventional H-Bridge, the switching frequency of the converter is set to 20 kHz, and the current ripple is chosen as 10% of the rated inverter current. The inductor is calculated by using the following equation:

$$L_{Grid} = \frac{V_{MPPT}}{4 \cdot \Delta I_{Grid} \cdot f_{sw}} = 147\ \mu\text{H} \tag{46}$$

The design of the inductor is done by using magnetic cores from the *Ferroxcube Data Handbook 2013*. As for the two inductors of the conventional H-Bridge, the magnetic core is made using two E cores with an air gap between both center legs. As for the design of the inductor in the conventional H-Bridge, a 3C90 ferrite is used.

In a 147 µH/30 A inductor, the energy stored W_{mag} (W) in the air gap is:

$$W_{mag} = \frac{1}{2} \cdot L_{Grid} \cdot I_{rms}^2 = 0.031\ \text{W} \tag{47}$$

The required air gap volume is:

$$V_{air\ gap} = \frac{2 \cdot W_{mag} \cdot \mu_0}{B_{sat}^2} \approx 400\ \text{mm}^3 \tag{48}$$

The chosen magnetic core is E42/33/20 with a 1540 µm air gap to reach the proper air-gap volume. The effective area of the core is $Ae = 236\ \text{mm}^2$. The datasheet of the core provides that the inductance factor is:

$$A_L = 250\ \text{nH}/turns^2 \tag{49}$$

The number of turns N_{turns} for a 147 µH inductance is:

$$N_{turns} = \sqrt{\frac{L_{Grid}}{A_L}} \approx 25 turns \tag{50}$$

Given that the wire must fit within the window area (=450 mm^2) of the magnetic core, the copper section (mm^2) is given by:

$$S_{copper} = \frac{W_a \cdot K}{N_{turns}} = 12.6\ \text{mm}^2 \tag{51}$$

Now that both the magnetic cores and the copper section have been designed, the copper and core losses can be estimated:

$$\begin{aligned} P_{copper} &= \frac{N_{turns} \cdot l_{turn} \cdot \rho_{copper}}{S_{copper}} \cdot I_{rms}^2 \\ &= 4\ \text{m}\Omega \times (20.46\ \text{A})^2 = 1.67\ \text{W} \end{aligned} \tag{52}$$

The core losses can be calculated as in Section 2. The low ripple current leads to a low amplitude of the flux density at 20 kHz ($\Delta B = 10$ mT). This leads to a very low power loss density of the magnetic core. On top of that, the volume of the inductance is also very low. Thus, the core losses are neglected:

$$P_{core} \approx 0\ \text{W} \tag{53}$$

The total inductor losses are:

$$P_{ind} = P_{copper} + P_{core} = 1.67\ \text{W} \tag{54}$$

The characteristics of the chosen topology and its passive elements are summarized in Table 6.

Table 6. Cascaded H-Bridge Multilevel Inverter design.

Inverter Parameters	Name	Value	Reference	Series Resistance
L-Filter	L_{Grid}	147 µH/30 A	E42/33/20 (×2)	$R_L = 4$ mΩ
DC-link capacitor	C_{PV}	12.4 mF/50 V	B41505 (4 in parallel per module, 52 in total)	$R_c = 36$ mΩ (ESR of a single capacitor)
Switching frequency	f_{sw}	20 kHz		

3.3. MOSFET

For the N-channel MOSFET design, and as for the conventional H-Bridge, a 25% tolerance is applied on the maximum drain to source voltage and the maximum drain current. Thus, the chosen MOSFET is at least a 50 V/35 A transistor.

As for the design of the conventional H-Bridge, it is set that conduction and switching losses should not exceed 1% of the total output power, and passive element losses should not exceed 0.5% of the total output power.

3.3.1. Conduction Losses

Given the fact that N H-Bridge converters are used in the CHBMLI instead of only one for the conventional H-Bridge under standard conditions, the current is passing through half the transistors of each H-Bridge. The limit for conduction losses is based on the following equation:

$$P_{conduction} = 2 \cdot N \cdot \left(R_{ds-on} \cdot I_{out}^2 \right) < 1\% \times P_{out} \tag{55}$$

Then R_{ds-on} (with a 50 °C junction temperature) is limited by:

$$R_{ds-on}(50\ ^\circ\text{C}) < 1\% \times \frac{P_{out}}{2 \cdot I_{out}^2 \cdot N} = 4\ \text{m}\Omega \tag{56}$$

3.3.2. Switching Losses

The full system switching losses are expressed by the following equation:

$$P_{switching} = N \cdot \left(V_{MPPT} \cdot \left(\frac{I_{out}}{2} \cdot t + \frac{5}{4} \cdot Q_{rr} \right) \cdot \frac{f_{sw}}{N} \right) \tag{57}$$

$$t = t_{rise\ I} + t_{fall\ I} + t_{rise\ V} + t_{fall\ V} \tag{58}$$

On average, each H-Bridge switches around f_{sw}/N times per second.

3.3.3. MOSFET Choice

The transistor chosen for the CHBMLI that complies with these constraints is the DMTH6004SK3. Table 7 provides the parameters of the DMTH6004SK3 that are used to calculate all the remaining losses.

Table 7. Parameters of the DMTH6004SK3.

Parameters of the DMTH6004SK3			
$R_{ds-on_{50\ ^\circ C}} = 3.8\ m\Omega$	$Q_{rr_{50\ ^\circ C}} = 120\ nC$	$V_{Miller} = 4.5\ V$	$Q_g = 95\ nC$
$t_{rise\ I} = 11.7\ ns$	$C_{gd}(40\ V) = 40\ pF$	$R_{gate}(int) = 660\ m\Omega$	$V_{diode} = 0.9\ V$
$t_{fall\ I} = 12\ ns$	$C_{gd}(0\ V) = 1\ nF$	$t_{Dr} = 13\ ns$	$C_{oss} = 1383\ pF$
		$t_{Df} = 31\ ns$	

The conduction and switching losses are:

$$P_{conduction} = 42\ W \approx 1\%\ of\ P_{out} \tag{59}$$

$$P_{switching} = 5\ W \approx 0.1\%\ of\ P_{out} \tag{60}$$

The dead time losses depend on the body diode's forward voltage during phases when both transistors of a leg are off:

$$P_{deadtime} = N \cdot \left(V_{diode} \cdot I_{rms} \cdot \left(t_{Dr} + t_{Df} \right) \cdot \frac{f_{SW}}{N} \right) = 21\ mW \tag{61}$$

In unipolar PWM, gate charge losses for all the transistors are provided by the H-Bridge driver:

$$P_{gate} = 2N \cdot \left(Q_g \cdot V_{driver} \cdot \frac{f_{sw}}{N} \right) = 590\ mW \tag{62}$$

The parasitic capacitance C_{oss} of the MOSFET is also responsible for extra losses:

$$P_{C_{oss}} = 2N \cdot \left(\frac{1}{2} \cdot C_{oss} \cdot V_{MPPT}^2 \cdot \frac{f_{sw}}{N} \right) = 410\ mW \tag{63}$$

Approximately 300 mW (including the gate charge losses per H-Bridge) are necessary for the control side of each converter (microcontroller, sensors, communication), and 3 W are necessary for the Master control of the full converter (microcontroller, communication, and relays):

$$P_{IC} = N \times 300\ mW + 3\ W = 6.90\ W \tag{64}$$

4. Discussion

The aim of this section is to compare the design of the two converters in terms of size and cost for the passive elements on the basis of simulations. Efficiencies of both converters are also assessed for the full range of output power. Finally, the costs of MOSFETs (+driver and heatsink) for both converters are compared. Simulations of both topologies are performed under the MATLAB/SIMULINK platform.

4.1. Circuit Simulations

The waveforms of both converters are shown in Figure 6. The parameters used for the two simulations are presented in Table 2. The multilevel ability of the CHBMLI offers much more possibilities in terms of reducing the harmonics than the Conventional H-Bridge [35]. However, the comparison made in this study only considers the grid current ripple and neglects the harmonics in order to use the control algorithm for the CHBMLI presented by the authors in a previous study [36], as these algorithms do not yet include specific harmonics elimination. Several control algorithms, such as Selective Harmonics Elimination Pulse Width Modulation (SHE-PWM), can be used to remove current harmonics and reduce Total Harmonic Distortion (THD) [21]. Conventional control with integrated control loops [37] is used for the Conventional H-Bridge (CHB) with a unipolar PWM.

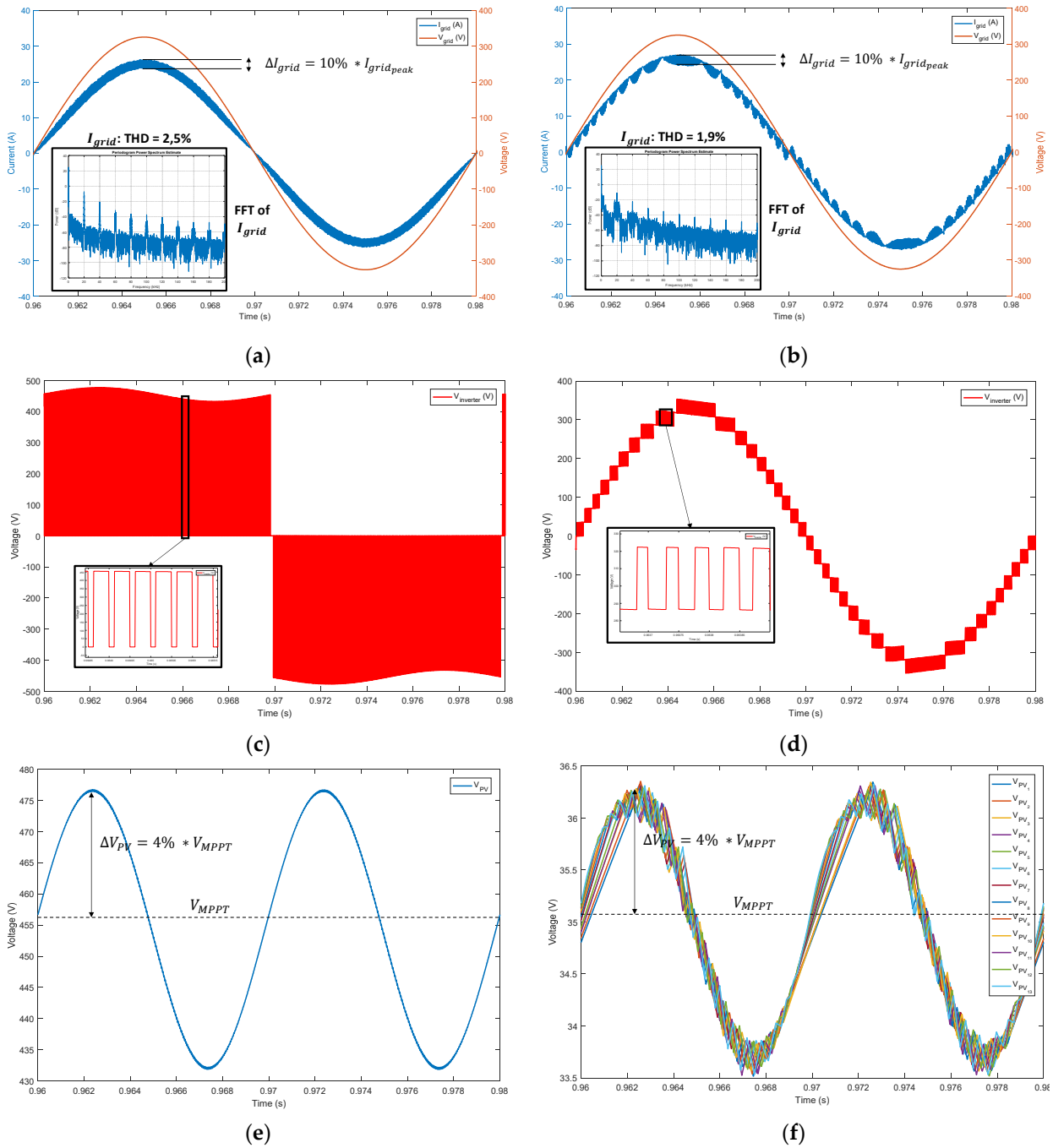


Figure 6. (**a**) Grid Voltage (red) and Grid Current (blue) for the CHB (**b**) Grid Voltage (red) and Grid Current (blue) for the CHBMLI (**c**) Inverter Voltage (red) for the CHB (**d**) Inverter Voltage (red) for the CHBMLI (**e**) PV Voltage for the CHB (blue) (**f**) PV Voltages for the CHBMLI.

The Conventional H-Bridge (CHB) and the CHBMLI both have a maximum output current ripple ΔI_{grid} limited to 10% of the peak output current $I_{grid_{peak}}$ (Figure 6a,b), which validate the design of both inductors. Furthermore, for both simulations, the current (blue) is set in phase with the grid voltage (red). The THD of the CHBMLI (1.9%) is slightly lower than the THD of the CHB (2.5%). This is due to the control algorithm that mitigates some harmonics. However, the THD of the CHBMLI could be further improved by using Selective Harmonics Elimination [21]. The output waveform of both inverters is presented in Figure 6c for the CHB and Figure 6d for the CHBMLI. The CHB has a three-level output voltage with high switching voltages (∼450 V), and the CHBMLI has a stair-shaped output

waveform with low switching voltages (∼34 V). The waveform of the CHBMLI, almost sinusoidal, visually explains why the inductor is much lower for a similar grid current ripple than the CHB. Finally, both converters have an identical DC-link voltage ripple ΔV_{PV} limited to 4% of the optimal voltage V_{MPPT} (Figure 6e,f), which validates the design of both capacitors. In the case of the CHBMLI, the converter regulates each DC-link voltage of the N modules around V_{MPPT} with the same ripple ΔV_{PV}. The waveforms of the DC-link voltages of the CHBMLI are not as sinusoidal as the one of the CHB, because the average switching frequency of each module is f_{sw}/N.

4.2. Passive Elements

Elements of comparison for the design and the choice of the capacitor are presented in Table 8.

Table 8. Comparison of the capacitor design.

Topology	Capacitance per H-Bridge	Number of Capacitor	Capacitor Losses
Conventional H-Bridge	950 µF/600 V	21	4.5 W
CHBMLI	12.3 mF/50 V	52	8.8 W

For the conventional H-Bridge, the amount of stored energy (E_{stored}) to limit the ripple voltage ΔV on the DC-link voltage is:

$$E_{stored} = \frac{1}{2} \cdot (950\ \mu\text{F}) \cdot (N \cdot V_{MPPT})^2 = 93\ \text{J} \tag{65}$$

For the CHBMLI:

$$E_{stored} = N \times \frac{1}{2} \cdot (12.3\ \text{mF}) \cdot (V_{MPPT})^2 = 93\ \text{J} \tag{66}$$

The same amount of energy needs to be stored under both voltages because in both topologies, the global input DC power and the global output AC power are identical. The cost of capacitors is proportional to the energy stored E_{stored}. From that perspective, the CHBMLI has no direct advantages compared to the conventional H-Bridge regarding the cost and volume of the DC-link capacitors.

The capacitor choice for both topologies is presented in Table 8. For the CHBMLI, the required capacity can be divided into up to 52 capacitors. For the conventional H-Bridge, 21 capacitors (47 µF/600 V) are placed in parallel. The capacitor losses are higher on the CHBMLI topology because the RMS current per H-Bridge has a lower frequency ($\frac{f_{sw}}{N} = 1.5$ kHz) than the RMS current on the H-Bridge of the conventional H-Bridge Inverter. As the ESR of a capacitor decrease with the frequency, the global capacitor ESR in a CHBMLI is higher than the global capacitor ESR in a conventional H-Bridge. However, the extra losses in the CHBMLI are very low compared to the other losses (conduction, switching, inductor). On top of that, the temperature rise (12 °C for the CHBMLI compared to 7 °C for the conventional H-bridge) of each capacitor is very low. As a result, the lifespan expectancy will not be affected by those losses.

The inductor choice for both topologies is presented in Table 9. The value of the inductor is proportional to the switched voltage ($N \cdot V_{MPPT}$ for the conventional H-Bridge and V_{MPPT} for the CHBMLI). The use of N low voltage modules in a CHBMLI leads to a reduction of the inductor's value by a factor of N. Cost and volume are proportional to the value of the inductor at the same current value. Thus, a much cheaper and lighter inductor is used for the CHBMLI at the same current ripple. The volume (and the price) of the magnetic core of the inductor of the CHBMLI is reduced by almost a factor of N. On top of that, the volume (and cost) of the copper for the CHBMLI inductor is also reduced by almost a factor of N. This leads to low copper losses due to a very low ESR of the inductor

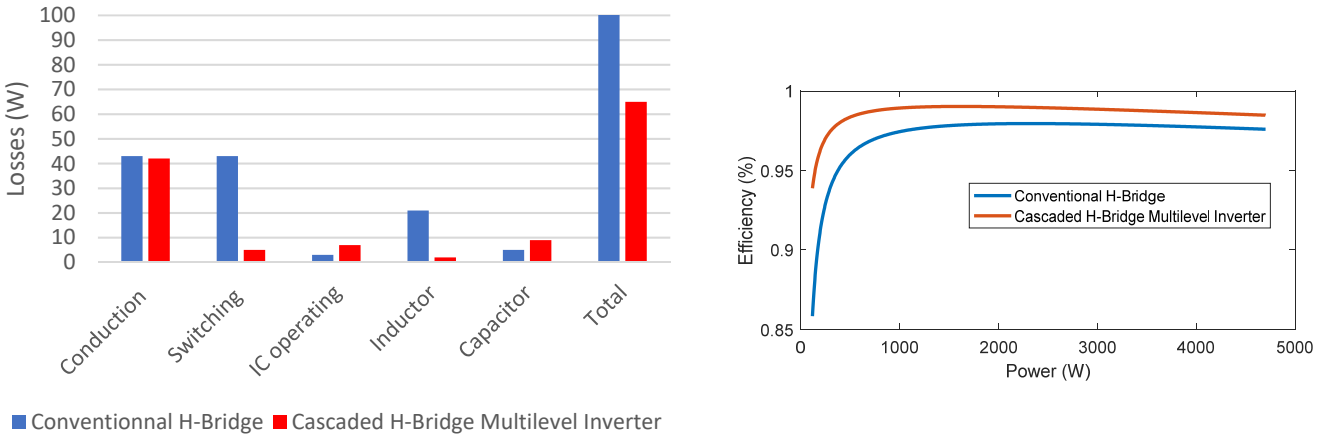
(4 mΩ for the CHBMLI and 50 mΩ for the conventional H-Bridge)—the low output current ripple leads, in both topologies, to reduced core losses. As a result, the inductor losses and the cost of this output filter in a CHBMLI are both very low.

Table 9. Comparison of the inductor design.

Topology	Inductor	Magnetic Core	Inductor Losses (P_{ind})
Conventional H-Bridge	1.9 mH/30 A	E71/33/32 (×4)	21.6 W
CHBMLI	147 µH/30 A	E42/33/20 (×2)	1.67 W
Topology	**Copper Cost (weight)**	**Magnetic Core Cost**	**Total cost**
Conventional H-Bridge	$21.2 (2.28 kg)	$48	$69.2
CHBMLI	$2.5 (0.27 kg)	$3.4	$6.0

4.3. Power Losses and Efficiency

The loss comparison between the conventional H-Bridge and the CHBMLI is shown in Figure 7a. The switching losses for the CHBMLI are much lower. Indeed, switching low voltages combined with the use of transistors that have a much lower reverse recovery charge (due to their low voltage rating) leads to a reduction by almost a factor of 10 of the switching losses. The conduction losses in both topologies are similar because both transistors were chosen as such. The CHBMLI requires more IC operating power than the unique control board of the conventional H-Bridge. It has been estimated in this case that the amount of power required is double. However, it does not affect the overall efficiency due to its low value. Inductor and capacitor losses have already been discussed.



(**a**) (**b**)

Figure 7. (**a**) Losses distribution comparison at maximum output power (**b**) Efficiency comparison.

The efficiency of both converters in the function of the total output power is shown in Figure 7b. The CHBMLI has better efficiency than the conventional H-Bridge for any output power. Overall, the key factors that contribute to the better efficiency of the CHBMLI are reduced switching and inductor losses. The reduced losses both come from the low switching voltages of the CHBMLI due to its multilevel ability. At low output power (<100 W), the efficiencies of both converters are affected by their IC operating losses because they remain constant regardless of the output power. As the power increases, the efficiency increases as well because the IC operating losses become negligible. Around 1500 W, both converters reach their peak efficiencies: 98.2% for the conventional H-Bridge and 99% for the CHBMLI. From that point, efficiencies decrease due to conduction and inductor losses. Indeed, unlike other losses, they are proportional to I_{out}^2 (when P_{out} is proportional to I_{out}). At 4700 W, the efficiency of the conventional H-Bridge is 97.9%, and the efficiency of the CHBMLI is 98.4%. For any output power, the efficiency of the CHBMLI is at least superior to the efficiency of the conventional H-Bridge by 0.5%.

4.4. MOSFETs

4.4.1. Temperature Rise

Limiting the temperature rise is then a trade-off between the size and cost of the heatsink and MOSFETs lifespan and losses. A proper comparison of the transistors must be made by considering the same temperature rise. The losses per transistor in both topologies are:

$$P_{Total\,MOSFET} = P_{conduction} + P_{switching} \tag{67}$$

$$\left(Losses_{perMOSFET}\right)_{CHBMLI} = \left(\frac{P_{Total\,MOSFET}}{4N}\right)_{CHBMLI} = \frac{46.4\text{W}}{4\text{N}} = 890\ \text{mW} \tag{68}$$

$$\left(Losses_{perMOSFET}\right)_{HB} = \left(\frac{P_{Total\,MOSFET}}{4}\right)_{HB} = \frac{84.6\ \text{W}}{4} = 21.1\ \text{W} \tag{69}$$

First, for the CHBMLI with maximum output power, the temperature rise of each transistor without any heatsink is:

$$\Delta T_{MOSFET_{CHBMLI}} = \left(Losses_{perMOSFET}\right)_{CHBMLI} \times R_{j-a} = 36\ ^{\circ}\text{C} \tag{70}$$

where R_{j-a} is the junction-to-ambient thermal resistance ($R_{j-a} = 40$ K/W). In a converter design, the junction temperature of a transistor is usually limited to 100 °C. A 36 °C temperature rise at maximum output power is perfectly acceptable for a solar inverter. No heatsink is required for the CHBMLI. For the conventional H-Bridge with maximum output power, the temperature rise of each transistor without any heatsink is:

$$\Delta T_{MOSFET_{HB}} = \left(Losses_{perMOSFET}\right)_{HB} \times R_{j-a} = 846\ ^{\circ}\text{C} \tag{71}$$

This high temperature rise is caused by complete losses distributed on a reduced number of transistors. On top of that, due to lower efficiency, the total transistors losses are higher for the conventional H-Bridge. Finally, compared to the CHBMLI, each transistor dissipates significantly more energy. In this case, a heatsink is required. We chose to use a single heatsink on which all the transistors are fixed. The value of the heatsink is calculated to limit the junction temperature to $T_{junction_{lim}} = 100$ °C, which means a temperature rise of 75 °C from an ambient temperature of 25 °C:

$$\Delta T_{MOSFET_{HB}} = \left(Losses_{perMOSFET}\right)_{HB} \times \left(R_{j-c} + R_{c-h} + 4{\cdot}R_h\right)_{HB} = 75\ ^{\circ}\text{C} \tag{72}$$

where R_{j-c} is the junction-to-case thermal resistance (0.5 K/W), R_{c-h} is the case-to-heatsink thermal resistance (0.5 K/W) and R_h is the required heatsink thermal resistance (K/W).

Then:

$$R_h = \frac{1}{4}\left(\frac{\Delta T_{MOSFET_{CHBMLI}}}{\left(Losses_{perMOSFET}\right)_{HB}} - R_{j-c} - R_{c-h}\right) \tag{73}$$

Thus:

$$R_h = 0.6\ \text{K/W} \tag{74}$$

The chosen heatsink is a 0.6 K/W heatsink from ABL components (109AB1500B, $14).

4.4.2. Gate Drivers

The selected MOSFET drivers for the conventional H-Bridge are two UCC21520 Isolated Dual-Channel Gate Drivers. These drivers are designed to power MOSFETs with a very low propagation delay (typically 19 ns) and a high common-mode transient immunity (up to 100 V/ns). On each driver, both channels are fully isolated and are guaranteed to operate with a DC voltage up to 1500 V.

For the CHBMLI, a unique H-bridge driver is used: the MIC4606. This driver also has a very low propagation delay (typically 35 ns) and very low power consumption. It uses

a bootstrap circuit to supply the two high-side transistors per H-Bridge up to a maximal voltage of 80 V. Those drivers do not need to be isolated because they are directly powered by the solar panel (through a small local power supply).

4.4.3. Overall Cost

The overall cost for the MOSFETs (including the drivers and the heatsink) is presented in Table 10. The CHBMLI uses N times more transistors than the conventional H-Bridge. However, those transistors are much cheaper due to their low voltage characteristics and compact packages. The addition of drivers (more expensive for the CHBMLI) makes the cost (MOSFETs + driver) similar between the two topologies. In the end, the need for a heatsink for the conventional H-Bridge leads to a higher overall cost (for the MOSFETs part) than for the CHBMLI.

Table 10. MOSFETs + Driver + Heatsink.

	Conventional H-Bridge			**CHBMLI**		
	Reference	Number	Cost	Reference	Number	Cost
MOSFETs	NTHL040N65S3F	4	$44	DMTH6004SK3	52	$27
Driver	UCC21520	2	$6	MIC4606	13	$28
Heatsink	109AB1500B	1	$17			
Total			**$67**			**$45**

This paragraph does not take into account the cost of the other components in the complete converter (AOP for measurements, microcontroller, onboard power supply). It is expected that, when adding the total cost of every component of the circuit, the CHBMLI might not keep its advantage.

4.5. Summary

All the comparison points of this section are summed up in Table 11.

Table 11. Summary of comparison points between both topologies.

	Conventional H-Bridge	**CHBMLI**
MOSFETs-Conduction Losses	43 W	43 W
MOSFETs-Switching Losses	43 W	5 W
Temperature rise per MOSFET	75 °C	36 °C
Cost of MOSFETs (+driver + heatsink)	$67	$45
Capacitor-Losses	4.5 W	8.5 W
Inductor-Losses	21.6 W	1.7 W
Inductor-Cost	$69.2	$6.0
Peak efficiency	98.2%	99.0%

5. Experimental Measurements for the CHBMLI

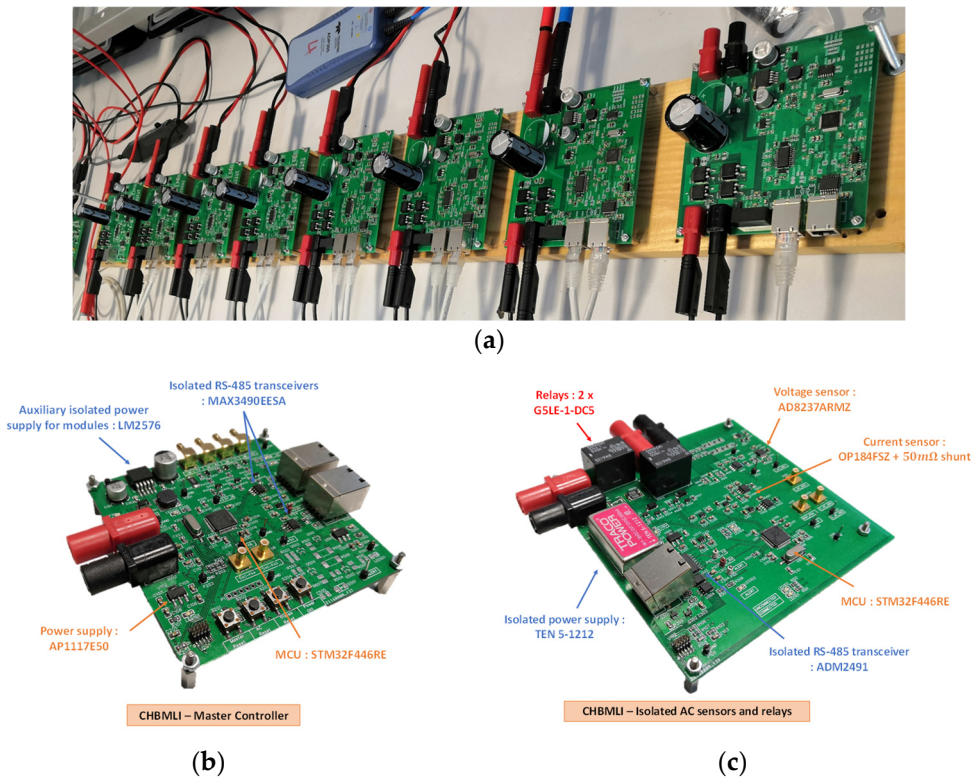
The objective of this section is to validate the thermal design of the CHBMLI through a temperature measurement on a real prototype. Only the CHBMLI prototype was built to limit the time and resources required. Furthermore, due to limited equipment, this validation is performed by measuring the efficiency and temperature of a single module operating at its rated power (365 W). For this purpose, a sinusoidal four-quadrant power supply (TOE7610) is used on the output, while a DC power source (Cpx400D) is used on the input. On the other hand, a prototype composed of eight modules used at a lower power is tested to provide the inverter waveforms, such as the inverter voltage $V_{inverter}$, the module output voltage V_H and the output grid current I_{grid}.

The control of the converter was detailed in previous work by the authors. First, it was demonstrated that it is possible to control the CHBMLI with a hardware architecture having up to 20 modules with a switching frequency of 20 kHz [36]. A second paper detailed how this topology can be controlled with a reduced number of sensors [23] while

operating, for each solar panel, an individual Maximum Power Point Tracking (MPPT) algorithm with minimum power oscillations. Those papers demonstrate that the CHBMLI can be controlled with low-cost components while maintaining a wide range of operations (number of modules > 20).

5.1. Experimental Setup

The experimental setup for the CHBMLI is presented in Figure 8. Figure 8a presents the prototype of the CHBMLI with 8 H-Bridge modules with all the output placed in series, Figure 8b presents the master controller of the inverter with the main MCU (STM32F446RE), and Figure 8c presents the circuit with isolated AC voltage and current sensors and relays to connect the inverter to the grid. This setup was designed according to the elements detailed in Section 3.



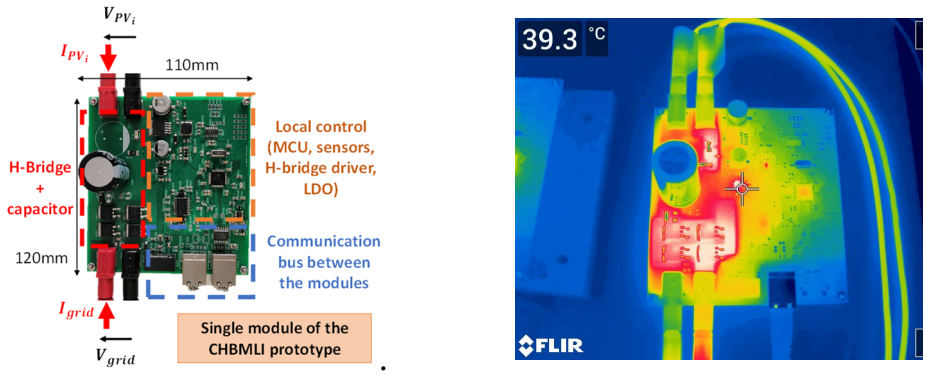
(**a**)

(**b**) (**c**)

Figure 8. (**a**) Experimental setup of the Cascaded H-Bridge Multilevel Inverter with eight modules (**b**) Master controller of the CHBMLI (**c**) Circuit with isolated AC sensors and relays for the CHBMLI.

5.2. Temperature Rise of a Single Module (CHBMLI)

A single module is detailed in Figure 9a. The left side of the board contains the power converter (H-Bridge and capacitors). Under an input power of 365 W and a switching frequency of 1.5 kHz (for the H-Bridge of this module), the power switches have a temperature rise of 32 °C (Figure 9b), which validates the thermal analysis presented in Section 4.4. The measured efficiency (including IC operating losses) is 98.5%. This measurement does not include inductor losses. However, with a full converter at nominal power, the low inductance value would not significantly modify the overall efficiency. This low temperature rise confirms that no heatsink is required to maintain the junction temperature of the MOSFETs below 100 °C. On top of that, in a conventional inverter, the heat released by the MOSFETs (with heatsink) usually increases the temperature of the DC-link capacitors, which have to be placed close to the H-Bridge in order to reduce the parasitic inductance of the track. This temperature rise of the DC-link capacitor often leads to faster aging and reduced lifetime [38]. Failure of the aluminum electrolytic of the DC-link capacitor is one of the most common faults on a conventional H-bridge.



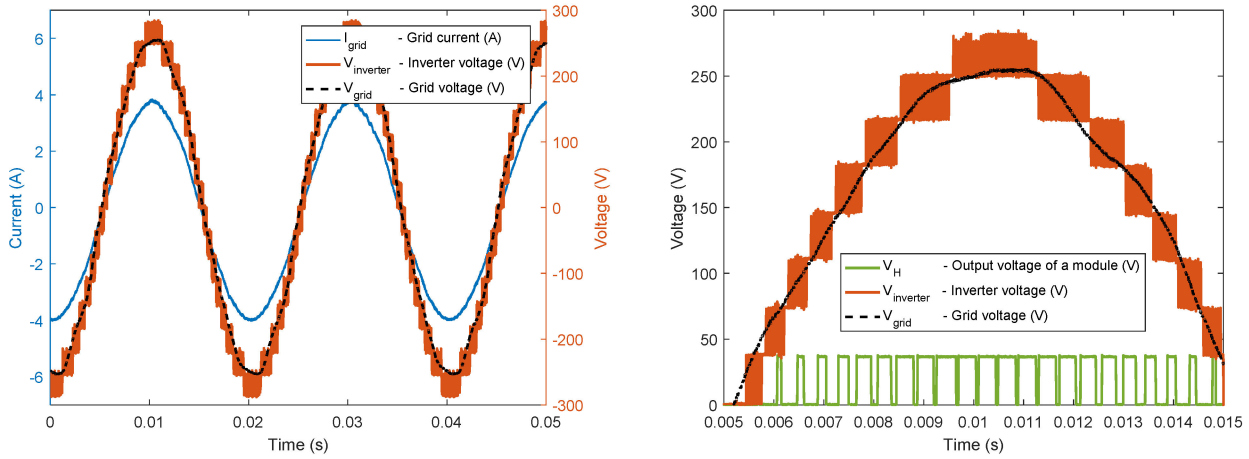
(**a**) (**b**)

Figure 9. (**a**) Prototype of a single module of the Cascaded H-Bridge Multilevel Inverter (CHBMLI) (**b**) Thermal image of a module at $P_{out} = 365$ W.

5.3. Waveforms of the CHBMLI

The waveform of the CHBMLI voltage $V_{inverter}$ (in red) and the output current (in blue) are shown in Figure 10a. This figure is zoomed over a half grid period in Figure 10b, including in green the output voltage of a single module. The low switching frequency (in green) of a single module (compared to the high switching frequency $f_{sw} = 20$ kHz of the complete converter) can be observed.

$$f_{sw_{module}} = \frac{f_{sw}}{N} = 2.5 \text{ kHz} \tag{75}$$



(**a**) (**b**)

Figure 10. (**a**) Waveforms of the CHBMLI with $I_{grid_{rms}} = 3$ A, $N = 8$, $V_{grid_{rms}} = 180$ V: Current grid I_{grid} (blue), Inverter Voltage $V_{inverter}$ (red), Grid voltage V_{grid} (black) (**b**) Same as (**a**) but including the output voltage of a single module V_{H_i} (green).

Due to limited power on the experimental setup, the complete converter was tested with 70 W per module. This results in an output RMS current of 3 A, and an off-the-shelf inductor was chosen for this current (2 mH/5 A) to limit the harmonics. For the same output current, a high-frequency ripple, a bigger inductor would be required (by a factor $N = 8$). The output sinusoidal current (in blue) is set in phase with the grid voltage (in black) in order to ensure a unity power factor. On top of that, each solar panel is regulated around its own optimal voltage (V_{MPPT_i}). Thus, the energy extraction is maximized by the

CHBMLI. Under partially shaded weather conditions, the CHBMLI extracts more power than the conventional H-Bridge.

6. Conclusions

A comparison between the design of the conventional H-Bridge and the CHBMLI is presented in this paper. First, a series of constraints regarding the efficiency, the maximum solar power extraction, the components' lifespan, and the cost were established to make the comparison as realistic as possible. For both topologies, inductors, capacitors, transistors, and heatsink are sized. The multilevel ability of the CHBMLI makes it more interesting when it comes to filtering the output current of the inverter, thus reducing the size and cost of the inductor. As both topologies are DC−AC converters with the same amount of DC and AC power and considering the same DC-link voltage ripple ratio, the capacitor's energy sizing is similar in both cases. For the conventional H-Bridge, low-value and medium-voltage capacitors are used, and for the CHBMLI, medium-value and low-voltage capacitors are used. The reduced choices for capacitors for the CHBMLI lead to higher global ESR, which creates slightly higher losses. When it comes to global efficiency, the CHBMLI has a serious advantage due to very low switching losses compared to the conventional H-Bridge, thanks to low voltage levels. The reduced losses, which are furthermore spread over a higher number of transistors, lead to low temperature rise without the need for a heatsink for the CHBMLI. For the conventional H-Bridge, the trade-off between cost and efficiency leads to the use of a heatsink to cool transistors. The vast choice of small voltage transistors (for the CHBMLI), despite the large number of transistors required, makes it easier to select low-cost components for the design. The cost of medium voltage transistors combined with the cost of the heatsink and the isolated drivers is about 50% superior to the cost of transistors and the drivers for the CHBMLI with the same performances (same global conduction losses and same temperature rise). A real CHBMLI prototype with eight modules was built to validate several aspects of the design. The converter was tested with a 20 kHz switching frequency on the grid voltage with a sinusoidal output current of 3 Arms, a low current ripple, and a unity power factor. The low temperature rise (without a heatsink) of a single module at 365 W was also validated.

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