electronics

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Design of a 0.4 V, 8.43 ENOB, 5.29 nW, 2 kS/s SAR ADC for Implantable Devices

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Abstract: This paper presents a 9-bit differential, minimum-powered, successive approximation register (SAR) ADC intended for implantable devices or sensors. Such applications demand nanowatt-range power consumption, which is achieved by designing the SAR ADC with a proposed bootstrap switch, bespoke split-capacitive DAC, customized comparator and a modified dynamic bit-slice unit for SAR logic. The linearity of the ADC is improved by introducing a bootstrap switch with a low clock feedthrough and threshold voltage variations along with the disseminated attenuation capacitor in the split-capacitive DAC. The dynamic comparator is customized to be simple in terms of the number of transistors to gain the advantage of low power and is also designed to have a low dynamic offset voltage. The stacking concept is embedded in the bit-slice unit of SAR logic to achieve reduced leakage power. This paper is concerned with how to contribute to low power consumption in all the aspects possible related to the implementation of the SAR ADC. With a 0.4 V supply and at 2 kS/s, the proposed ADC achieves an SNDR of 52.52 dB and a power consumption of 5.29 nW, resulting in a figure of merit (FOM) of 7.66 fJ/conversion-step.

Keywords: implantable devices; low-power electronics; SAR ADC; CMOS circuits; bootstrap switch; linearity errors

Citation: Lakshmi, P.V.; Musala, S.; Srinivasulu, A.; Ravariu, C. Design of a 0.4 V, 8.43 ENOB, 5.29 nW, 2 kS/s SAR ADC for Implantable Devices. *Electronics* **2023**, *12*, 4691. https://doi.org/10.3390/electronics12224691

Academic Editor: Costas Psychalinos

Received: 4 September 2023
Revised: 30 October 2023
Accepted: 8 November 2023
Published: 18 November 2023

1. Introduction

These days, many applications similar to vivo sensors, biomedical implantable devices or wireless guided devices utilize the SAR ADC over other ADC architectures [1–3]. This is owing to its advantages of being scaled down with the technology, as it uses the least analog circuitry, and the benefit of energy efficiency allows it to operate at ultra-low-power supply voltages, which is in demand for medical electronics. Also, for the digitization of the sensed biopotential signal, a moderate resolution (8–12 bits) with sampling frequencies between 1 kS/s and 1000 kS/s ADC may be sufficient, which is aptly fulfilled by the SAR ADC [4–7]. Considering low power as the main constraint, it is achieved by trading off speed in this paper with a low sampling rate of 2 kS/s.

The capacitive DAC utilized in SAR ADC forms one of the power-thirsty blocks [8,9]. Its power consumption is mainly due to the DAC's switching activity as well as the total capacitance of the DAC. This paper mainly focuses on reducing the total capacitance of the DAC and, thus, reducing its area and power consumption. The majority of SAR ADCs utilize charge-scaling DACs to gain the advantage of low power dissipation, as the capacitive array does not dissipate static power. Furthermore, the offset of the DAC can also be easily compensated for if a switch capacitor circuit is used. However, the value of capacitors used in the DAC rises exponentially with the number of bits [10]. For this reason, charge-scaling DACs employed in high-resolution SAR ADCs suffer from problems

like mismatch of the capacitors, large area, high power consumption and inaccuracy of the DAC [10–12].

These problems can be overcome by utilizing a split-capacitive DAC that incorporates an attenuation capacitor to split the charge-scaling DAC into two groups [10]. This method reduces the weight of the MSB capacitor, thus reducing the area and dynamic power dissipation and also improving the linearity errors. The DAC area can be further minimized by reducing the value of MSB capacitance by further splitting the DAC, as shown in [13]. This method reduces the area of the DAC by 47% in the case of 8-bit architecture and improves accuracy with small capacitor mismatches. Furthermore, the thermometer code is utilized for replacing C and 2C capacitors with three capacitors of value C. So, the maximum capacitance value used will only be the attenuation capacitance of 4C/3, and the mismatch will be between C and 4C/3. The modified split-capacitive DAC eliminates the use of thermometer code and extra logic gates to achieve the simplicity of using only one valued capacitor. The design is carefully considered in the proposed DAC to realize the entire DAC with only a single-valued capacitor C design, thus minimizing capacitor mismatches.

The comparator is a constituent block of the SAR ADC that consumes a considerable amount of power. To save power, the design of the comparator should be as simple as possible while simultaneously using a reduced number of CMOS transistors. Also, due to the presence of mismatches in the dynamic comparator, which have inherent positive feedback, there will be an input-referred offset voltage that has to be minimized as it creates linearity errors. Between the static offset voltage caused by transistor parameters and threshold variations, and the dynamic offset voltage caused by mismatches in the parasitic capacitances, this paper concentrates on reducing the dynamic offset voltage. From the analytically balanced model, an intuition about the main contributors of the offset is obtained and the design modifications are performed accordingly to minimize the offset. Top plate sampling has the advantage of eliminating the use of MSB-valued capacitance as the direct comparison after sampling with equal DACp and DACn voltages, generating the MSB bit. This reduces DAC area and power consumption but affects linearity. Hence, a bootstrap sampling switch is an incumbent as it reduces the possible linearity errors. A bootstrap switch is proposed in this paper and implemented in the SAR ADC.

On the other hand, organic field effect transistors have also been recently used in sensors in order to convert a biosignal into an electronic signal [14]. Often, the transducers are commanded by a complementary metal-oxide semiconductor (CMOS) circuitry. The advantages of the combination of implantable sensors, CMOS electronics and integration technologies have been revealed by many authors [15–22]. In 2019, Angotzi et al. presented an implantable CMOS biosensor for simultaneous large-scale neural recording. The increase in the number of simultaneous neural recordings was possible due to the 180 nm CMOS technology, which offered a power consumption of less than 6 μW per pixel and referred to noise around 7.5 μV, incorporated in an in vivo neuro-biosensor applied on rats [18]. In 2020, Harpaz et al. reported a CMOS-based sensor that integrated specific DNA strands and could be able to detect enoyl-CoA-hydratase-isomerase as an indicator of the presence of the Colletotrichum gloeosporioides fungi [19]. In 2023, Tran et al. described the first bioluminescent-paper-based biosensor for ATP, combining zeolitic imidazolate framework-8 as the metal–organic framework (MOF), luciferase as the key enzyme, a portable detector and a smart-phone-integrated CMOS [20]. In all these cases, a constant triadic demand needs to be solved: low power, low voltage and low noise must be harmonized within the electronic recording circuitry. Therefore, this paper contributes to the design of a low-power SAR ADC using a 45 nm CMOS process in all possible aspects related to the implementation of implantable sensors, as every sensor needs an ADC for its data to be digitized.

The paper is structured as follows. Section 2 portrays the SAR ADC inclusive architecture. Section 3 describes the ADC design and its implementation, which comprises the proposed bootstrap switch operation; a discussion about its linearity, customized comparator operation and calculation of its static and dynamic offset; and elucidates the modified

split-capacitive DAC and dynamic bit-slice unit of the SAR logic block of the ADC in detail. Section 4 presents the simulation results of the proposed SAR ADC, and conclusions are drawn in Section 5.

2. SAR ADC Architecture

Figure 1 represents the proposed fully differential SAR ADC, designed using a novel bootstrap switch, modified split-capacitive DAC, SAR logic and the proposed dynamic comparator. The bootstrap switch is a necessary component in all SAR ADCs operated at low supply voltages to maintain a low resistance and to reduce the sampling distortion [21]. A differential architecture is used to avail the advantage of high common mode noise rejection and good linearity [23]. The designed dynamic comparator achieves low offset and consists of a lower number of transistors that aids in attaining low power consumption. The differential DAC voltages are compared by the comparator to generate a digital signal that produces a digital code through SAR logic, which is further fed back to the differential DAC to convert the same into an analog signal.

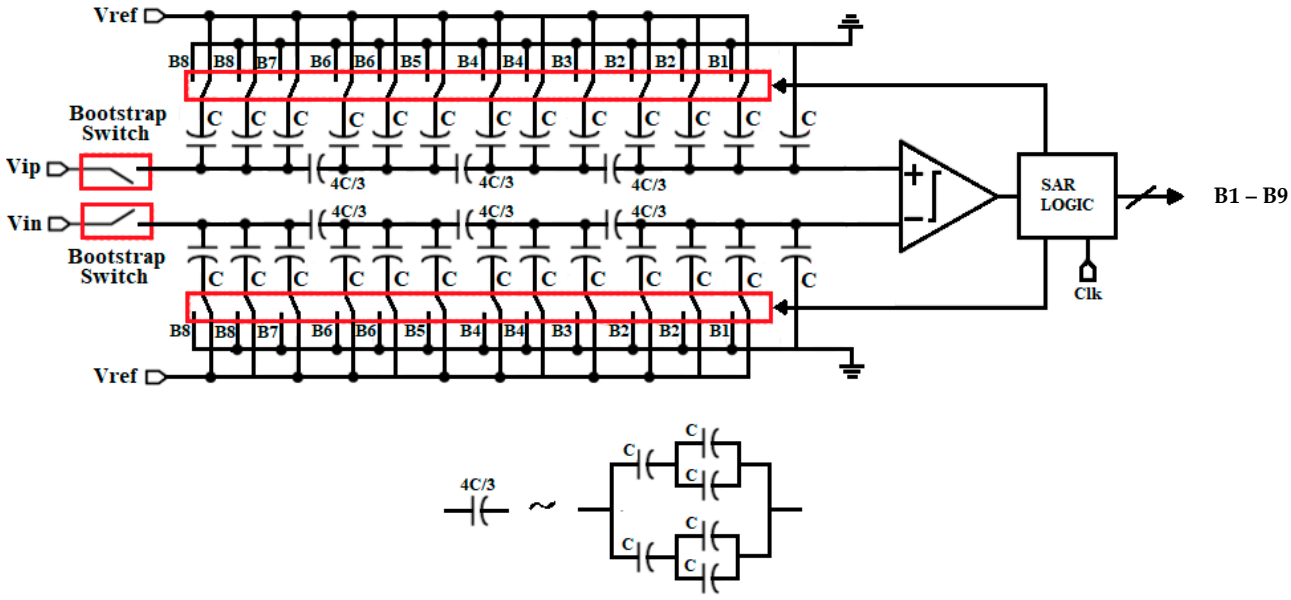


Figure 1. Proposed fully differential SAR ADC.

3. Implementation of Key CMOS Blocks

The basic building blocks of SAR ADC are two bootstrap switches, two capacitive DACs, a dynamic comparator and SAR control logic. The detailed description of each block is presented in the following subsections.

3.1. Proposed Bootstrap Switch

Figure 2a represents the proposed bootstrap switch circuit along with its layout shown in Figure 2b. When the clk signal is high, the sampling switch is turned off and the C_1 capacitor pre-charges to supply voltage V_{dd}. In this design, $\overline{clk}$ is generated internally to reduce the transistor count and achieve low power. Later, when clk becomes low, the floating battery C_1 charges the sampling transmission gate to $V_{dd} + V_{in}$. The source terminal of the transmission gate receives V_{in}, thus maintaining a constant V_{gs} that makes the sampling switch work in a deep linear region to provide low resistance in the direction of improving linearity.

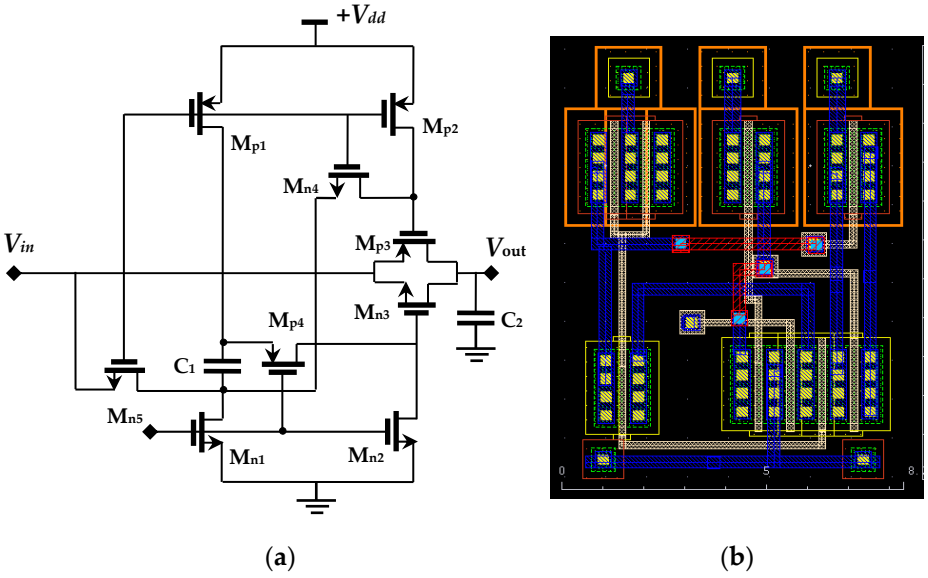


Figure 2. (**a**) Proposed bootstrap switch and (**b**) its layout.

As the transmission gate switch reduces the error and non-linearity caused by the charge injection, clock feedthrough and non-uniform on-resistance, a new bootstrapped S/H circuit is proposed, utilizing the transmission gate switch. The on-resistance and the change in voltage of the proposed S/H design can be written in (1) and (2), respectively. Moreover, the change in voltage expression excludes the overlap capacitance consideration as it is a very minimally impacting term.

$$R_{on} = \frac{1}{\mu_n C_{ox}\left(\frac{W_n}{L_n}\right)(V_{dd} - V_{tn}) + \mu_p C_{ox}\left(\frac{W_p}{L_p}\right)\left(V_{dd} - \mid V_{tp} \mid\right)} \tag{1}$$

$$\Delta V = \frac{C_{ox}\left[W_p L_p\left(V_{dd} - \mid V_{tp} \mid\right) - W_n L_n (V_{dd} - V_{tn})\right]}{2C_H} \tag{2}$$

where the subscripts n and p represent the nMOS and pMOS transistors of the transmission gate switch, respectively. Equation (1) shows that the resistance is independent of the input voltage but dependent on the threshold voltage. However, as V_{th} is proportional to the substrate to bulk voltage, connecting bulk to substrate overcomes this problem, and the R_{on} of the design is maintained constant and will be independent of input. Also, the resistance is very low as the switch is biased in a deep linear region. Good linear S/H circuits desire constant and low on-resistance, which is achieved by the proposed design. Moreover, the change in voltage at the output node of the sampling switch Equation (2) is also independent of the input voltage, further enhancing the linearity of the design. Another reason for high linearity is the reduced harmonic distortion due to the low gate capacitance of the sampling switch compared with other state-of-the-art designs.

In low-power applications, the body effect due to threshold variations is also the cause of non-linearity, and an attempt is made to improve this through the design. The bodies of M_{p1} and M_{p4} are connected to the high-voltage end of C_1 to reduce the threshold voltage variations, thus reducing the linearity errors. Body effect is also minimized by using the transmission gate as a sampling switch that introduces differential clock feedthrough error, which is equal in amplitude and opposite in phase at the drain terminals of the transmission gate, thus reducing clock feedthrough error.

Most of the existing bootstrap switches have no direct discharge path; rather, they consist of transistors not driven by the clk signal. This introduces a delay in the switch, which is reduced in the proposed design by connecting the gates of the transmission switch

to transistors that are directly driven by a clock. Moreover, care is taken in the design to have only one transistor in the discharge path in order to improve the speed of the circuit.

Direct connection of the input signal to the sources of the transmission gate ensures that the V_{gs} of the gate does not exceed V_{dd}. In this design, the typical value of C_1 = 50 fF is approximately five times the parasitic capacitance of the transistor with a channel length of 45 nm. Reliability constraints and a load capacitance value of 1 pF are considered while choosing the transistor sizes in order to not violate the specifications.

To evaluate the performance of the proposed bootstrap switch, it is used as a sample and hold circuit and is simulated using cadence virtuoso 45 nm CMOS technology files with a supply voltage of 0.45 V by applying a sinusoidal input of 0.45 $V_{p\text{-}p}$ at 0.2 KHz frequency using a sampling clock of 2 KHz frequency, suitable for in vivo biosensing applications [14–18]. The post-layout is shown as the transient simulation result in Figure 3a. For fair comparison, bootstrapped switches from [24,25] are re-simulated with the same input parameters and then compared. The power consumed by the proposed switch is 111.9 pW, which is 23.5% less than [24] and 18.6% less than the bootstrap switch proposed in [25] because the proposed circuit benefits from the advantage of a lower transistor count and simplicity in its design. Moreover, the simulated leakage power is only 19.9 pW, about 17.7% of the total power, which is not considerable; hence, the design is not enhanced with the leakage reduction techniques.

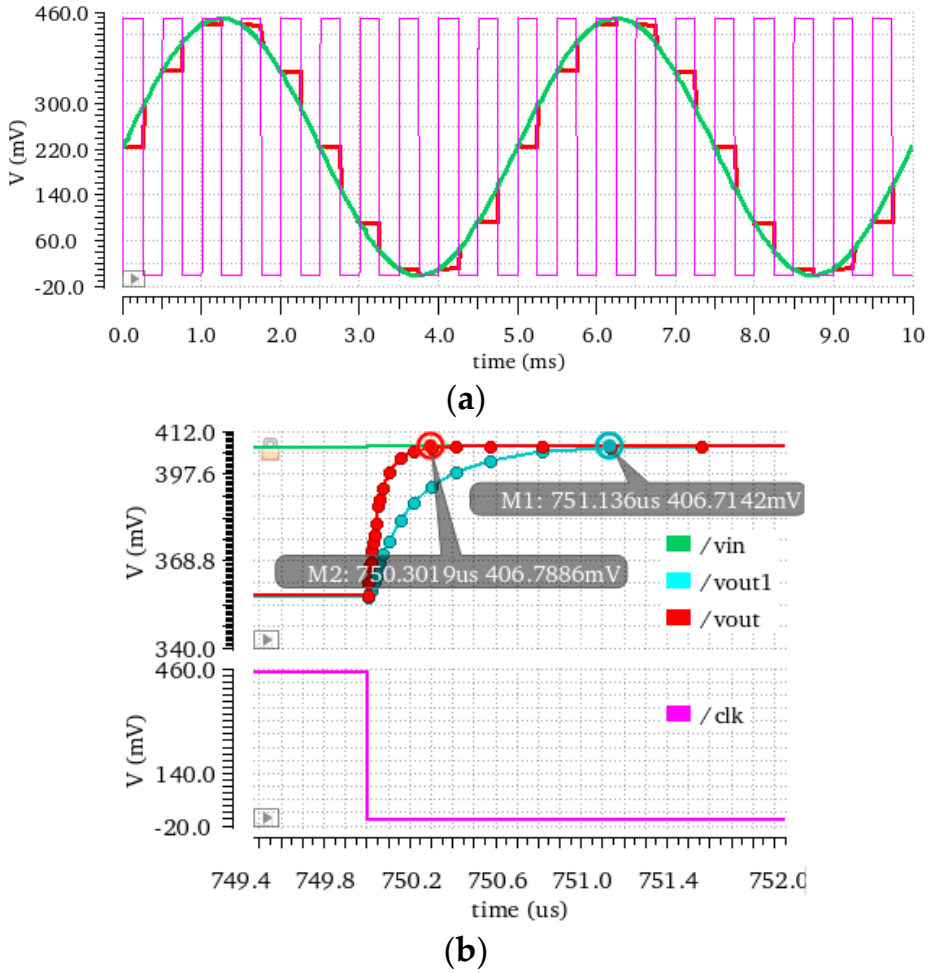


Figure 3. (**a**) Transient response of novel bootstrap switch. (**b**) Transient response with low *Vt* and standard *Vt*.

Lowering of the supply voltage is one of the techniques for low-power design, but the disadvantage of this practice is that it increases delay. As it is known that delay is

inversely proportional to supply voltage and directly proportional to the threshold voltage, the increase in delay due to the lowered supply voltage can be compensated by reducing the threshold voltage. Hence, in this design, low-V_t devices are preferred to speed up the turn-on time of the sampling switch by 8.3% compared with the standard V_t, as shown in Figure 3b.

Figure 4 shows the simulated FFT plot of the proposed bootstrap as a sample and hold circuit that achieves an ENOB of 12.77 bits, SFDR of 79.16 dBc and SNR of 78.65 dB, which are reasonably good results at lower sampling rates compared with those mentioned in [24,25] that achieve similar results at higher sampling rates. Hence, the proposed bootstrap switch is a better choice to be used in biomedical applications as a sample and hold circuit, which requires a good ENOB and SNR at low frequencies with low power consumption.

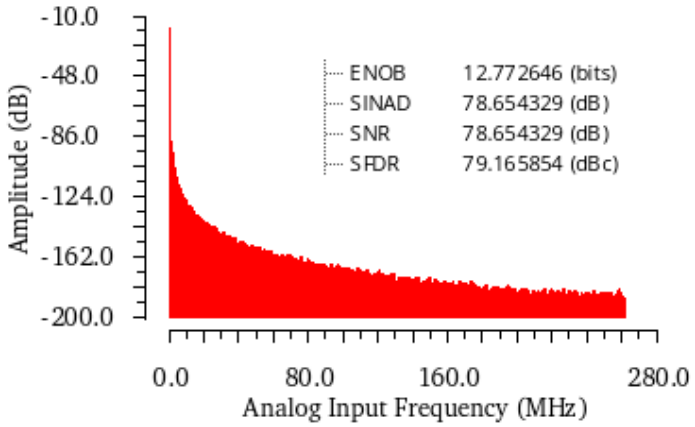
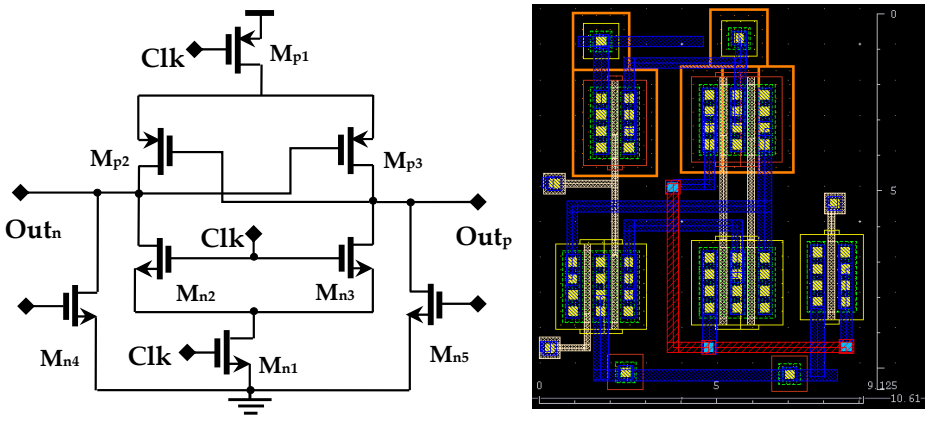


Figure 4. FFT spectrum plot of novel bootstrap switch.

3.2. Dynamic Comparator

Figure 5a represents the proposed dynamic comparator, intended to be used in SAR ADCs applicable in implantable sensors. In this circuit, when Clk is high, M_{n1}, M_{n2} and M_{n3} are ON, discharging the nodes 1 and 2 to ground. Subsequently, when Clk is low, M_{p1} is turned on, bringing M_{p2} and M_{p3} to an ON state by making the V_{gs} of these transistors negative. Hence, nodes 1 and 2 are charged to V_{dd}. These nodes are then discharged to the ground based on the differential inputs applied to M_{n4} and M_{n5}. Figure 5b represents the layout of the proposed dynamic comparator design.



(**a**) (**b**)

Figure 5. (a) Proposed dynamic comparator and (**b**) its layout.

The proposed design avails the advantage of employing the circuit with a single clock that speeds up the comparison process compared with other different clocks, such as those in [26,27]. This circuit also generates an output that could be directly used to drive the SAR logic block of SAR ADC, unlike the conventional process where the differential outputs of a comparator are fed to a latch that further drives the SAR logic. The proposed design from the output point of view avoids the use of a latch, thus saving the chip area and power. As the input-driven transistors are directly connected to the output nodes, the design is supposed to endure a considerable amount of kickback noise. However, as the gate to drain parasitic capacitance and a parallel combination of drain to bulk and source to bulk parasitic capacitance are associated with inputs in opposite directions, the difference of charge in these capacitances will add on to the input, thus producing a negligible amount of kickback noise. This has been verified by simulating the proposed design and the existing designs using the kickback noise test bench from [28], and the results are tabulated. Apart from saving power, this design also provides low offset, which is a key factor to enhance the performance of the comparator that, in turn, augments the performance of the whole ADC. Process variations lead to device mismatches, which is a primary source of offset [28–30]. There are two types of offsets: static and dynamic, where static offset is due to current factor and threshold variations between the devices while dynamic offset is due to parasitic capacitance variations [22]. In the proposed design, as M_{n1}, M_{n2} and M_{n3} are off during the comparison phase, they do not affect the offset value. Even though M_{p1} is on during the same phase, it is out of the differential operation, so it does not have an influence on the static offset. To find the static offset voltage, the transistors M_{p2} and M_{p3} are in the saturation region as they are directly connected to the output nodes Out_p and Out_n, respectively, and the input differential transistors M_{n4} and M_{n5} are in the triode region as they simply act as voltage-controlled resistors. Hence, the currents from these transistors can be mentioned as follows:

$$I_{dsp2} = (\mu_{p2}C_{ox}/2)\,(W/L)_{p2}\,(Out_p - Out_n - V_{tp2})^2 \tag{3}$$

$$I_{dsp3} = (\mu_{p3}C_{ox}/2)\,(W/L)_{p3}\,(Out_n - Out_p - V_{tp3})^2 \tag{4}$$

$$I_{dsn4} = (\mu_{n4}C_{ox})\,(W/L)_{n4}\,(V_p - V_{tn4} - V_{dsn4}/2)V_{dsn4} \tag{5}$$

$$I_{dsn5} = (\mu_{n5}C_{ox})\,(W/L)_{n5}(V_n - V_{tn5} - V_{dsn5}/2)V_{dsn5} \tag{6}$$

Consequently, utilizing these current equations from (3)–(6), the offset from the balanced method [22] is

$$V_{os\,(Mn4,Mn5)} = (I_{dsn4} - I_{dsn5})\,R_{p2} \tag{7}$$

where R_{p2} is the constant resistance at M_{p2}, which is like the resistance at M_{p3} under a balanced condition, i.e.,

$$R_{p2} = 1/(\mu_{n2}C_{ox})\,(W/L)_{p2}\,(V_{d2}) \tag{8}$$

Substituting (5), (6) and (8) in (7) and elaborating yields

$$V_{os(Mn4,Mn5)} = \frac{\left[(\mu_{n4}C_{ox})\left(\frac{W}{L}\right)_{n4}\left(V_p - V_{tn4} - \frac{V_{dsn4}}{2}\right)V_{dsn4} - (\mu_{n5}C_{ox})\left(\frac{W}{L}\right)_{n5}\left(V_n - V_{tn5} - \frac{V_{dsn5}}{2}\right)V_{dsn5}\right]}{(\mu_{n2}C_{ox})\left(\frac{W}{L}\right)_{p2}V_{d2}} \tag{9}$$

Under the balanced condition,

$$\text{Let } \mu_{n4}C_{ox} = \mu_n \;\&\; \mu_{n5}C_{ox} = \mu_n + \Delta\mu_n \tag{10}$$

$$V_{tn4} = V_{tn} \;\&\; V_{tn5} = V_{tn} + \Delta V_{tn} \tag{11}$$

$$V_p = V_n = V_{in} \tag{12}$$

$$V_{dsn4} = V_{dsn5} = V_{dsn} \tag{13}$$

$$(W/L)_{n4} = (W/L)_{n5} \tag{14}$$

where $\Delta\mu_n$ = mobility variations and ΔV_{tn} represents threshold variations due to the mismatch between M_{n4} and M_{n5} transistors. Substituting (10)–(14) into (9) and simplifying would lead to

$$V_{os(Mn4,Mn5)} = \frac{\left[\Delta V_{tn}(\mu_n + \Delta\mu_n) + \Delta\mu_n\left(V_{tn} - V_{in} + \frac{V_{dsn}}{2}\right)\right]\left(\frac{W}{L}\right)_{n4} V_{dsn}}{\mu_{p2} C_{ox}\left(\frac{W}{L}\right)_{p2} V_{d2}} \tag{15}$$

In (15), if the lengths of the transistors are the same, then the variations in the mobility and threshold voltages are inversely proportional to the width of the differential transistor pair and directly proportional to the width of switch, producing constant resistance. Hence, static offset due to a differential pair can be reduced by increasing the size of the differential transistors and reducing the size of the cross-coupled pMOS transistors. However, as M_{p2} and M_{p3} are used to generate constant currents, a reduction in their size would also affect the offset voltage. Hence, the overall static offset of the comparator will be

$$\sigma^2_{OS} = (\sigma^2_{\Delta VMn4\text{-}Mn5} + \sigma^2_{\Delta VMp2\text{-}Mp3})^{1/2} \tag{16}$$

The static offset of the cross-coupled pMOS transistors is also inversely proportional to their widths as they generate constant current; so, in contrast to the abovementioned, the widths of these transistors must be increased. Hence, design care is taken regarding the aspect ratios to have a trade-off between offset voltage and transistor size. Simulations of offset contributed by each mismatch transistor pair are shown in Figure 6. As mentioned, M_{n1}, M_{n2} and M_{n3} are off during the comparison phase, and M_{p1} is on but is not affected by the differential operation; hence, it does not influence the static offset.

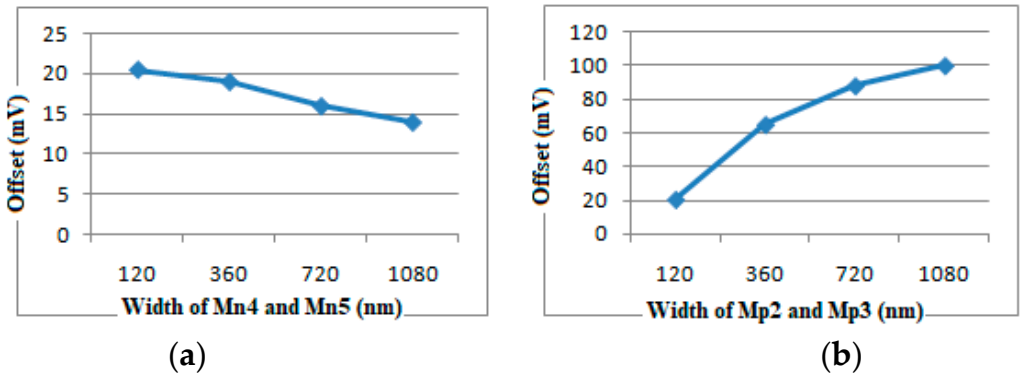


Figure 6. Simulation of offset rendered by each transistor.

As discussed, regarding the dynamic offset, it is due to the parasitic capacitance variations that can be obtained by equating the differential output voltages as described in the balanced method [22], $dOut_p/dt = dOut_n/dt$, which means

$$I_{dsp2} = C_n \frac{dOut_n}{dt} \tag{17}$$

and

$$I_{dsp3} = C_p \frac{dOut_p}{dt} \tag{18}$$

equating the differential outputs

$$\frac{I_{dsp2}}{C_n} = \frac{I_{dsp3}}{C_p} \tag{19}$$

Applying the square law model to overwrite the drain source current in terms of voltage, the offset voltage due to mismatches in C_p and C_n is derived as

$$V_{os\ Cpn} = \frac{\Delta C_{pn}}{C_p} \frac{I_{dsp3}}{\mu_{n2} C_{ox} \left(\frac{W}{L}\right)_2 V_{ds2}} \tag{20}$$

Hence, this proves that dynamic offset depends on relative capacitance mismatch $(\Delta Cpn/Cp)$ rather than absolute capacitance mismatch. So, this dynamic offset is reduced by the following:

- Increasing the transistor sizes of the differential pair;
- Matched capacitors can be added at the output nodes to reduce the relative mismatch;
- Constant current can be generated into the output nodes.

By the end of the comparison phase, both the output nodes Out_p and Out_n are pulled down to ground by the differential pair of transistors due to which M_{p2} and M_{p3} will enter saturation. Subsequently, during the reset phase, M_{p1} turns ON, forming ac as a code current source path along with M_{p2} and M_{p3} to both the output nodes Out_p and Out_n, respectively. This produces constant drain currents. In a while, at the beginning of the comparison phase, when one of the output nodes is low, the cross-coupled pMOS transistor driven by the same output node will be in saturation, generating a constant current that makes a stable current to flow in the other branch too, as they are cross-coupled. Hence, through this design, constant drain currents are generated to the output nodes to reduce the dynamic offset. The geometric dimensions followed in this design to obtain the optimized offset voltage are revealed in Table 1.

Table 1. Dimensions of each transistor.

	Mp1	**Mp2, Mp3**	**Mn2, Mn3**	**Mn4, Mn5**	**Mn1**
W (nm)	120	240	120	1000	120
L (nm)	45	45	45	45	45

Table 2 presents the post-layout simulation results of the proposed comparator. It includes a comparative analysis of the proposed circuit with the referenced comparators, which are also simulated at 45 nm for equivalence. The design has a comparatively low offset due to its simple circuitry and careful sizing of the transistors in the circuit. Ref. [31] has lesser kickback noise due to its three-stage network, which isolates the input from the output strongly but at the cost of power consumption. Refs. [21,32] have low delay due to less cascaded transistors from supply rail to output. But the proposed one proves that the design is efficient and can be sufficiently used in low-power applications with less offset voltage. Moreover, the leakage power calculated for the design is only 51.4 pW, which is barely 4.8% of the total power. The kickback noise simulated is 2 mV, which is comparatively lower owing to the addition of the difference of the charge in the parasitic capacitance associated with the input nodes.

Table 2. Comparative analysis.

S. No.	[33]	[21]	[32]	[31]	Proposed
Technology (nm)	45	45	45	45	45
Supply Voltage (V)	0.4	0.4	0.4	0.4	0.4
No. of Transistors	12	17	13	23	8
Offset Voltage (mV)	35.6	25	43	42	20
Kickback Noise (mV)	3.37	2.99	2.5	1.3	2
Power (nW)	6.77	4.6	1.97	10	1.07
Leakage power (W)	384 p	1.33 n	1.04 n	33.2 p	51.4 p
Delay (ns)	15.14	6.75	5.15	15	7.16

3.3. Modified Distributed Attenuation Capacitor Split-Capacitive DAC

Capacitive DAC is one of the main blocks of SAR ADC that consumes significant power. In a weighted capacitive DAC, the capacitance value increases with the number of bits; hence, a split-capacitive DAC was used that availed the advantages of low chip area and, thus, low power dissipation and high speed, but the fractional value of the attenuation capacitor produces mismatch errors [12]. For this reason, a distributed attenuation capacitor split-capacitive DAC was proposed in [13] that used capacitors of a single value to generate an 8 bit. In this paper, multiple attenuation capacitors are used instead of a single attenuation capacitor so that the MSB-driven capacitance value can be far reduced to 2C instead of 8C, as in a conventional split-capacitor DAC for an 8-bit ADC.

This saves about 47% of the chip area and reduces the capacitive mismatch errors as the capacitance values utilized are only C, 2C and 4C/3. [13] It further reduces the mismatch by replacing the 2C capacitance value with three capacitors of value C using a thermometer coding technique. This is represented in Table 3, and its circuit implementation is presented in Figure 7. However, this will still retain the mismatch between C and 4C/3 capacitance values and has an area overhead of using thermometer encoding. Also, realization of fractional-valued capacitance may introduce error. Hence, it is preferable to realize the entire ADC using a single-valued capacitance.

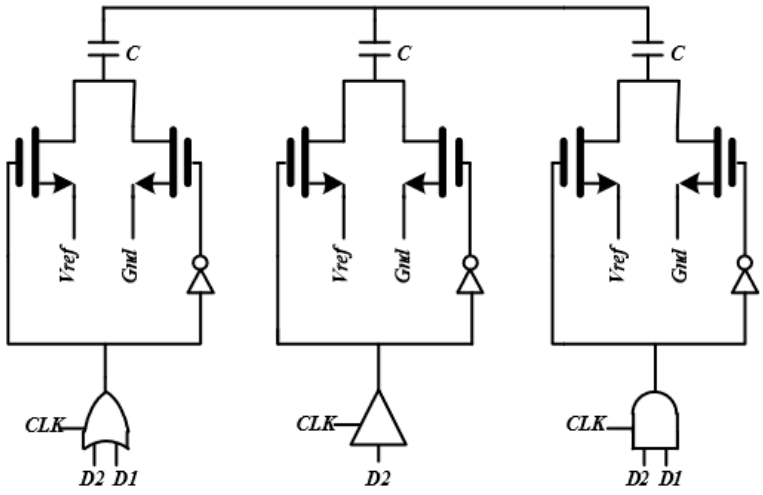


Figure 7. DAC capacitors along with 2-bit binary to thermometer decoding [13].

Table 3. 2-Bit thermometer decoding truth table [13].

Binary Code		Thermometer Code		
D_2	D_1	T_3	T_2	T_1
0	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	1	1	1

The modified distributed attenuation capacitor split-capacitive DAC proposed in this paper avoids the use of thermometer encoding, retaining the advantage of using the capacitance value of only C in the DAC part to which the bits are applied. The truth table in Table 3 can be modified in Table 4.

Table 4. 2-Bit thermometer decoding truth table.

Binary Code		New Code		
D_2	D_1	C_3	C_2	C_1
0	0	0	0	0
0	1	1	0	0
1	0	0	1	1
1	1	1	1	1

The proposed truth table, a modified form of the binary to thermometer decoding technique, is designed to represent the output codes (21–22) in terms of input bits to avoid the use of digital circuitry, as implemented in Figure 7.

$$C3 = D1 \tag{21}$$

$$C2 = C1 = D2 \tag{22}$$

Thus, the use of digital circuitry is avoided to save area and power consumption. So, now, the mismatch in the DAC would be with the C-valued capacitors through which bits from SAR logic are applied and an attenuation capacitor of value 4C/3. To represent the entire DAC in terms of unit capacitors, the attenuation capacitor is rearranged with the capacitors of value C to obtain the value 4C/3. Hence, minimizing the mismatch errors and limiting the maximum capacitance value used in the 9-bit DAC to value C to reduce the charging and discharging time of the capacitor improves the speed of the device. Here, the shortcoming is the parasitic capacitance associated with each capacitance that may deteriorate the capacitance equivalence. However, as the circuit is designed for low-frequency signals, this would not be of much use. The implementation of the modified DAC is shown in Figure 1, where MSB comparison is performed through top plate implementation and the remaining 8-bit DAC is split into three sub-DACs with a maximum capacitance of 2C, which is further split as per Table 4 into C and C, to which the MSB bit of the sub-DAC is applied. Attenuation capacitor representation is also shown in Figure 1. As the purpose of the paper is to showcase the use of split-capacitive DAC and overcome its problem of using a fractional attenuation capacitor, an energy switching scheme was not incorporated. But with the use of efficient energy switching schemes like in [34,35], better results could be incorporated.

3.4. SAR Logic

SAR control logic is implemented using dynamic logic as a substitute for complementary logic because its realization requires less transistors, thus offering better performance in terms of speed and power consumption [36]. But in this, at lower sampling rates, the leakage currents on the side of the output nodes of the bit-slice unit cause decision error at the P and N nodes of the logic. Hence, it is implemented using dynamic latch logic in [37] to eliminate the decision error caused by the leakage current. Accordingly, when the comparator output is ready, the positive feedback circuit latches the comparator outputs Out_p and Out_n to the P and N nodes, respectively, and are held constantly until there is a change in the comparator outputs, henceforth reducing the problem of leakage current. In the case of a proposed comparator design, the outputs are either differential in the comparison phase or grounded during the reset phase. As already mentioned, the bit-slice unit in [37] works well with the differential outputs, but when the comparator outputs are zero, leakage current might still exist.

This can be overcome by using a stacking of transistors technique to reduce leakage currents, reducing the leakage power thereafter. Figure 8 represents the modified SAR control logic designed by stacking the transistors driven by the comparator outputs in the bit-slice unit of [37]. Table 5 mentions the leakage power comparison of the bit-slice unit modified with that of the units from [36,37]. It proves that a stacked transistor bit-slice unit has low leakage power, thus contributing to the low power consumption of the entire SAR logic block.

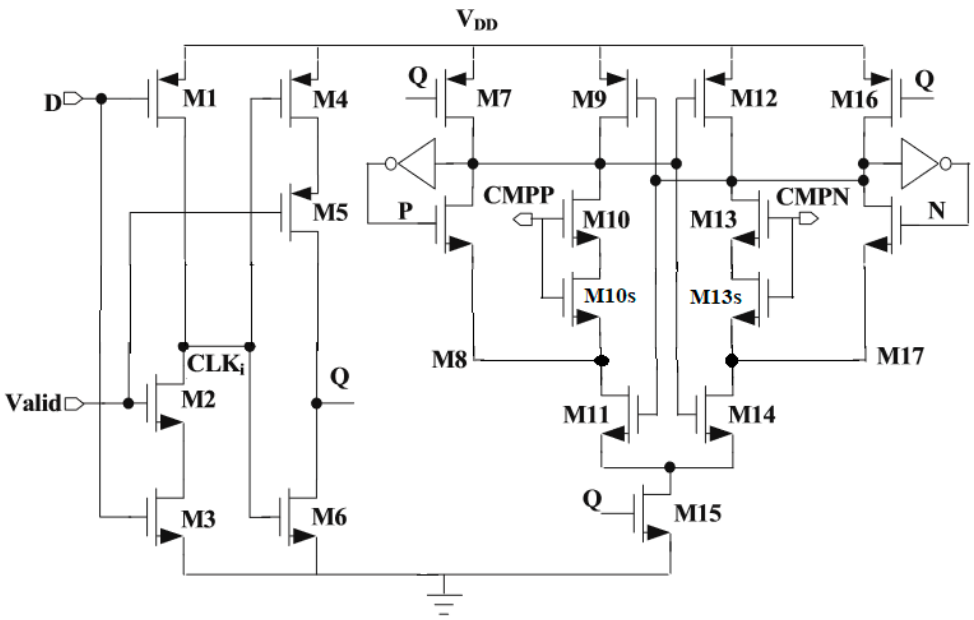


Figure 8. Modified SAR control logic.

Table 5. Comparison of leakage power of the bit-slice unit.

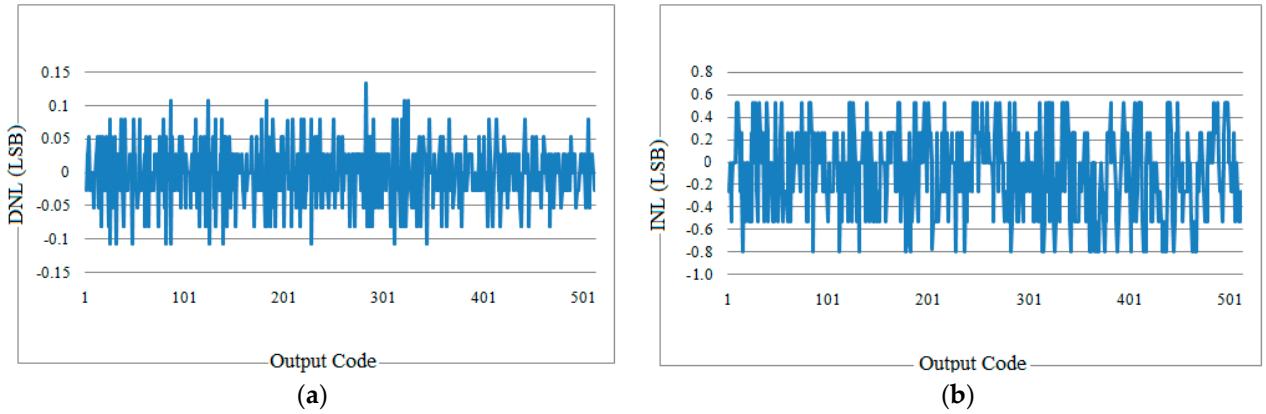
Reference	Leakage Power (pW)
[36]	56.08
[37]	41.8
Modified	38.4

4. Simulation Results of the Proposed ADC

The proposed 9-bit SAR ADC is simulated using a 45 nm CMOS process with a supply voltage of 0.4 V and a sampling rate of 2 kS/s. The simulated results are presented and discussed below.

4.1. Static Performance

Figure 9a,b show the simulated differential non-linearity (DNL) and integral non-linearity (INL) of the proposed SAR ADC. The DNL is in the range of −0.10/+0.13 LSB while the INL is within −0.8/+0.5 LSB. These values agree with the linearity range demand [14,17,20]. These are due to small changes in the output codes related to the MSB capacitor as it switches from low to high. This may be owing to the effect of the parasitic capacitance on the output.

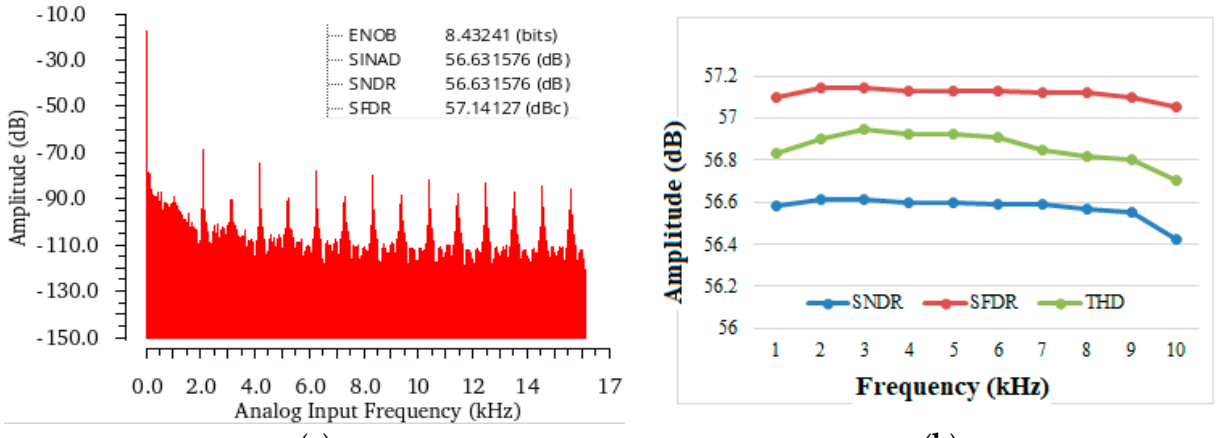


(**a**) (**b**)

Figure 9. Linearity error of (**a**) DNL and (**b**) INL.

4.2. Dynamic Performance

Figure 10a shows the simulated FFT spectrum of the proposed SAR ADC with a 0.4 V, 8 Hz sinusoidal input signal with a 0.4 V supply and 2 kS/s sampling rate. The obtained signal-to-noise ratio (SNR) is 56.63 dB, equivalent to an effective number of bits (ENOB) of 8.43 bits and a spurious-free dynamic range (SFDR) of 57.14 dB. Figure 10b plots the simulated SNDR, SFDR and THD against the input frequencies that remain almost constant up to 7 KHz and drop later.



(**a**) (**b**)

Figure 10. (**a**) Simulated dynamic performance FFT spectrum. (**b**) Dynamic performance vs. input frequency.

4.3. Power Performance

Leakage power is usually in terms of nW, which is the total power consumption of the entire ADC designed for low-frequency, medium-resolution, low-power applications. Hence, in this design, leakage power is reduced to reduce the overall power consumption of the ADC and care is taken in the design to propose each block with the minimum number of transistors and to avoid the static power consumption. Table 6 summarizes the simulation

results of the proposed ADC. From the data obtained, the design consumes only 5.29 nW in total.

Table 6. Performance summary of the proposed ADC.

Technology	45 nm
Power Supply	0.4 V
Reference Voltage	0.2 V
DAC Size	620 fF
SAR logic complexity	271 transistors
Unit Capacitor	20 fF
Input Range	[0, 0.4] V
DNL	−0.10/+0.13 LSB
INL	−0.8/+0.5 LSB
ENOB	8.43 bits @ 2 kS/s
SNDR	56.63 dB
SFDR	57.14 dB
Power	5.29 nW
Leakage Power	1.5 nW
FOM	7.66 fJ/conv.step @ 2 kS/s

Figure 11 shows the power consumption of each block. As the total array capacitance of DAC is 620 fF, it consumes a large portion of the power.

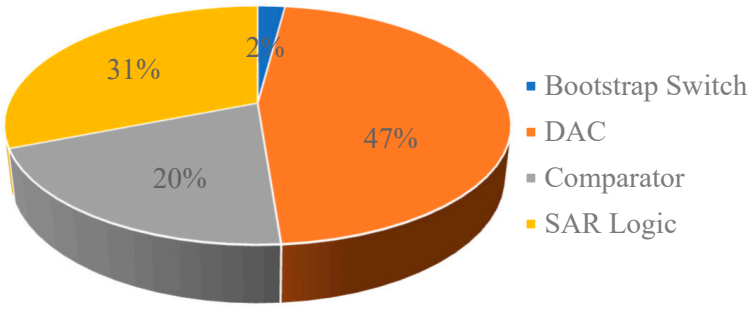


Figure 11. Power breakdown.

To compare the power efficiency of the ADCs designed with different technologies and topologies, with various sampling rates and resolutions, the commonly cited figure of merit (FOM) is used for comparison:

$$FOM = \frac{Power}{2^{ENOB} * f_s} \tag{23}$$

The FOM of the proposed ADC is 7.66 fJ/conv. step at 2 kS/s, lower than the referred noise for implantable devices [18].

Table 7 represents the comparative analysis of the ADCs picked through the literature survey of low-power ADCs, having lower sampling frequencies, with the proposed 9-bit ADC. Because of their excellence in terms of achieving low power, some of the earlier works were also taken into consideration for comparison. The comparison proved that the proposed ADC has comparatively low power consumption, but [28] has the least. This is due to the fact that it is implemented using a power gating technique that reduces the leakage power; the same technique can be utilized in the proposed design to further

enhance the power saving. Yet, the FOM of the proposed design portrays its efficiency. Ref. [31] is efficient in terms of achieving good SNDR due to the three amplification phases of the comparator used in the ADC that reduce the overall flicker noise and decouple the NTF zeros from the attenuation factor, allowing further reductions in noise. But the complex circuitry and generation of non-overlapping clocks made the designer to look for an alternative. Ref. [38] uses a body-driven technique in bootstrapped switches, SAR logic and a comparator to minimize leakage power consumption. In addition, a dynamic comparator with a floating inverter amplifier (FIA) architecture was designed to reduce the noise and offset by reducing the noise current. As a result, low power and good SNDR were achieved. However, as it uses a bulk-driven technique, it has low gain due to less transconductance compared with gate-driven and, thus, the efficiency of the circuit is low. The appreciating concern is that the proposed design achieves almost similar results using gate-driven transistors. Fabricated results may vary the simulated results by 10%, which would still prove the competence of the proposed design with the state-of-the-art low-power SAR ADCs included in [39–46].

Table 7. Performance summaries and comparison.

	[25] 2016	[27] 2015	[28] 2019	[29] 2006	[30] 2012	[33] 2010	[31] 2020	[38] 2022	**Proposed**
Technology (nm)	180	90	40	40	180	65	180	180	45
Result	Sim.	Sim.	Fab.	Fab.	Fab.	Fab.	Fab.	Sim.	Sim.
Resolution (bit)	9	9	9	9	8	10	8	10	9
Supply (V)	0.6	1	0.4	0.6	1.1	0.9	1	0.6	0.4
Sampling Rate (kS/s)	100	100	1	1	2	1	10	10	2
Power (nW)	399	473	1.8	130	27	5.8	90	41	5.29
DNL (LSB)	-	+0.8/−0.6	+0.36/−0.35	+0.8/−0.65	+0.28/−0.17	+0.59/−0.62	-	-	+0.13/−0.10
INL (LSB)	-	+0.5/−0.7	+0.44/−0.35	+0.85/−0.6	+0.81/−0.27	+0.89/−0.41	-	-	+0.5/−0.8
SNDR (dB)	53.5	53.55	50.1	-	46.3	56.5	65	61	56.63
SFDR (dB)	61.7	60.16	59.5	-	61.9	75.3		69	57.14
ENOB (bit)	8.59	8.35	7.9	7.6	7.4	9.1	7	10	8.43
FOM (fJ/conv.step)	10.4	14.5	7.7	666	79.9	10.94	50	4.14	7.66

5. Conclusions

This paper has presented an ultra-low-power SAR ADC intended for low-frequency, implantable bio-devices. The proposed ADC uses a modified split-capacitive DAC that uses a single-valued capacitor in order to reduce mismatch errors and a novel bootstrap switch to improve linearity and reduce power consumption. A dynamic comparator is also proposed that achieves a lower offset value and saves power through its design as it has a lower transistor count and a modified SAR control logic that implements stacked transistors to reduce leakage currents, thus contributing to power saving, as the SAR logic block is one of the power-hungry blocks of SAR ADC. The simulation results of the proposed ADC have verified the effectiveness of the design. The design achieves an ENOB of 8.43 bits at 2 kS/s with an overall power consumption of 5.29 nW and a FOM of 7.66 fJ/conversion-step, which are the minimal performances demanded in the biosensing area, to the best of our knowledge. Hence, the proposed ADC is also a serious candidate for the analog front-end circuitry that accompanies the usual implantable device applications.

Author Contributions: Conceptualization, P.V.L. and S.M.; methodology, P.V.L. and C.R.; software, P.V.L.; validation, S.M. and A.S.; resources, S.M. and A.S.; writing—original draft preparation, P.V.L.; writing—review and editing, S.M., A.S. and C.R.; visualization, S.M.; supervision, A.S.; project administration, A.S. and C.R.; funding acquisition, C.R. All authors have read and agreed to the published version of the manuscript.

Funding: In the case of acceptance, the APC of this research was funded by Universitatea Nationala de Stiinta si Tehnologie Politehnica Bucuresti, grant PubArt.

Informed Consent Statement: Not applicable.

Data Availability Statement: Data is contained within the article.

Conflicts of Interest: The authors declare no conflict of interest.

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