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Offset Voltage Reduction in Two-Stage Folded-Cascode Operational Amplifier Using High-Precision Source Degeneration

Cristian Stancu [1,*], Andrei Neacsu [1], Teodora Ionescu [1], Cornel Stanescu [2], Ovidiu Profirescu [1], Dragos Dobrescu [1] and Lidia Dobrescu [1]

[1] Department of Electronic Devices, Circuits and Architectures, Faculty of Electronics, Telecommunications and Information Technology, National University of Science and Technology Politehnica Bucharest, 060042 Bucharest, Romania; andrei.neacsu1411@stud.etti.upb.ro (A.N.); teodora.ionescu@stud.etti.upb.ro (T.I.)
[2] Onsemi Romania, 060042 Bucharest, Romania
* Correspondence: cristian.stancu2011@stud.etti.upb.ro; Tel.: +40-7437-65463

Abstract: The demand for CMOS precision operational amplifiers for critical applications has continuously increased over time due to higher accuracy and sensitivity requirements. Trimming or chopper architectures are advanced solutions that reduce the offset voltage and improve the circuit's parameters, but the complexity and the increased chip die size are serious downsides. An efficient solution is a source degeneration configuration to control the transistor's current-mirror transconductance, which impacts the offset voltage, with cost savings and a die area reduction also obtained. This paper focuses on designing and implementing such an approach in a two-stage folded-cascode operational amplifier. State-of-the-art thin-film resistors that use silicon–chromium as the metallic alloy were implemented to reduce mismatch variations between these passive components. Distinct methods that control the offset voltage parameter are also discussed and established. A comparison between the offset voltage standard deviation obtained using different types of resistors and that achieved with the innovative high-precision resistors was also carried out. The source degeneration's impact on the common-mode rejection ratio, power supply rejection ratio, bandwidth and phase margin was also analyzed, and a comparison between the proposed design and the classical one was performed. The process variation's influence on the circuit functionality was studied. A pre-layout ±1.273 mV maximum offset voltage at T = 27 °C was achieved using vector/array notations for the amplifier with the best overall performance. Post-layout simulations that included parasitic effects were performed, with a ±1.254 mV maximum offset voltage reached at room temperature.

Keywords: operational amplifier; CMOS technology; offset voltage; source degeneration; parasitic extraction; mismatch variation; process variation

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1. Introduction

Electronic systems are widely used nowadays, from medical equipment [1] (EKGs, pulse oximeters, etc.) to battery manager systems (electric vehicles, smartphones, etc.) [2]. They provide an appropriate response to the output after analyzing and processing a stimulus from the input. In general, the input stimulus is a very-small-value electronic signal. An operational amplifier (op-amp) [3–6] is used in critical applications as an important part of the whole system. It reads the small electronic signal at the input, amplifies it in order to be readable and, at the output, drives the device's next block.

Considering higher accuracy, precision and sensitivity requirements, precision operational amplifiers are mandatory in state-of-the-art applications. Complementary Metal Oxide Semiconductor (CMOS) technology is preferred by Integrated Circuit (IC) designers due to its high speed, high impedance at the transistor gate and low manufacturing cost.

One of the op-amp's important parameters that could have an impact on the circuit behavior is the offset voltage (V_{OS}) [7], which is the supplementary voltage that needs to be

applied at the circuit input so that the output has the desired value. In applications where the signal value at the amplifier's input is low (for example, in medical equipment) and if the V_{OS} from the system is unfortunately high enough, the undesirable signal overlaps with the signal that needs to be processed, thus creating the premise for the wrong interpretation of the information, and a malfunction in the system could occur. One more parameter that can cause a fault is the voltage noise density (e_n) [8], but fortunately, the methods that reduce the offset voltage and that will be presented in Section 2 are highly correlated with the ones used for noise reduction (thermal noise through transconductances but also the flicker noise through the transistor sizing); thus, designing a low-offset op-amp should lead to a low value for e_n. Moreover, the offset voltage has an impact on other electrical characteristics, such as the common-mode rejection ratio (CMRR) [9] (1) and the power supply rejection ratio (PSRR) [10] (2).

$$CMRR = 20\text{dB}\left(\frac{V_{OS1}|_{V_{CM1}} - V_{OS2}|_{V_{CM2}}}{V_{CM1} - V_{CM2}}\right) \quad (1)$$

where V_{OS1} and V_{OS2} are the offset voltages at two different common-mode inputs, V_{CM1} and V_{CM2} are the respective common-mode voltages, and $V_{CM1} > V_{CM2}$.

$$PSRR = 20\text{dB}\left(\frac{V_{OS1}|_{V_{DD1}} - V_{OS2}|_{V_{DD2}}}{V_{DD1} - V_{DD2}}\right) \quad (2)$$

where V_{OS1} and V_{OS2} are the offset voltages at two supply voltages, V_{DD1} and V_{DD2} are the respective supplies, and $V_{DD1} > V_{DD2}$.

According to Formulas (1) and (2), in order to increase the CMRR and PSRR parameter performance, the offset voltage standard deviation fluctuation that occurs when the common-mode and supply voltages are changing should be reduced.

Figure 1 shows one application that uses the op-amp as the main core: a unidirectional high-side current-sense circuit. Current-sense [11] topologies are widely used in battery management systems or overcurrent protection. The current that flows through R_SENSE establishes a potential between the pins of the R_1 and R_3 resistors. The op-amp, together with resistors $R_1 - R_4$, creates a loop that amplifies the voltage and sets the output to a value directly proportional to the R_SENSE current.

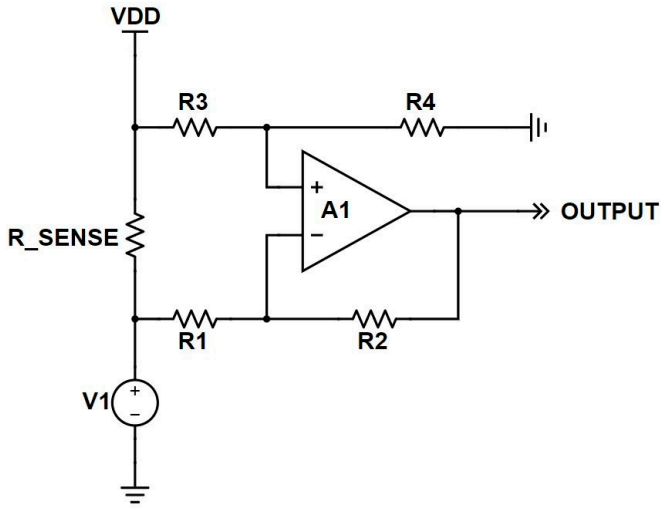


Figure 1. Unidirectional high-side current-sense-circuit schematic.

If we consider $R_1 = R_3$, $R_2 = R_4$ and neglect the mismatch between the resistors and the offset voltage, the current sense output value is:

$$OUTPUT = V_{R\_SENSE}\frac{R_2}{R_1} \tag{3}$$

By having the output correlated with the current, the system can decide, for example, when a battery is discharged. Unfortunately, in real-life applications, the offset voltage cannot be ignored and will impact the architecture's output. For high V_{OS} values, the system could perform maliciously, make an inaccurate decision and cause a malfunction due to the output value:

$$OUTPUT = \frac{R_2}{R_1}(V_{R\_SENSE} - V_{OS}) - V_{OS} \tag{4}$$

New state-of-the-art architectures have been implemented that reduce the offset voltage by an order of hundreds of µV (trimming or chopping methods are the best known nowadays), but these come with downsides, such as higher complexity, increased required time for IC designers in the development phase, increased production cost and increased part qualification before being released to the market). For example, trimming [12] requires a digital block that enables the op-amp's programming, activating the necessary bits to fit the offset voltage in the desired range. In addition, each circuit must be evaluated separately, since the offset is a random component that differs from part to part.

Chopper architectures use a clock signal, at least two chopping blocks and a low-pass or a notch filter [13], to surpass the V_{OS}. The design requires a multipath approach [14], with one path, called "null", which gives the offset voltage, e_n, CMRR and PSRR, and another called "main", which establishes the overall phase margin and the bandwidth. Process variation and mismatches between adjacent transistors, along with parasitic capacities and resistances in the layout, will alter the filters' and oscillators' paired frequencies, causing a ripple at the amplifier's output. To reduce this unwanted behavior, a ripple reduction loop [15] must be implemented, which will increase the chopper's complexity and manufacturing cost.

A more valuable approach that is efficient and generates cost savings involves using the source degeneration configuration [16] to control the transistor's current-mirror transconductance, which affects the offset voltage. In this case, no auxiliary subcircuits are required; thus, the complexity, non-conformities and error probability are diminished. A tighter offset voltage distribution should be obtained compared to the architecture where the source degeneration configuration is not applied. This solution is optimal in systems where improved parameter variation is mandatory, together with a reduced die area.

This paper shows a two-stage folded-cascode op-amp [17], where a source degeneration configuration is implemented to reduce the offset voltage without auxiliary subcircuits. Distinct methods that control the amplifier's offset voltage are also discussed and established. Different resistor values were tested to analyze their impact on the common-mode rejection ratio, power supply rejection ratio, bandwidth and phase margin. A comparison between the suggested design and the classical one, without degeneration, is also conducted.

This paper's structure is as follows: Section 2.1 presents the offset voltage calculation and evaluation for the two-stage op-amp with a folded cascode, excluding the source degeneration for the pMOS and nMOS current mirrors. In Section 2.2, source degeneration is introduced to improve the offset voltage, and the new equation for this parameter is calculated. Section 2.3 demonstrates that in order to realize an offset voltage reduction, high-precision resistors are required to reduce the mismatch between adjacent resistors, and our state-of-the-art thin-film resistors are introduced. Section 3 presents schematic-level simulations using three resistor values for the pMOS and nMOS source degeneration alongside a comparison using three other resistor types (high-poly resistors, poly resistors and well resistors) (Section 3.1). Post-layout simulations were carried out alongside a comparison with previously reported works in the literature (Section 3.2). Section 4 presents

the layout implementation for the op-amp with the finest overall performance. After this, the conclusions of this work are established.

2. Design and Implementation

The following section presents the offset voltage calculation and evaluation for the two-stage op-amp with a folded cascode excluding and including the source degeneration, alongside this paper's state-of-the-art resistor, which reduces the mismatch between these passive components to improve and reduce the V_{OS} standard deviation.

2.1. Offset Voltage in Two-Stage Op-Amp with Folded Cascode

The two-stage op-amp with a folded cascode is presented next, together with the main contributors to the offset voltage. This design is the starting point for the improved and more efficient version presented in this paper. The schematic is shown in Figure 2. Only the pMOS input differential pair $M_1 - M_2$ is displayed for a simplified schematic, as the offset voltage contributors for the nMOS pair are similar. The $M_3 - M_4$ current mirrors convert the differential signal at the input into single-ended. The $M_5 - M_6$ current mirrors bias the folded-cascode structure. $M_7 - M_8$ and $M_9 - M_{10}$ establish the architectures' high gain. The transistors $M_{18} - M_{19}$ use a classic AB configuration [18] to confer the signals' rail-to-rail capability at the output. M_{17} is used to reduce the schematic systematic offset voltage. V_{B1} and V_{B2} establish the voltages applied at $M_7 - M_{10}$ cascode gates, and V_{B3} is the voltage that sets the current's value generated by $M_5 - M_6$.

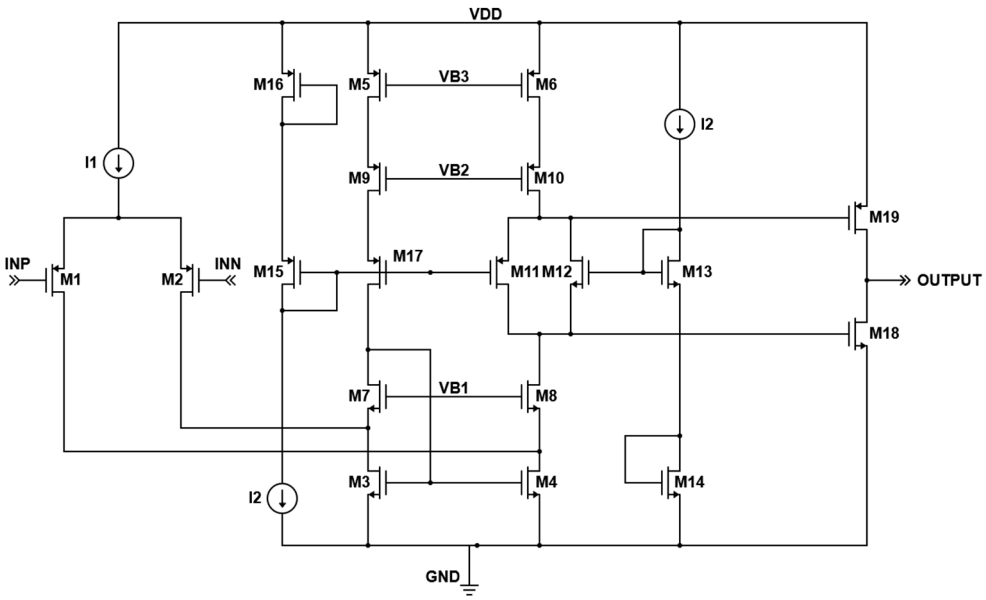


Figure 2. Two stage op-amp with folded cascode.

The output stage biasing is set using a trans-linear loop $M_{11} - M_{16}$ as follows:

$$V_{GS18} = V_{GS13} + V_{GS14} - V_{GS12} \tag{5}$$

$$V_{SG19} = V_{SG15} + V_{SG16} - V_{GS11} \tag{6}$$

The offset voltage in the presented architecture is a consequence at the op-amp inputs given by the offset current that is induced by the adjacent transistors' mismatch $M_1 - M_6$. Consider the drain-current equation:

$$I_D = \beta(V_{GS} - V_T)^2 \tag{7}$$

where I_D is the transistor drain current, β is the transconductance factor and V_T is the threshold voltage.

Differentiating the equation above, the mismatch current (offset) between two adjacent transistors is obtained:

$$\Delta I_D = I_D \frac{\Delta\beta}{\beta} + 2I_D \frac{(\Delta V_{GS} - \Delta V_T)}{V_{GS} - V_T} \tag{8}$$

where ΔI_D is the offset voltage, $\Delta\beta$ is the transconductance factor mismatch, ΔV_{GS} is the gate-source voltage mismatch and ΔV_T is the threshold voltage mismatch [19].

Considering $\Delta V_{GS} = 0$ (due to the fact that it represents the gate-source voltages for two adjacent transistors that are established only by the current passing through the transistors and does not depend on other parameters, as in the case of the threshold voltage, or it cannot be expressed using an additional equation, as in the source degeneration's case that will be presented in Section 2.2) and substituting it in Equation (8) $\frac{2I_D}{V_{GS}-V_T}$ as the transconductance for the MOS transistors, the offset current formula becomes:

$$\Delta I_D(I_{OS}) = I_D \frac{\Delta\beta}{\beta} - g_m \Delta V_T \tag{9}$$

In Figure 2, if we consider $I_{D5} = I_{D6} = 2I_{D1} = 2I_{D2}$, $I_{D3} = I_{D4} = 3I_{D1} = 3I_{D2}$ and refer to the amplifier's input by dividing I_{OS} by the differential pair's transconductance [20], the two-stage op-amps with the folded-cascode offset voltage is obtained:

$$V_{OS} = \frac{I_D}{g_{m1,2}} \left(\frac{\Delta\beta_{1,2}}{\beta_{1,2}} + 3\frac{\Delta\beta_{3,4}}{\beta_{3,4}} + 2\frac{\Delta\beta_{5,6}}{\beta_{5,6}} \right) - \Delta V_{T1,2} - \Delta V_{T3,4} \frac{g_{m3,4}}{g_{m1,2}} - \Delta V_{T5,6} \frac{g_{m5,6}}{g_{m1,2}} \tag{10}$$

To reduce the overall offset voltage distribution depicted in Equation (8), it is essential to increase the differential's transconductance by biasing the pair with a higher drain current simultaneously with the transistors' operating point in weak inversion [21]. The subthreshold operation for the differential pair does not impact the offset voltage equation; it affects only the transconductance being adjusted and depends directly proportionally on the drain current. Furthermore, the transconductance of the current mirrors $M_3 - M_6$ should be decreased by increasing the length and downsizing the width. The threshold voltage mismatch is controlled according to Pelgrom's theorem [22] by increasing the devices' area, and the optimal length for the differential pair must also be taken into account [8] to minimize the voltage noise density.

One of the downsides of the method presented above is the current-mirror overdrive voltage V_{OV}, which is inversely proportional to the $\frac{W}{L}$ ratio. A decrease in this value to reduce V_{OS} will lead to a higher overdrive voltage. This will cause a drop in the differential pair's V_{DS} voltage; thus, the amplifier's specifications could be affected, especially at common-mode voltages close to the supply. In Figure 2, if the common-mode voltage is set at 0 V (V_{SS}):

$$V_{SD1,2} = V_{SG1,2} - V_{DS3,4} \tag{11}$$

A reliable design should maintain the transistors' drain-source voltage at a value at least 100 mV higher than V_{OV}, regardless of the conditions in which the application works, to avoid the linear region [23] that can appear with process variation. Malfunctions can occur at higher temperatures, where the V_{SG} voltage drops. Nowadays, high-performance op-amps should manage to accommodate a common mode that covers at least the supply voltage range (preferably 0.1 V below and above), without affecting its specifications for the entire temperature range. The proposed architecture in this paper uses V_{SS} as the minimum common-mode voltage.

2.2. Source Degeneration as a Method to Reduce Offset Voltage Variations

The source degeneration technique [24] reduces the equivalent mutual transconductance G_m; thus, the offset voltage spread manages to be minimized, and the op-amp's

overall performance is heightened. The small-signal schematic for this configuration is presented in Figure 3.

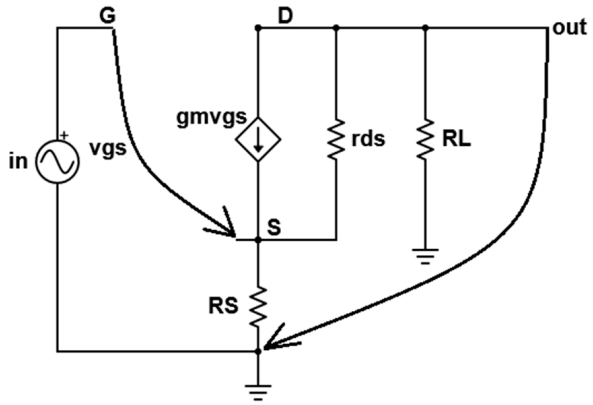


Figure 3. Small-signal schematic for common source with degeneration.

The equivalent mutual transconductance is:

$$G_m = \frac{1}{\frac{1}{g_m} + \frac{R_S}{g_m r_{ds}} + R_S} \simeq \frac{1}{R_S} \tag{12}$$

For a high transconductance and internal resistance, the G_m value is inversely proportional to the source resistor, and a lower offset voltage is ensured. Moreover, a high g_m is equivalent to a lower overdrive voltage, which will improve the amplifier's common-mode rejection ratio. It is important to mention that Equation (12) does not consider the mismatch found between the adjacent resistances that form the current mirrors' source degeneration. Figure 4 shows a basic current mirror that has implemented this technique.

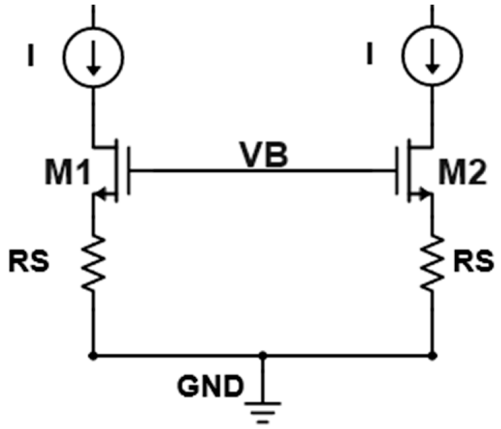


Figure 4. Current mirror with source degeneration implemented.

In this case, the mismatch due to the gate-source voltage can no longer be neglected due to:

$$V_{GS} = I_D R_S \tag{13}$$

$$\Delta V_{GS} = -(\Delta I_D R_S + \Delta R_S I_D) \tag{14}$$

where ΔR_S is the mismatch between the resistors.

Substituting Equation (14) in (8) and considering the transconductance formula explained above, the offset current between two adjacent transistors with source degeneration implemented is:

$$\Delta I_D(I_{OS}) = \frac{(I_D \frac{\Delta\beta}{\beta} - g_m \Delta V_T - g_m I_D \Delta R_S)}{1 + g_m R_S} \tag{15}$$

The first term in Equation (15) can be neglected due to its very small variation; thus, the final form for the offset current is:

$$\Delta I_D(I_{OS}) = -\frac{\Delta V_T + I_D \Delta R_S}{\frac{1}{g_m} + R_S} \tag{16}$$

A higher transconductance for the current mirrors means that the resistance given by the $\frac{1}{g_m}$ ratio can be neglected in the operational amplifier's offset voltage equation. Compared with Equation (10), the current mirror's g_m is in opposition to the first case, where it needs to be as low as possible to reduce the circuit's offset voltage. The new equation has the following formula:

$$V_{OS} = -\left(\Delta V_{T1,2} + \frac{\Delta V_{T3,4}}{g_{m1,2} R_{S3,4}} + \frac{\Delta V_{T5,6}}{g_{m1,2} R_{S5,6}}\right) - \frac{I_D}{g_{m1,2}}\left(\frac{\Delta R_{S3,4}}{R_{S3,4}} + \frac{\Delta R_{S5,6}}{R_{S5,6}}\right) \tag{17}$$

where $R_{S3,4}$ and $R_{S5,6}$ are the $M_3 - M_4$, $M_5 - M_6$ transistors source degeneration resistors.

The higher the source degeneration resistance, the lower the transistors' threshold voltage mismatch. However, a drawback may arise due to the adjacent resistors' fluctuation (ΔR_S), which could lead in the end to higher offset voltage values. This topic is discussed in the next subsection, alongside the innovative solution proposed in this paper to overcome the resistors' variation.

2.3. High-Precision Thin-Film Resistors (SiCr) to Overcome Mismatch Influence

As mentioned above, an important aspect that must be considered in Equation (17) is the mismatch between the adjacent source degeneration resistors $R_{S3,4}$ and $R_{S5,6}$ when variations related to the manufacturing process appear. As a discrepancy comes out from $R_{S3,4}$ and $R_{S5,6}$, the folded-cascode branches are unbalanced due to the fact that currents $I_3 - I_4$ and $I_5 - I_6$ are not equal; thus, a supplementary offset voltage is inducted at the operational amplifier's input.

The mismatch between two adjacent resistors (ΔR_S) is the measured device ratio's deviation from the intended device ratio and is expressed as:

$$\Delta R_S = -\frac{R_1 r_2}{R_2 r_1} - 1 \tag{18}$$

where r_1 is the actual value of the first resistor, r_2 is the actual value of the second resistor, R_1 is the desired value for the first resistor and R_2 is the desired value for the second resistor.

The IC mismatch that can appear can be divided in two categories: systematic mismatch and random mismatch. The first one is design- and layout-related and can be easily anticipated and compensated. On the other hand, random variations are process-dependent (random dopant change, peripheral and areal variations, etc.), which are difficult to reduce and compensate. The higher the fluctuation between resistors, the greater the negative impact on the offset voltage.

The source degeneration described in this paper is implemented using state-of-the-art high-precision thin-film resistors (TFRs). These resistors are made with metallic film and are integrated into the back-end-of-line (BEOL) process; thus, they are available in analog BCD technology. The metallic alloy is composed of silicon–chromium (SiCr), which provides a typical accuracy of 0.1% for the resistor ratio (a much-improved mismatch compared to other resistor types) and a more stable resistance value over time; hence, the inconstancy is minimized, and a reduced offset voltage is achieved. The silicon–chromium resistors'

downside is the production cost: they are more expensive than those made with polysilicon, for example. A comparison between the proposed method and other resistor types used in the CMOS process is available in Section 3.1.

The final design for the proposed op-amp architecture is depicted in Figure 5. Transistor dimensions and other component values that form the circuit are listed in Table 1. All nMOS devices have their bulk connected to the source pin. This is possible due to the technological capability to allow IC designers to use isolated nMOS transistors; thus, no body effect is present. The term "isolated transistor" refers to an additional N+ buried layer utilized over the P substrate, which allows supplementary isolated P-well creation from the substrate through the NBL. The newly created P-well represents the transistor's bulk, thus allowing the bulk connection to the source.

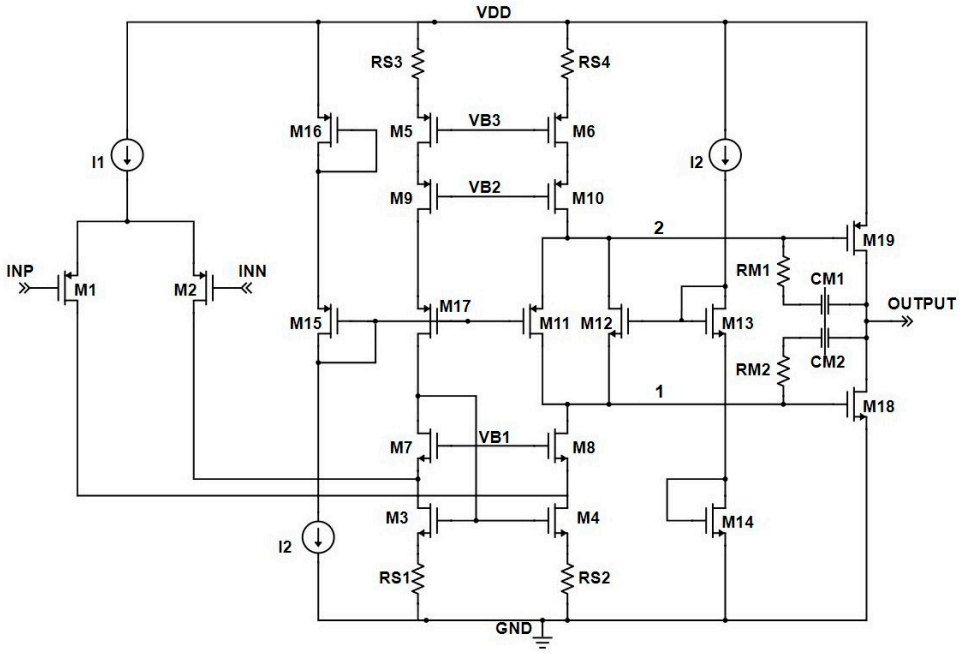


Figure 5. Proposed low-offset-voltage two-stage folded-cascode current-mirror source degeneration op-amp.

Table 1. Design parameters for low-offset-voltage op-amp.

Parameter	Value
RS1, RS2, RS3, RS4	500 Ω, 1 kΩ, 1.5 kΩ
CM1, CM2	7.35 pF
RM1, RM2—control op-amp and RS3, RS4 added	1.47 kΩ
RM1, RM2	3.45 kΩ
(W/L) M1–M2	1360/2 µm/µm
NF, multipliers M1–M2	1, 68
(W/L) M3–M4, M7–M8	720/10, 288/4 µm/µm
NF, multipliers M3–M4	1, 24
(W/L) M5–M6, M9–M10	480/10, 416/3 µm/µm
NF, multipliers M5–M6	2, 8
(W/L) M11, M15, M16, M17	96/1.2, 24/1.2, 12/0.5, 192/1.2 µm/µm
(W/L) M12, M13, M14	32/1.2, 8/1.2, 4/0.5 µm/µm
(W/L) M18, M19	156/0.5, 468/0.5 µm/µm
I1, I2 @ room temperature	40, 5 µA

I_1 and I_2 represent current mirrors, which bias the circuit with a proportional-to-absolute-temperature (PTAT) current, generated using a current source that has a bandgap

reference as the architecture's core, which is adjusted to ensure the desired current slope with temperature; thus, reduced variation with temperature for the differential stage transconductance is ensured. In Section 3, the process variations and devices' mismatch from the previously mentioned current source are also included; thus, increased accuracy for the results obtained is provided. The die areas for the current-mirror transistors $M_3 - M_4$ and $M_5 - M_6$ are increased by factors of 3 and 2 to accommodate g_m, alongside Miller compensation [25], to keep the same pole frequencies as in the classic two-stage op-amp case so that a parameter comparison can be made in Section 3.

This type of compensation splits the frequency at which the amplifier's first two poles are found; the dominant pole and the non-dominant one, along with the circuit's unity-gain bandwidth position, are given as [26]:

$$p_1 = -\frac{1}{g_{mOUT} R_{1,2} R_{OUT} C_{M1,2}} \tag{19}$$

$$p_2 = -\frac{g_{mOUT}}{C_{1,2} + C_{OUT}} \tag{20}$$

$$f_{UGBW} = \frac{g_{m1,2}}{2\pi C_{M1,2}} \tag{21}$$

where p_1 represents the dominant pole, g_{mOUT} is the output stage transconductance, $R_{1,2}$ is the output impedance seen in nodes 1 and 2, R_{OUT} is the output stage impedance, $C_{M1,2}$ is the Miller compensation, p_2 is the non-dominant pole, $C_{1,2}$ is the capacitance seen in nodes 1 and 2, C_{OUT} is the capacitance seen at the amplifier's output, and f_{UGBW} is the unity-gain bandwidth.

Furthermore, $R_{M1,2}$ moves the right-half-plane zero to the left; thus, it can contribute to obtaining improved stability by canceling one of the pole's effects, depending on the frequency at which it is located. This value can be easily determined given the equation [26]:

$$z_1 = \frac{1}{\left(\frac{1}{g_{mOUT}} - R_{M1,2}\right) C_{M1,2}} \tag{22}$$

where z_1 is the zero frequency's position.

3. Simulations and Results

The results for the proposed designed architectures following the circuit analysis are presented and discussed in this section. Two types of simulations were performed to evaluate the performance obtained: schematic-level (which includes only the devices used—Section 3.1) and parasitic extraction simulations (which also involves the parasitic effects' calculation induced by both devices used and the interconnecting wiring within the circuit—Section 3.2).

There are two types of approaches to transistors when simulating the circuit's schematic: using the multiplicity factor "m" or using arrays/vectors. The first method's advantage consists of the generated netlist file's increased processing speed, with the simulation times being considerably reduced. However, a disadvantage of using the multiplier is that the transistors are not multiplied "m" times in the netlist, so there could be inconsistencies when applying Monte Carlo mismatch to the devices. A method to increase the results' credibility provided by the simulator and to obtain a circuit netlist close to the one resulting from the PEX extraction is to use array/vector notations instead of multipliers; thus, each transistor is multiplied "m" times in the netlist. The second approach is preferred in this work in order to simulate and interpret the operational amplifiers' parameters.

3.1. Schematic-Level Simulations

Schematic-level simulations were performed in a Cadence Virtuoso environment work system using 250 nm CMOS technology. This node is preferred due to its stability at high

temperatures (low leakage current) and the reliability that it has proven over time in the automotive industry. The $M_5 - M_6$ current mirrors' source degeneration is discussed and analyzed first, along with the control amplifier. Three resistor values were implemented: 500 Ω, 1 kΩ and 1.5 kΩ. Considering that V_{B3} is set in such way that the current that flows through $M_5 - M_6$ is equal to the one generated by I_1, the voltage drop across the three resistors at room temperature is 20 mV, 40 mV and 60 mV, respectively. The V_{B2} voltage is adjusted to maintain a difference between V_{DS} and V_{OV} that is higher than 100 mV.

The testbench utilized to evaluate the operational amplifiers' current-mirror source degeneration DC parameters studied in this paper (such as the offset voltage, CMRR, PSRR, quiescent current) is presented in Figure 6. The supply voltage was set through the V_1 piecewise-linear voltage source (V_{PWL}), as well as the common-mode voltage, established by V_2. A reaction loop was implemented through the Voltage-Controlled Voltage Source ($VCVS$) E_1, which can be considered an ideal op-amp with differential output. Because this operational amplifier's voltage gain is equal to 1, the device-under-test (DUT) output is set at the circuit's half supply voltage (MID_VDD) ± the offset voltage. MID_VDD was also obtained through a $VCVS$ used as the ideal op-amp (E_2), with a voltage gain of 0.5 in this case. Through this method, the load resistance and capacitance, placed on the right in Figure 5, are immune to supply-voltage and common-mode variations; thus, the parameters' measurement errors are reduced to a minimum. The load resistance and capacitance values for which the phase margin and bandwidth are presented in this paper are 10 kΩ and 200 pF, respectively.

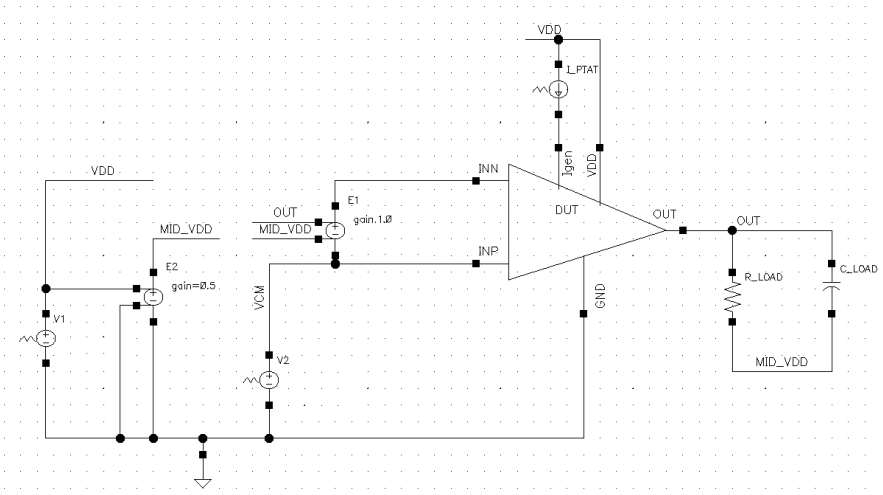


Figure 6. DC parameter evaluation testbench.

The offset standard deviation [27] results versus temperature are presented in Figure 7a,b, considering two supply voltages, 2.7 V and 5 V, and 1000 Monte Carlo [28] sampling points. The sampling method selected for this test was a low-discrepancy sequence since it covers the domain of interest more quickly and evenly compared to the random one. The common-mode voltage was fixed at $V_{DD} - 1.3V$, close to the pMOS differential stage operating limit.

When comparing the values obtained using the control op-amp with those obtained with source degeneration implemented, it is noticed that pMOS degeneration does not lead to significant improvements in the offset voltage standard deviation: from 282.2 µV (control op-amp, T = 27 °C) to 275.8 µV ($R_{SP} = 1.5$ kΩ, T = 27 °C). The same behavior is maintained over temperature.

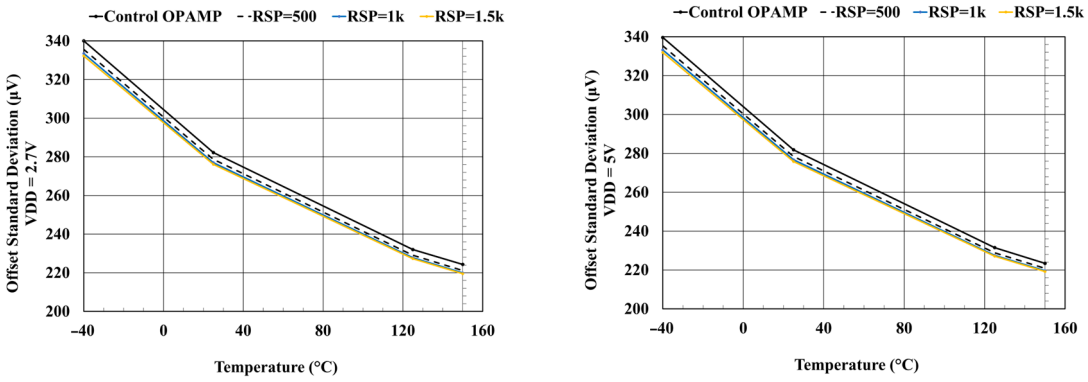


Figure 7. Offset voltage standard deviation distribution versus temperature, with RS3 = RS4 = RSP (considered a parameter) and RS1 = RS2 = RSN = 0 Ω. (**a**) VDD = 2.7 V; (**b**) VDD = 5 V.

As the pMOS source degeneration does not impact the differential pair's drain-source voltage, and thus, the common-mode rejection ratio is not affected, this parameter's analysis was performed only for the nMOS source degeneration.

The power supply rejection ratio behavior versus frequency is also discussed and analyzed for the control op-amp and the three resistor pairs in this subsection. To carry out these simulations, the testbench in Figure 6 was used, with only one minor change: in series with the V_1 supply voltage, an AC signal source with a 1 V magnitude was added, and the designed amplifiers' output response was monitored. The common-mode voltage was established as in the DC case at 0 V. The waveforms are depicted in Figure 8.

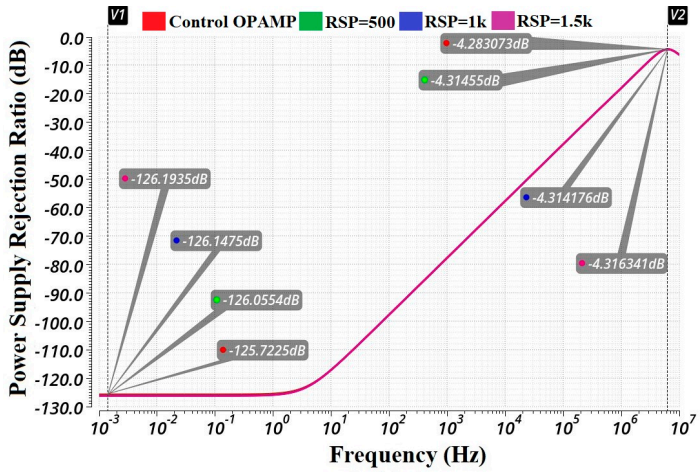


Figure 8. PSRR waveform behavior vs. frequency, with RS3 = RS4 = RSP (considered a parameter) and RS1 = RS2 = RSN = 0 Ω.

Their behavior is specific to a two-stage operational amplifier with a folded cascode: at low frequencies (<1–2 Hz), the values are constant and close to those obtained in DC. As the frequency increases, the ability to reject the power supply variation decreases, but it does not end up being positive. The values obtained for low frequencies are −125.72 dB (R_{SP} = 0 Ω), −126.05 dB (R_{SP} = 500 Ω), −126.14 dB (R_{SP} = 1 kΩ) and −126.19 dB (R_{SP} = 1.5 kΩ). The improvement is minimal, as the waveforms overlap regardless of the frequency, as in the PSRR cases obtained in DC.

Figure 9 illustrates the testbench required for the amplifiers' AC parameters (UGBW, phase margin, gain). It is very similar to the one used in the DC parameter case, but, in addition, it has an IPRB0 instance that serves as a signal source in the STB analysis, introducing a current that facilitates the parameter measurement mentioned above. In

DC, it behaves as a short, inserting a 0 Ω resistor in the circuit branch under study. V_1 and V_2 sources are DC in this testbench, with the common-mode voltage established at $V_{DD} - 1.3V$.

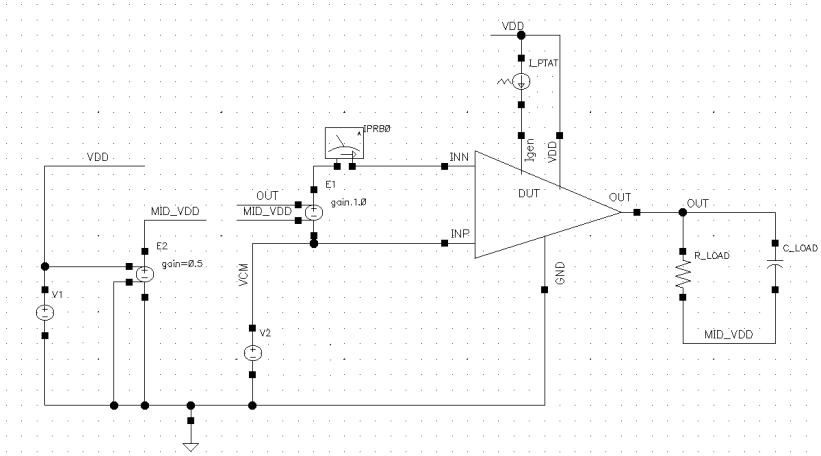


Figure 9. UGBW, phase margin and gain testbench schematic.

Figure 10a,b present the gain and phase margin waveforms for the control op-amp and the three implemented pMOS degeneration resistor values.

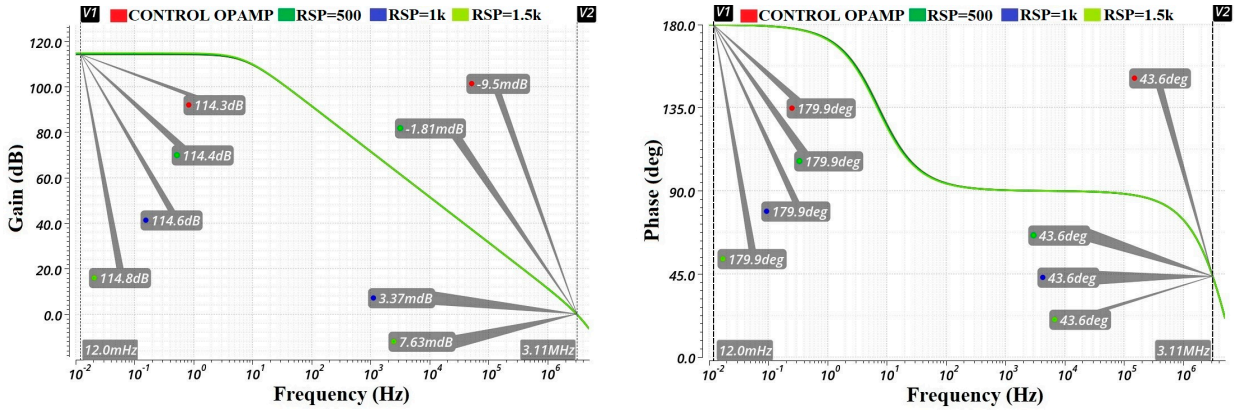


Figure 10. Bode plot waveforms for RS3 = RS4 = RSP (considered parameters) and RS1 = RS2 = RSN = 0 Ω. (**a**) Gain waveforms; (**b**) phase waveforms.

Total harmonic distortion (THD) was also measured for the same configurations as mentioned above. A sinusoid signal on the non-inverting input with a 1 kHz frequency and the same peak-to-peak value as the established common-mode signal was used for this test. The output and the inverting input were connected together. The results are listed in Table 2. Typical parameter outcomes for the discussed resistor values alongside the control op-amp, such as the power supply rejection ratio, unity-gain bandwidth, phase margin, voltage noise density and amplifier's overall gain [29], are also listed in Table 2 at a 5 V supply voltage. A slight improvement occurred in e_n for resistances higher than 1 kΩ, but this is insignificant in high-precision applications. All other parameters listed are unchanged, regardless of the values for R_{S3} and R_{S4}; thus, a maximum 6 µV upgrade is secured (R_{S3} = R_{S4} = 1.5 kΩ) for the offset voltage distribution compared to the control amplifier at room temperature, which is translated into a 36 µV maximum offset decrement if the mean ±6 sigma technique [30] for process improvement is considered. The PSRRs' typical values in DC were evaluated with the common mode set at 0 V.

Table 2. Op-amp parameter values for RS3 = RS4 = RSP source degeneration resistors (VDD = 5 V), T = 27 °C.

Parameter	Control Op-Amp	RSP = 500 Ω	RSP = 1 kΩ	RSP = 1.5 kΩ
UGBW (MHz)	3.11	3.11	3.11	3.11
Phase Margin	43.6	43.6	43.6	43.6
Voltage noise density @ 1 kHz (nV/sqrt (Hz))	32.04	32.11	31.96	31.85
Voltage noise density @ 10 kHz (nV/sqrt (Hz))	18.97	19.2	19.04	18.9
THD @ VCM = 2.5 V (%)	0.001756	0.00178	0.001764	0.001752
Gain (dB)	114.3	114.4	114.6	114.8
PSRR (dB)	124	124.1	124.3	124.5
Quiescent current (µA)	420.8	420.8	420.8	420.8

To further inspect the $M_3 - M_4$ nMOS current mirrors' source degeneration importance for the offset voltage and other parameters, R_{S3} and R_{S4} were set at 1 kΩ. The same testbenches and resistor values discussed for the pMOS current mirrors' case in this paper were used: 500 Ω, 1 kΩ and 1.5 kΩ. The voltage drop across these three resistors at room temperature is 30 mV, 60 mV and 90 mV, respectively. The V_{B1} voltage was adjusted to maintain the nMOS current mirrors' difference between V_{DS} and V_{OV} at higher than 100 mV.

Figure 11a,b show the offset voltage standard deviation considering the same two supply voltages (2.7 V, 5 V) and common-mode voltage, alongside the related histograms (Figure 11c,d and Table 3).

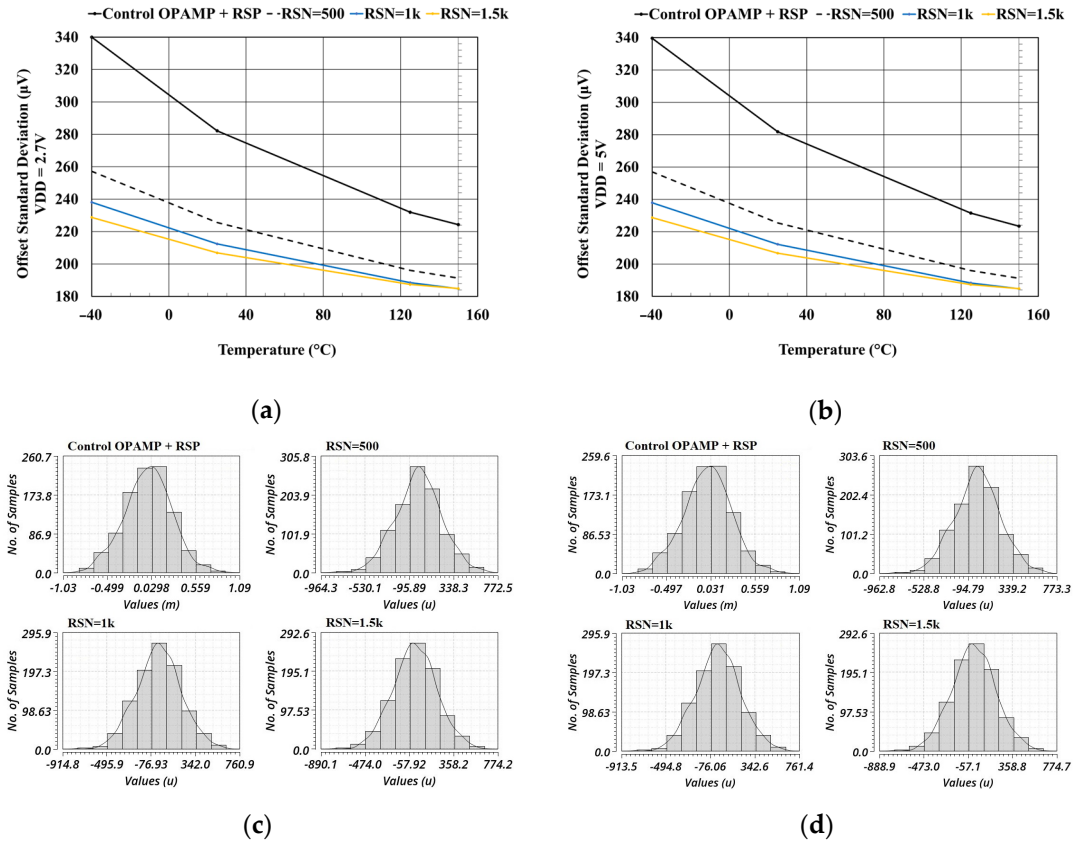


Figure 11. Offset standard deviation distribution versus temperature, with RS3 = RS4 = RSP = 1 kΩ and RS1 = RS2 = RSN (considered a parameter). (**a**) VDD = 2.7 V; (**b**) VDD = 5 V; (**c**) Monte Carlo histograms, T = 27 °C—VDD = 2.7 V; (**d**) Monte Carlo histograms, T = 27 °C—VDD = 5 V.

Table 3. Monte Carlo summary: Vos.

	VDD = 2.7 V				VDD = 5 V			
RSN	0 kΩ	500 Ω	1 kΩ	1.5 kΩ	0 kΩ	500 Ω	1 kΩ	1.5 kΩ
Mean (μV)	−10.59	−6.3	−6.5	−6.7	−9	−5.1	−5.3	−5.6
Std. Dev. (uV)	282.1	225.6	212.4	206.9	281.8	225.4	212.2	206.7

Compared to the first case discussed, where the transistors' source degeneration resistance increment after the 500 Ω value does not improve the offset variation distribution, in the nMOS current-mirror source degeneration case, the R_{S1} and R_{S2} increase leads to a parameter variation reduction. This is expected behavior, as, in $M_3 - M_4$ transistors, the differential and folded-cascode currents are summed, and the overall mismatch between them is decreased.

Typical values obtained are 225.6 μV (R_{S1} = R_{S2} = 500 Ω, both supply voltages), 212.4 μV (R_{S1} = R_{S2} = 1 kΩ, both supply voltages) and 206.9 μV (R_{S1} = R_{S2} = 1.5 kΩ, both supply voltages). This means that, compared to the original control op-amp, a 74.9 μV standard deviation reduction is accomplished and a ±1.241 mV maximum V_{OS} is obtained for R_{SN} = 1.5 kΩ. Furthermore, source degeneration improves the offset voltage drift with temperature [31] (TC_{VOS}): from 608.9$\frac{nV}{°C}$ reached in the control op-amp to 231$\frac{nV}{°C}$ using R_{S1} = R_{S2} = 1.5 kΩ. A diminished TC_{VOS} fluctuation means better op-amp precision, regardless of the ambient temperature at which it works in the system. Figure 11c,d illustrate the Monte Carlo histograms alongside a summary (Table 4), considering the control op-amp with pMOS source degeneration provided and the three nMOS source degeneration resistors' values implemented above at room temperature and both supply voltages for the offset voltage.

Table 4. Monte Carlo summary: CMRR.

	VDD = 2.7 V				VDD = 5 V			
RSN	0 kΩ	500 Ω	1 kΩ	1.5 kΩ	0 kΩ	500 Ω	1 kΩ	1.5 kΩ
Mean (nV/V)	481	274	364	477	64.6	22.5	45.6	78.4
Std. Dev. (nV/V)	198.2	171.1	188.1	214.9	107	77.16	70.77	72

As a consequence of the fact that $M_3 - M_4$ transistors' drains are connected alongside the differential stage's drains, the source degeneration's influence on the common-mode rejection ratio parameter was analyzed The common-mode signal range set at the amplifier's input is [V_{SS} to $V_{DD} - 1.3V$]. The results are summarized in Figure 12a,b. As can be seen from the graphs listed below, all of the chosen resistor configurations minimize the standard deviation fluctuations compared to the op-amp in which only R_{S3} and R_{S4} are included. The best outcome with increasing temperature was obtained for R_{S1} = R_{S2} = 500 Ω, with maxima of 539.9$\frac{nV}{V}$($V_{DD} = 2.7V$) and 177.7$\frac{nV}{V}$($V_{DD} = 5V$) achieved with increasing temperature.

However, minimizing the offset voltage distribution using source degeneration has a drawback. Raising the resistors' values leads to a higher voltage across them; thus, the differential drain-source voltage is reduced, leading to a higher CMRR standard deviation variation over the entire range of temperatures (the same voltage difference between $M_3 - M_4$ transistors' V_{DS} and V_{OV} is maintained as in the control amplifier's and R_{S3} and R_{S4} cases). This behavior can be noticed in Figure 12a,b, where for the 1.5 kΩ value, the standard deviation increases to 1982$\frac{nV}{V}$($V_{DD} = 2.7V$) and 675.7$\frac{nV}{V}$($V_{DD} = 5V$) with increasing temperature. At room temperature, the three waveforms are tighter, with maximum differences of 43.8$\frac{nV}{V}$($V_{DD} = 2.7V$) and 5.15$\frac{nV}{V}$($V_{DD} = 5V$) between them.

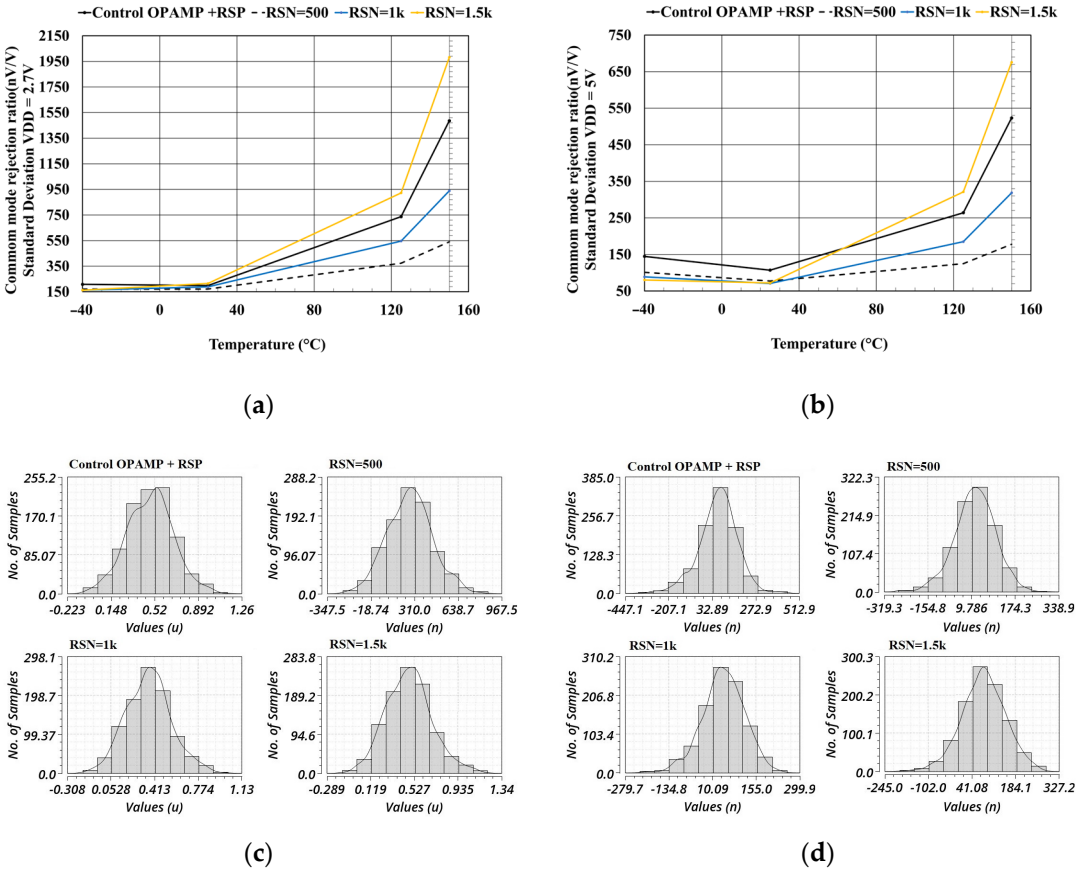


Figure 12. Common-mode rejection ratio deviation distribution versus temperature, with RS3 = RS4 = RSP = 1 kΩ and RS1 = RS2 = RSN (considered a parameter). (**a**) VDD = 2.7 V; (**b**) VDD = 5 V; (**c**) Monte Carlo histograms, T = 27 °C—VDD = 2.7 V; (**d**) Monte Carlo histograms, T = 27 °C—VDD = 5 V.

Figure 12c,d illustrate the Monte Carlo histograms considering the control op-amp with pMOS source degeneration implemented and the three resistor values implemented above at room temperature and both supply voltages for the CMRR. The IC designers must choose a compromise between the offset voltage and CMRR, depending on the application's environment and conditions in which the amplifier is to be used.

Process variations [32] can affect the op-amp's main parameters. To evaluate the circuits' performance considering this aspect, slow and fast corner simulations were performed using the Monte Carlo sampling method, with 1000 points being allocated per temperature corner, in order to obtain accurate results. The same configurations described for the nMOS transistors' source degeneration were utilized. In the slow corner (Figure 13a—offset voltage; Figure 13b—common-mode rejection ratio), the transistor's threshold point is shifted to a higher value; thus, a higher voltage is required to turn the devices on.

Only the 5 V supply voltage is analyzed here due to the op-amp's high PSRR; thus, the same results are expected, regardless of the supply voltage. Compared to Figure 11b, where typical process variations are implemented, no major shift in the offset distribution can be spotted, with the waveforms being approximately the same, with a variation of a few µV for each individual case: 281.8 µV vs. 281.1 µV (control op-amp and RSP included), 225.4 µV vs. 224.6 µV (R_{S1} = R_{S2} = 500 Ω), 121.2 µV vs. 210.7 µV (R_{S1} = R_{S2} = 1 kΩ) and 206.7 µV vs. 205.4 µV (R_{S1} = R_{S2} = 1.5 kΩ) (room-temperature results only). The common-mode rejection ratio standard deviation improves for all analyzed schematics at room temperature due to the higher source-gate voltage in the differential stage, with the R_{S1} = R_{S2} = 500 Ω graph having the lowest variation with temperature, while

$R_{S1} = R_{S2} = 1.5$ kΩ has the highest. The minimum standard deviation is reached at 25 °C with 1.5 kΩ resistance: $69.2\frac{nV}{V}$.

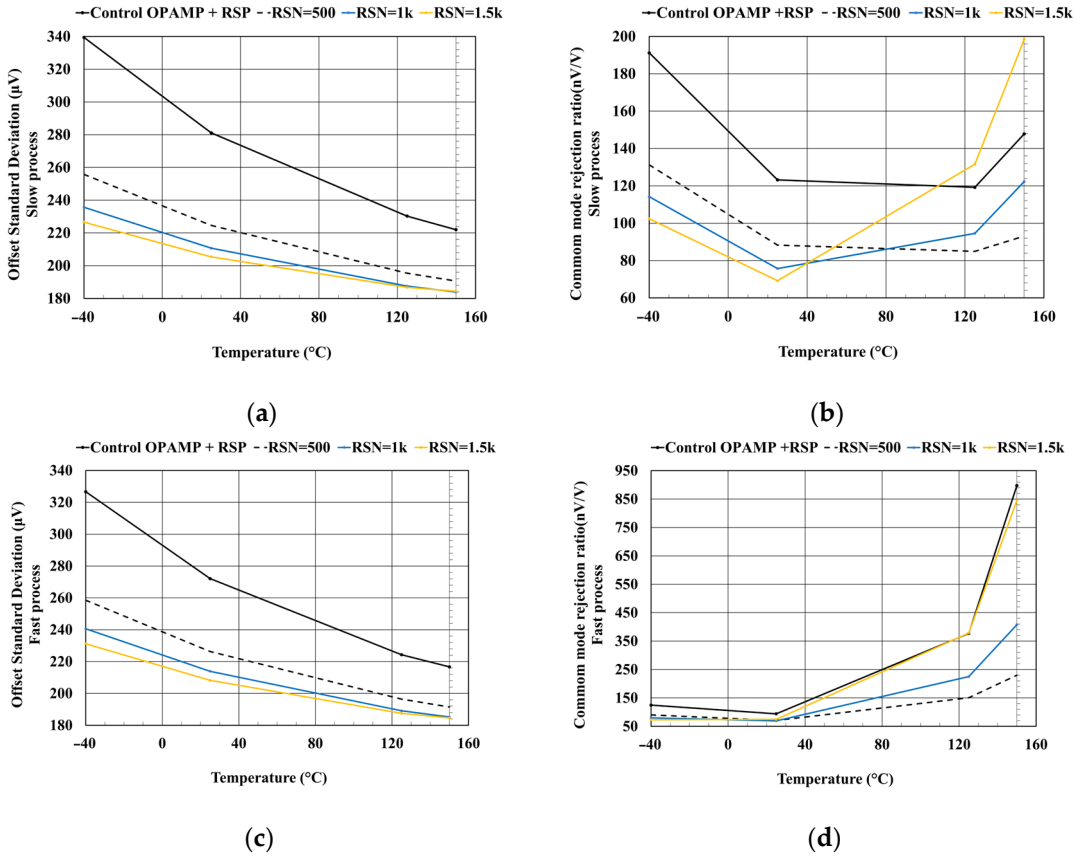


Figure 13. Process variation's influence, with VDD = 5 V, RS3 = RS4 = RSP = 1 kΩ, and RS1 = RS2 = RSN (considered a parameter). (**a**) Slow—offset voltage standard deviation distribution; (**b**) slow—CMRR standard deviation distribution; (**c**) fast—offset voltage standard deviation distribution; (**d**) fast—CMRR standard deviation distribution.

In the fast corner (Figure 13c,d), the transistor's threshold point is shifted to a lower value, leading to a decreased voltage needed to turn the devices on. In comparison with Figure 11b, the offset voltage standard deviation graphs are approximately the same as in the slow-corner process, with a variation of a few µV for each individual case. Considering that the differential pair's source-gate voltage is reduced in this corner, the common-mode rejection ratio is automatically impacted, with a higher standard distribution obtained for all temperatures, compared with Figure 12b.

Despite the process variations that can occur in the circuit manufacturing process, the schematic-level simulations' outcomes prove that the proposed technique increases the amplifier's precision and performance, with cost savings and a die area reduction also obtained, in contrast to the control op-amp and other architectures that offer higher complexity.

The power supply rejection ratio behavior versus frequency when the nMOS source degeneration resistors are added is depicted in Figure 14. An improvement in the values at low frequencies can be observed, exactly as in the PSRR cases simulated in DC and presented in Table 3. As the frequency increases, the waveforms overlap. The lowest PSRR results are obtained at around −5 dB, but at a frequency much higher than the amplifiers' unity-gain bandwidths. The values reached for low frequencies are −128.28 dB ($R_{SN} = 500$ Ω), −128.8 dB ($R_{SN} = 1$ kΩ) and −129.14 dB ($R_{SN} = 1.5$ kΩ).

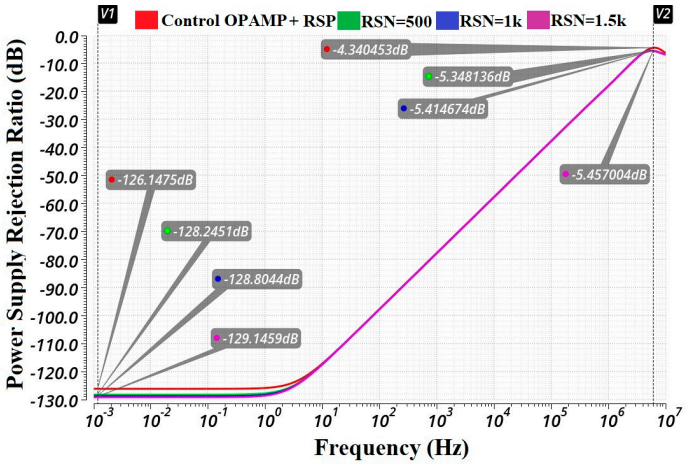


Figure 14. PSRR waveforms behavior vs. frequency, with RS3 = RS4 = RSP = 1 kΩ and RS1 = RS2 = RSN (considered parameters).

Following the results obtained with the three resistor values used in nMOS source degeneration, the best results for all of the operational amplifier's parameters are confirmed for $R_{S1} = R_{S2} = 1$ kΩ. In Section 2.3, it was stated that state-of-the-art high-precision thin-film resistors (silicon–chromium as the metallic alloy), which have better matching than other resistor types, were implemented to achieve an offset voltage reduction. To support the high-precision source degeneration method presented in this work and the benefits to the operational amplifier's performance, a comparison using three other resistor types (high-poly resistors, poly resistors and well resistors) was made. The same width was kept for all resistors; thus, a comparison between the resistors' die areas could be made. The models accompanying these SiCr resistors have been measured and verified in other developed ICs. The results obtained for the offset voltage are presented in Figure 15a (VDD = 2.7 V) and Figure 15b (VDD = 5 V), together with the related histograms at room temperature (Figure 15c,d and Table 5). The lengths and widths are specified in Table 6.

The offset voltage drift with temperature using high-poly resistors shows the best performance among the four graphs analyzed, but the standard deviation's average value versus temperature (296.2 μV) is much higher than that obtained using high-precision resistors (205.9 μV). Also, the highest offset voltage standard deviation is obtained for the high-poly resistors (292.4 μV at room temperature). The high-poly results at room temperature are even higher than those obtained with the original control op-amp (282.2 μV). This is due to the weak pairing that this type of resistor has.

Using the poly resistors, the results for the offset voltage standard deviation improve but are still higher than in the case when our high-precision resistors were used (11.7 μV at room temperature, 15.7 μV over temperature). The well resistor's offset voltage standard deviations are the closest to those achieved with high-precision thin-film resistors, but the drawback is the higher offset voltage drift with temperature ($381\frac{nV}{^\circ C}$ vs. $280.5\frac{nV}{^\circ C}$).

The minimum die area is obtained with the high-poly and proposed high-precision resistors (63.1 μm^2), while the largest necessary die area is in the poly-resistor case (325.38 μm^2). Thus, in addition to the very good mismatch that the innovative high-precision thin-film resistors presented in this paper have, they also require a smaller area, an essential advantage nowadays, when lower ICs are mandatory.

These results highlight the fact that, even if according to Equation (17) from Section 2.2, the offset voltage should be reduced, the mismatch between the resistors when the variations related to the manufacturing process appear (random dopant change, peripheral and areal variations etc.) cannot be neglected, and high-precision resistors should be implemented, such as the innovative ones presented in this paper.

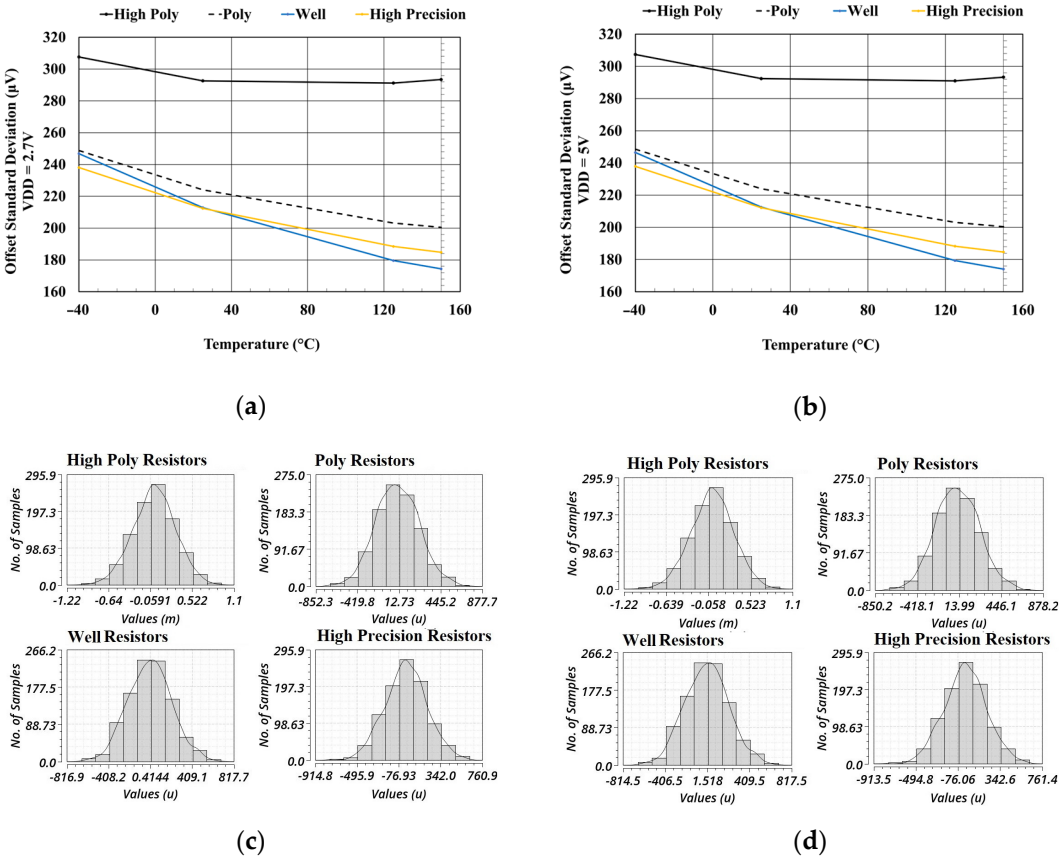


Figure 15. Offset voltage standard deviation distribution versus temperature with different resistor types implemented. (**a**) VDD = 2.7 V; (**b**) VDD = 5 V; (**c**) Monte Carlo histograms, T = 27 °C—VDD = 2.7 V; (**d**) Monte Carlo histograms, T = 27 °C—VDD = 5 V.

Table 5. Monte Carlo summary: different types of resistors.

	VDD = 2.7 V				VDD = 5 V			
Type of Res.	High P.	Poly	Well	Precision	High P.	Poly	Well	Precision
Mean (µV/V)	−6.6	−5.86	−5.89	−6.49	−5.48	−4.7	−4.73	−5.33
Std. Dev. (µV/V)	292.4	224.1	212.8	212.3	292.4	224	212.6	212.2

Table 6. Lengths and widths of the implemented resistors.

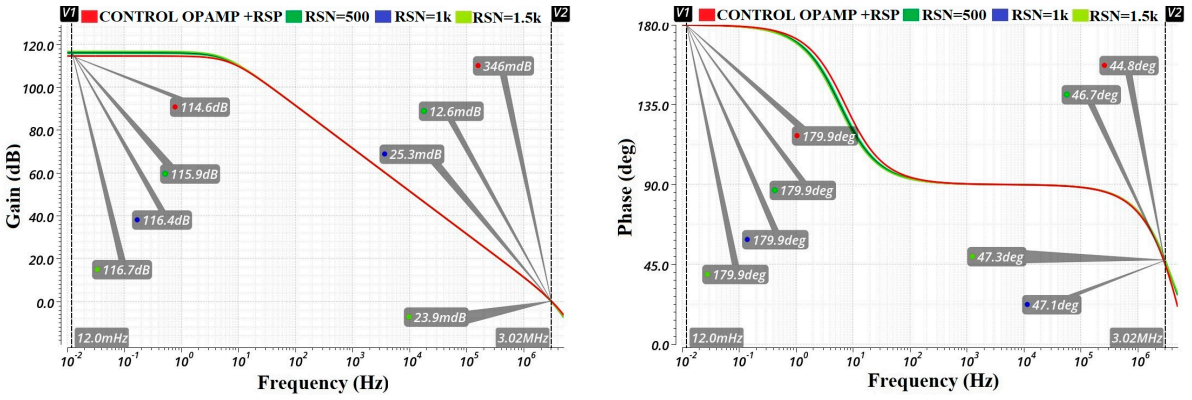
Type of Resistor	Length (µm)	Width (µm)
High Poly	6.4	9.86
Poly	33	
Well	7.5	
High Precision	6.4	

A summary of the results obtained at room temperature using the discussed designs is presented in Table 7. The offset voltage standard deviation could further be diminished by increasing the differential pair's die area to obtain a maximum offset voltage lower than 1 mV, but this paper focuses on the performance that can be achieved using the current mirrors' source degeneration.

Table 7. Results summary at T = 27 °C, with 5 V supply voltage, RS1 = RS2 = RSN added, and RS3 = RS4 = RSP = 1 kΩ.

Parameter	Control Op-Amp + RSP	RSN = 500 Ω	RSN = 1 kΩ	RSN = 1.5 kΩ
UGBW (MHz)	3.11	3.02	3.02	3.02
Phase Margin	43.6	46.7	47.03	47.21
Voltage noise density @ 1 kHz (nV/sqrt (Hz))	31.96	28.15	25.4	23.69
Voltage noise density @ 10 kHz (nV/sqrt (Hz))	19.04	18.8	17.63	16.87
THD @ VCM = 2.5 V (%)	0.001764	0.002032	0.001982	0.001945
Gain (dB)	114.6	115.9	116.4	116.7
Offset voltage std. dev. (μV)	276.7	225.4	212.2	206.8
CMRR std. dev. (nV/V)	107	77.16	70.77	72.01
PSRR (dB)	124.3	125.8	126.3	126.6
Quiescent current (μA)	420.8	420.8	420.8	420.8

Increasing the R_{S1} and R_{S2} values for offset optimization also reduces the voltage noise density, with a 25.87% improvement from 31.96$\frac{nV}{sqrt(Hz)}$ to 23.69$\frac{nV}{sqrt(Hz)}$ at 1 kHz frequency. A tighter gap between the two e_n measured also means that the frequency corner is reached faster, by scaling down the range in which the $\frac{1}{f}$ component is dominant. This performance is realized without increasing the quiescent current, which is important in low-power applications. The unity-gain bandwidth has a 0.1 MHz contraction, as can be seen in Table 7 and in Figure 16a,b. All other parameters do not have important changes in their values.



(**a**) (**b**)

Figure 16. Bode plot waveforms for RS3 = RS4 = RSP = 1 kΩ and RS1 = RS2 = RSN (considered parameters). (**a**) Gain waveforms; (**b**) phase waveforms.

3.2. Post-Layout Simulations

Parasitic effects, such as the wires' resistance and vertical and coupled capacitances, can influence the amplifiers' parameters and functionality. To evaluate the circuit performance considering these aspects, post-layout simulations were performed using the parasitic extraction method (PEX—R_C_CC). Furthermore, post-layout results are the most accurate and provide an overview of how the proposed architecture will behave in silicon. Only the op-amp with R_{S1} = R_{S2} = R_{S3} = R_{S4} = 1 kΩ is analyzed in this subsection due to the fact that it presented the best development in specifications in the schematic-level evaluation at room and with varying temperature compared to the other discussed situations. The architecture can also be configured to include the 500 Ω and 1 kΩ alternatives, with just a metal fix needed.

The same testbenches presented in Section 3.1 were also utilized in PEX simulations. This is due to the spectre file resulting from the parasitic element extraction. The components that compose the operational amplifier designed in this work were extracted directly from the layout, so each transistor has an independently generated number of fingers equivalent to the multiplicity established by design, just like in the case of using vector/array notation. In the end, the spectre file was inserted into the simulation environment that calls the discussed testbenches, thus making the transition between schematic-level simulations and PEX. A comparison showing slight differences between PEX netlist and schematic-level development for offset and common-mode rejection ratio standard deviations is presented in Figure 17a,b.

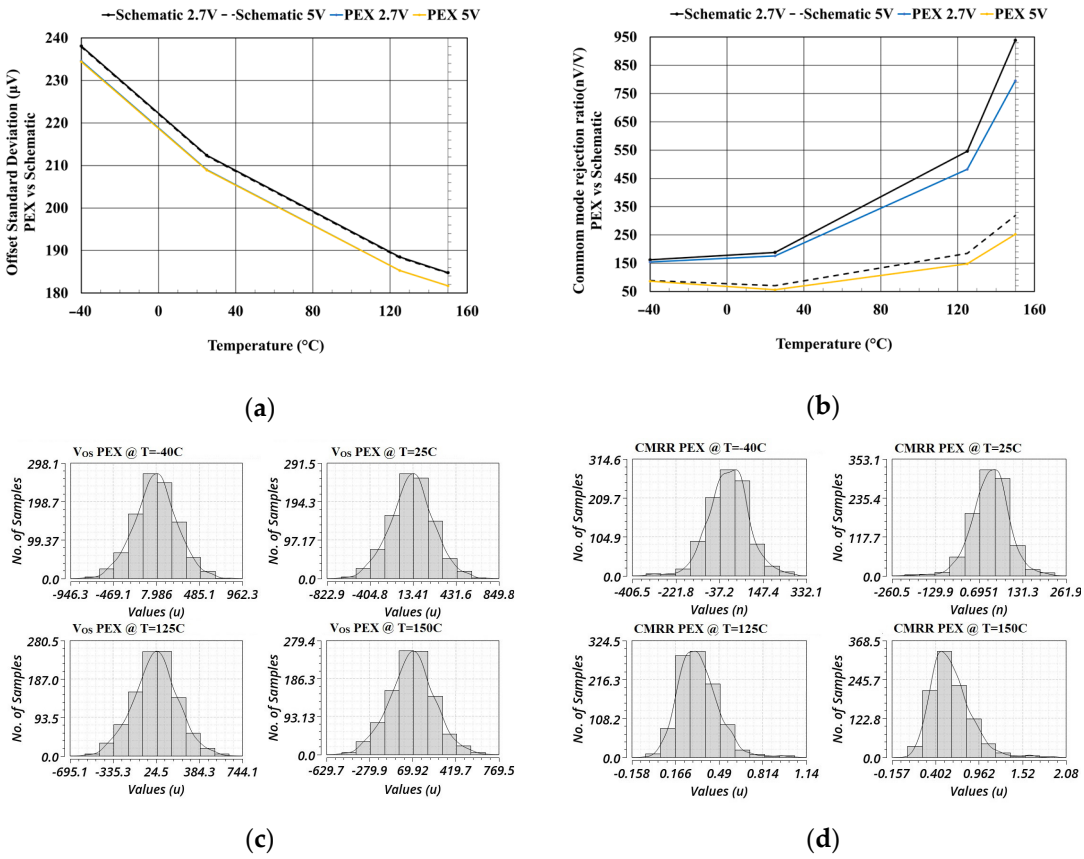


Figure 17. Parasitic extraction simulation results. (**a**) Offset standard deviation comparison; (**b**) common-mode rejection ratio standard deviation comparison; (**c**) V_{OS} histograms at different temperatures, VDD = 5 V; (**d**) CMRR histograms at different temperatures, VDD = 5 V.

A minor improvement in the offset voltage standard deviation compared to previously obtained results can be noticed in Figure 17a. This is due to the precise matching accomplished in the layout on the devices that influence this parameter and the source degeneration resistors, which cannot be implemented in the schematic. Furthermore, the resistors' values that compose the source degeneration for both pMOS and nMOS current mirrors are higher after parasitic extraction than the ones implemented in schematic-level simulations due to the wires' resistances that are in series with them. A 209 µV standard deviation at room temperature is measured for both supply voltages, with 3.5 µV less compared to the schematic level that uses vector/array notations. As the temperature increases, the difference between the schematic-level values and those obtained by extracting the parasitic effects remains relatively the same, with a variation between 3 and 3.3 µV being noticed. This is expected behavior due to the large number of points used in the Monte Carlo simulations that calculate the desired statistical parameters: 1000. The overlap between the curvatures with V_{DD} seen in Figure 17a suggests that the offset variation

caused by the supply voltage's fluctuation is also preserved with parasitic extraction, and a good power supply rejection ratio is achieved.

Figure 17b shows the CMRR fluctuation with temperature for the schematic implemented with vectors/arrays and PEX results. The variation between schematic-level simulations and PEX is comparable to the offset voltage case, regardless of the supply voltage, thus confirming the fact that the circuit layout does not negatively influence the amplifier's parameters. Figure 17c presents the Monte Carlo histograms for the offset voltage versus temperature for the 5 V supply voltage, and Figure 17d shows the Monte Carlo histograms for the common-mode rejection ratio versus temperature for the same supply voltage as mentioned above. The means and standard deviations for these histograms are showed in Table 8.

Table 8. PEX Monte Carlo summary: Vos and CMRR.

	Vos					CMRR			
Temp (°C)	−40	25	125	150		−40	25	125	150
Mean (µV)	−1.4	3.6	18	62.9	Mean (nV/V)	1.5	34.4	336.4	600.4
Std. Dev. (uV)	234.4	208.8	185.1	181.5	Std. Dev (nV/V)	86.4	56	148	252.4

To further increase the confidence in the source degeneration method to reduce the offset voltage, Monte Carlo simulations with a total of 1000 points per temperature after PEX in slow and fast corners were performed. As explained earlier in this paper, these corners represent the worst-case scenario in which the proposed circuit could operate. The high-precision resistors were also shifted, and mismatch was applied between them alongside the transistors. Furthermore, the models accompanying the devices used in this work are very precise, being verified after thousands of architectures that were designed with them. The offset voltage histograms at different temperatures for a 5 V supply voltage are presented in Figure 18a for the slow corner and Figure 18b for the fast corner alongside a summary (Table 9).

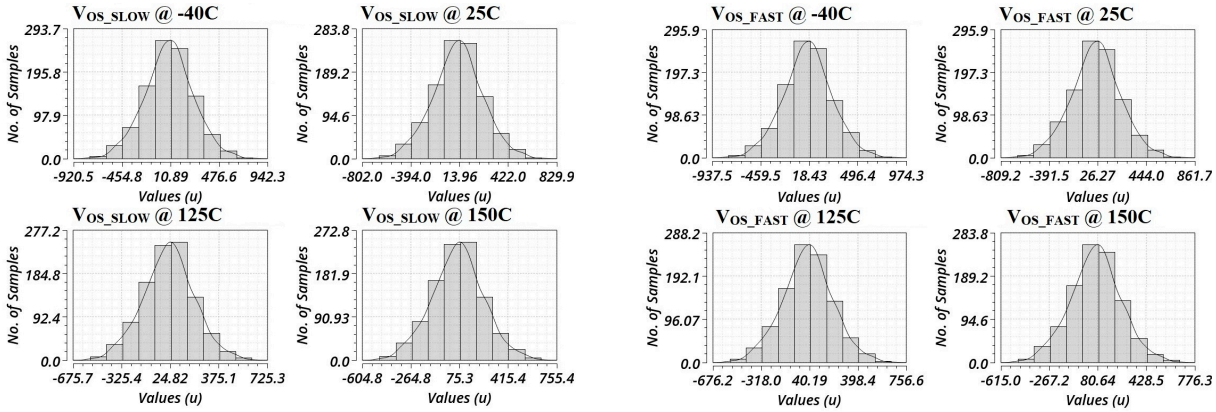


Figure 18. Parasitic extraction histogram results in corners for offset voltage: (**a**) slow; (**b**) fast.

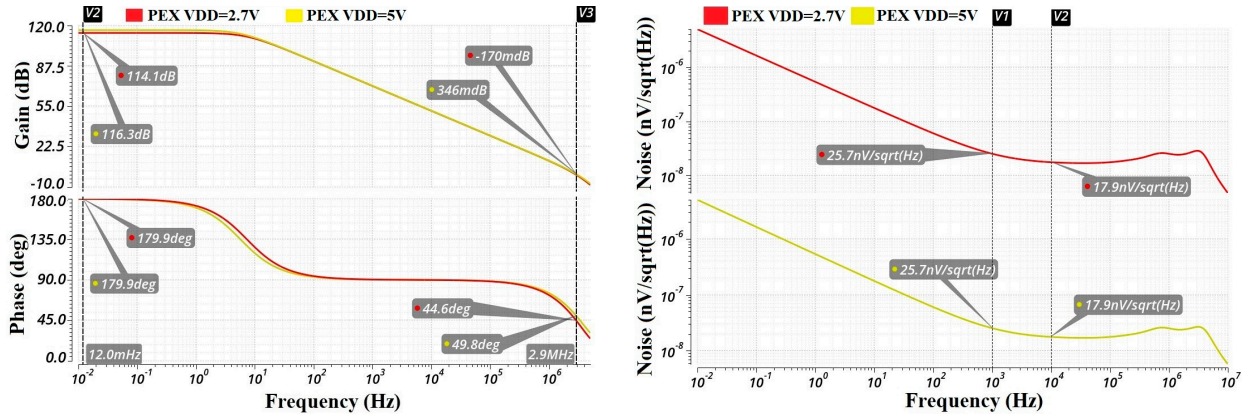
Table 9. PEX Monte Carlo summary: Vos—slow and fast.

	Slow				Fast			
Temp (°C)	−40	25	125	150	−40	25	125	150
Mean (µV)	−3.7	−0.2	13	62.1	2.9	10.1	25.3	64.4
Std. Dev. (uV)	232.6	207.7	184.5	181	237.3	210.7	185.9	182.2

Comparing the results achieved in slow and fast corners with the histograms from Figure 17c for a typical corner, a gradual increase in the mean and the standard deviation

values, applicable to all temperatures, is evident. At room temperature, the standard deviation fluctuation is imperceptible (207.21 µV slow vs. 208.86 µV typical vs. 210.73 µV fast), and for the mean values, the maximum variation is 13.54 uV. However, it is known that the two-stage operational amplifier with a folded cascode presents a systematic offset due to the unbalanced voltages in the folded stage. The highest mean values are found at 150 °C, regardless of the simulation corner.

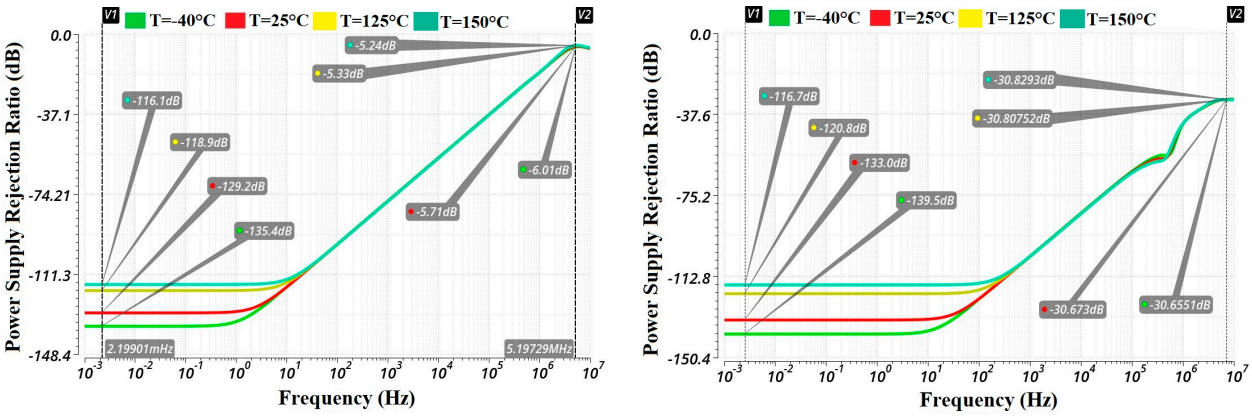
The gain and phase margin (Figure 19a) alongside the voltage noise density (Figure 19b) waveforms are illustrated and analyzed next. No major shifts before and after PEX can be spotted, meaning that the parasitic and coupled capacities in the layout are reduced to a minimum; thus, no disruption to the circuit functionality is introduced.



(**a**) (**b**)

Figure 19. AC and noise performance after PEX. (**a**) Gain and phase waveforms; (**b**) voltage noise density.

The power supply rejection ratio with PEX at different temperatures versus frequency is also discussed and analyzed in this subsection. The waveforms are depicted in Figure 20. Unaltered behavior and similar values are obtained at room temperature ($PSRR_+$—red waveform) as when schematic-level simulations were carried out (−128.8 dB vs. −129.2 dB at low frequencies, −5.41 dB vs. −5.71 dB minimum point at high frequencies). A negative power supply rejection ratio ($PSRR_-$—green waveform) is also disclosed, with superior performance at higher frequencies.



(**a**) (**b**)

Figure 20. Frequency response at different temperatures (**a**) $PSRR_+$; (**b**) $PSRR_-$.

The common-mode rejection ratio with PEX at different temperatures versus frequency is presented in Figure 21. A summary of the PEX results obtained in this paper is presented

in Table 10 alongside a comparison between these results and the ones obtained in the schematic-level analysis.

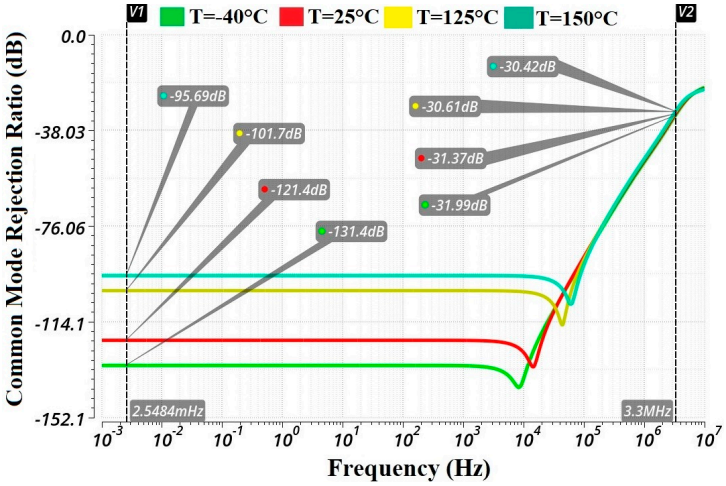


Figure 21. CMRR frequency response at different temperatures.

Table 10. Results summary for PEX simulations, T = 27 °C.

Parameter	VDD = 2.7 V	VDD = 5 V	Schematic Level, VDD = 5 V
UGBW (MHz)	2.86	2.98	3.02
Phase Margin	45	48.9	47.03
Voltage noise density @ 1 kHz (nV/sqrt (Hz))	25.7	25.7	25.4
Voltage noise density @ 10 kHz (nV/sqrt (Hz))	17.89	17.79	17.63
THD	0.01	0.002016	0.001982
Gain (dB)	114.1	116.3	116.4
Offset voltage std. dev. (μV)	209	208.9	212.2
CMRR std. dev. (nV/V)	175.7	56.08	70.77
PSRR (dB)	126.5		126.3
Quiescent current (μA)	420.8	420.8	420.8

Table 11 lists the proposed two-stage folded cascode with the source degeneration resistors' operational amplifier architecture performance obtained with parasitic effects (post-layout simulations) compared to previously reported works in the literature (measurement and simulation results). The proposed technique has superior DC performance to [33–39] in terms of the maximum offset voltage, open loop gain, CMRR and PSRR. The load capacitance is 2 times higher than that in [35] and from 13 to 40 times higher than those in the rest of the reported works. To have a fair comparison with the previous works, the following well-known figure of merit (FoM) is used:

$$FoM = \frac{UGBW \times C_L}{I_Q} \tag{23}$$

Our proposed operational amplifier with high-precision source degeneration implemented shows a superior FoM compared to all reported works in Table 11.

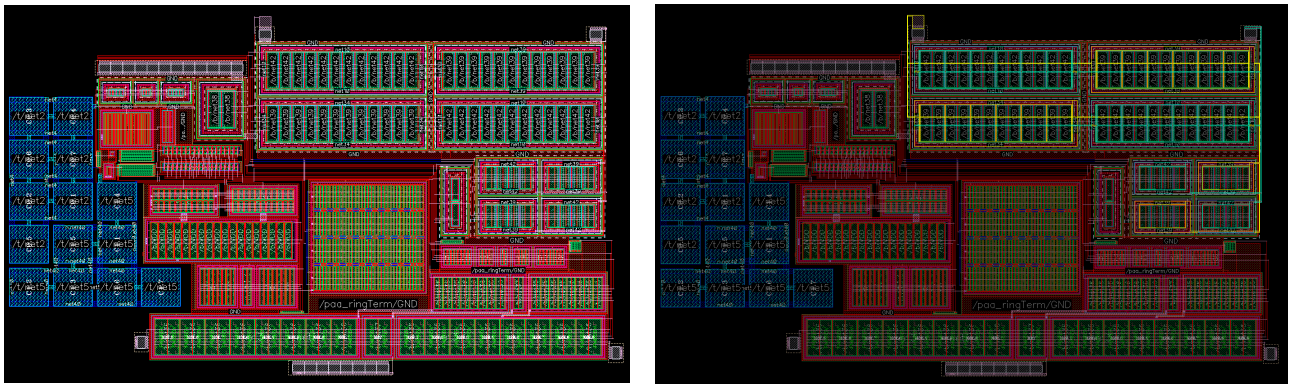
Table 11. Comparison results with previously reported work.

Parameter	[33]	[34]	[35]	[36]	[37]	[38]	[39]	This Work
Technology (nm)	1200	350	180	350	350	180	180	250
Supply voltage (V)	5	3.3	1.8	1	0.9	1.8	0.5	5
Gain (dB)	64.5	NA	98	88.3	65	54.9	78	116.3
Offset voltage (mV)	2.8 (no sample size)	1.898 (no sample size)	±14.6 (3σ)	10 (2 sample size)	5.7 (6 sample size)	±7.6 (3σ)	2.78 (8 sample size)	±1.254 (6σ)
Voltage noise density @ 1 kHz (nV/sqrt (Hz))	NA	NA	250 @ 100 kHz	60 @ 1 MHz	65 @ 100 kHz	NA	650	25.7
CMRR (dB)	65	NA	NA	40	45	NA	113.8	129.46
PSRR (dB)	70	NA	NA	40	51	NA	84.4	126.5
UGBW (MHz)	0.233	10	21	11.67	1	70.4	0.0075	2.98
Phase margin (°)	70	62	71	66.1	60	79.8	59	48.9
Capacitive load (pF)	NA	5	100	15	10	5.6	15	200
Power consumption (μW)	12300	600	3000	197	24.3	720	0.0455	2105
Die area (mm^2)	0.098	NA	0.053	0.16	0.014	0.003	0.019	0.16
FoM (pF·MHz·V/μW)	NA	0.275	1.26	0.89	0.37	0.98	1.23	1.415

4. Layout Implementation

In this section, the proposed circuit layout is further analyzed and discussed. By focusing on the differential op-amp input stage, the primary objective is to avoid circuit variations by effectively matching the devices [40] used and minimizing the parasitic effects [41]. Various layout optimization techniques were applied, and parasitic extraction simulations were conducted to realize accurate analog circuit modeling.

The overall layout is shown in Figure 22a, where the differential input stage is positioned in the middle. In order to avoid circuit variations in device parameters, a cross-coupled common-centroid layout array is used. Additionally, it is important to employ source sharing between fingers from both input transistors and drain sharing between the same input transistors' fingers [42] to reduce the circuit's die area and further improve matching capabilities. The nMOS current mirror and nMOS cascode were implemented using a cross-coupled layout configuration, thus optimizing current matching. However, for the pMOS mirror and cascode, due to their bulk connections being tied to different potentials, the conventional options of the interdigitate or common-centroid array were not viable. In this case, the pMOS transistors were positioned in close proximity to each other, arranged in a linear configuration. In order to ensure optimal performance, the reference device was centrally located, with the other transistors on either side. In accordance with the schematic design, the M1 and M2 transistors implemented in the layout exhibit a multiplicity of 68 each. Similarly, the nMOS transistors, M3 and M4, demonstrate a multiplicity of 24 each, while the pMOS transistors, M5 and M6, have a multiplicity of 8 with a corresponding gate number of 2.



(**a**) (**b**)

Figure 22. Proposed circuit layout, with RS1 = RS2 = 1.5 kΩ, and RS3 = RS4 = 1 kΩ. (**a**) Overview; (**b**) resistor wire matching for offset reduction.

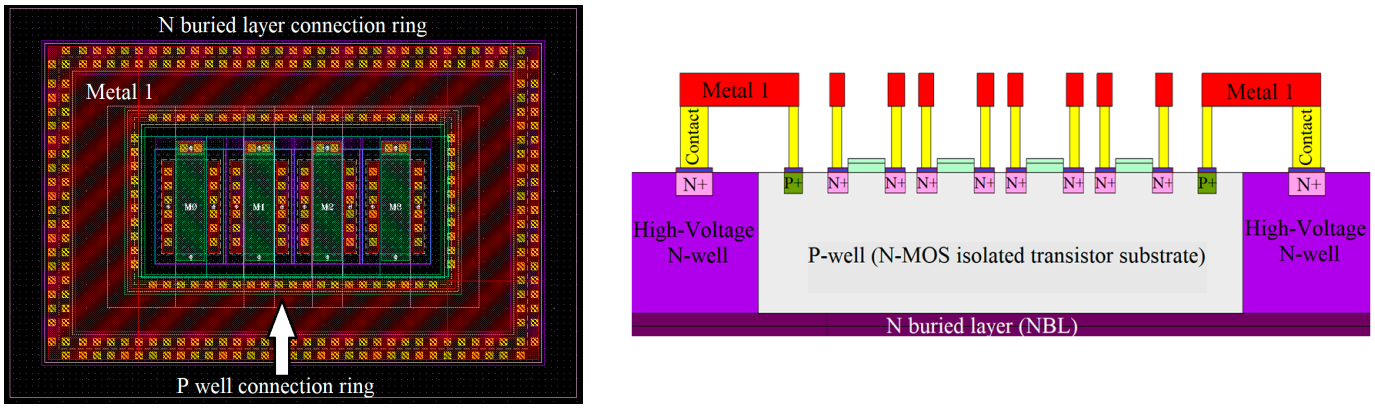
An issue that may arise in the layout is caused by the way in which the degeneration resistors are placed and interconnected in the circuit. They can introduce a systematic offset in the system, which is undesirable in applications that require high precision. These effects can be spotted only after the PEX method is handled, which involves calculating the parasitic effects induced by both the devices used and the interconnecting wiring within the circuit (wire and device capacitance, resistance and capacitive coupling). To overcome such a consequence, increased attention is paid to the two wires highlighted in Figure 22b. These run over the nMOS current mirror, ensuring the connection between the active devices and R_{S1} and R_{S2} resistors. It is essential to make the wires identical in terms of resistance. Through careful calculation and the adjustment of the wires' length, a minimum systematic offset voltage is achieved. The SiCr resistor layout view is presented in Figure 23. Two additional masks are required for the fabrication process. These masks are represented in the layout by the SiCr and SiCr body layers. The SiCr layer is manufactured between metal 1 and metal 2 and is aligned with the intermetal dielectric. To connect the SiCr layer with metal 2, via 1 is used. The SiCr body represents the SiCr etch area.

(**a**) (**b**)

Figure 23. SiCr layout implementation. (**a**) Layout view; (**b**) layer masks used.

Furthermore, the wires that connect the differential pair's drains could impact the offset voltage due to the parasitic capacities that can appear between the lines located on the same metal layer. A simple solution used in the layout presented above is to generate the

connections on a higher metal (m3) and to have an appropriate distance between them, thus reducing the capacitive coupling. The circuit presents no issues when layout vs. schematic (LVS) and design rule check (DRC) commands are executed. The total chip's die size is 523.89 × 305.12 µm. The utilized N+ buried layer (NBL), which connects to the P-well, is illustrated in Figure 24a. Given their distinct N-type and P-type characteristics, a diode forms between the two connection rings. To avoid potential forward bias issues, an essential step is connecting the NBL ring and P-well ring together using metal 1. This interconnection ensures that the diode remains non-conductive, maintaining proper functionality, as well as enhanced performance and circuit's reliability. The nMOS transistor's cross-section is presented in Figure 24b, highlighting the connection between the transistor's bulk (P-well) and the NBL.



(**a**) (**b**)

Figure 24. Isolated nMOS transistor. (**a**) Layout view; (**b**) cross-section.

5. Conclusions

This paper focuses on designing and implementing a source degeneration configuration to control the transistors' current-mirror transconductance, which impacts the offset voltage for a two-stage folded-cascode operational amplifier. Simpler complexity, cost savings and a die area reduction are obtained compared with other architectures, such as chopper or trimming. Simulations were performed using 250 nm CMOS technology. Three values for resistors were analyzed (500 Ω, 1 kΩ, 1.5 kΩ) for both the pMOS and nMOS current mirrors. Distinct methods that control the offset voltage parameter are also discussed and established. State-of-the-art thin-film resistors that use silicon–chromium as the metallic alloy were implemented to reduce mismatch variations between these passive components. A comparison between the offset voltage standard deviation obtained using different types of resistors and the one achieved with the high-precision resistor presented in this paper was also carried out. This method's impact on the amplifier's parameters, such as the common-mode rejection ratio, power supply rejection ratio, bandwidth, voltage noise density and phase margin, was also analyzed, alongside the process variation influence on the circuit functionality. A performance comparison between the proposed design and the classical one was made, and a summary is presented in Table 12. The resistors used to degenerate the pMOS current mirrors did not lead to significant improvements in amplifier's parameters, with only a 5–6 µV reduction in the offset voltage standard deviation being obtained. In contrast, the nMOS current mirrors' degeneration produced a remarkable improvement in the amplifier's parameters, with a 69.6 µV standard deviation reduction obtained compared to the original control op-amp, and a pre-layout ±1.273 mV maximum offset voltage at T = 27 °C was achieved using vector/array notations for the amplifier with the best overall performance (R_{S1} = R_{S2} = R_{S3} = R_{S4} = 1 kΩ). Post-layout simulations that included the parasitic effects were performed, with a ±1.254 mV maximum offset voltage obtained at room temperature. Monte Carlo simulations after PEX in slow and fast

corners were also performed to further increase the confidence in the suggested approach. These performance results were realized without increasing the quiescent current, which is important in low-power applications.

Table 12. Results comparison: VDD = 5 V, T = 27 °C.

Parameter	Control Op-Amp	Proposed Op-Amp PEX RS1 = RS2 = RSN = 1 kΩ RS3 = RS4 = RSP = 1 kΩ	Percentage Improvement (%)
UGBW (MHz)	3.11	2.98	−4.18
Phase margin	43.6	48.9	12.15
Voltage noise density @ 1 kHz (nV/sqrt (Hz))	32.04	25.57	20.19
Voltage noise density @ 10 kHz (nV/sqrt (Hz))	18.97	17.79	6.22
THD @ VCM = 2.5 V	0.001756	0.002016	−14.8
Gain (dB)	114.3	116.4	1.83
Offset voltage std. dev. (μV)	281.8	208.9	25.87
CMRR std. dev. (nV/V)	110.5	56.08	49.25
PSRR (dB)	124	126.5	2.01
Quiescent current (μA)	420.8	420.8	0

These results highlight the fact that the presented method using high-precision resistors can be used in precision op-amp architectures to minimize the offset voltage distribution and improve the voltage noise density and can further be incorporated into different systems where an op-amp presence is necessary.

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