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185–215 GHz CMOS Frequency Doubler with a Single Row Staggered Distribution Layout Design

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Abstract: This paper presents a 220 GHz × 2 amplifier–doubler chain composed of a rat-race balun, a 6-stage driver amplifier, and a frequency doubler. The presented amplifier–doubler chain was fabricated in commercial 40 nm bulk CMOS technology. The maximum cutoff frequency f_{max} for the NMOS transistor produced by this manufacturing process was 290 GHz. The saturation output power of the six-stage driver amplifier at 110 GHz was 11.5 dBm. The transistor of the frequency doubler consisted of a single-row interleaved Poly-Diffusion Contact balancing structure. Theoretically, the single-row interleaved Poly-Diffusion Contact balancing structure was able to effectively avoid parasitic components. The simulated results demonstrate that the presented structure achieves a higher output than the conventional designs. Based on these measured results, the presented amplifier–doubler chain provides a peak output power of 7.9 dBm at 200 GHz and a 3-dB bandwidth of 30 GHz. Based on the comparison with other reported results, the presented amplifier–doubler chain provides the highest output power among reported frequency doublers fabricated in CMOS technology.

Keywords: doubler; frequency multiplier; terahertz (THz); millimeter wave

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1. Introduction

The 220 GHz band is a frequency band of the millimeter wave [1]. This frequency band is not yet fully developed, and the spectrum resources are very rich. Moreover, this band has many advantages that electromagnetic waves in other frequency bands do not. The first one is the long transmission distance [2,3]. The 220 GHz band is a high-frequency band, so it is able to propagate over longer distances and is suitable for indoor communications [4,5] and urban canyons [6,7]. The second is the large bandwidth. The 220 GHz band has a large bandwidth, so it can support high-speed data transmission [8–12]. The third one is strong penetration [13,14]. Millimeter waves can penetrate walls and other obstacles: another reason for their suitability for indoor communications and communications in urban canyon environments. The fourth is that it is not easy to disturb them. Due to its shorter wavelength, the 220 GHz band has less interference compared to other frequency bands. These characteristics make the 220 GHz band a very useful frequency band, which is widely used in wireless communication [15,16], radar [17,18], satellite communication [19], and other fields [20].

Currently, the main approach to generating electromagnetic waves at the 220 GHz band is to obtain the local oscillator signal by oscillating at a low frequency and then multiply the frequency by the desired frequency band. This means that the frequency doubling circuit is crucial for generating the 220 GHz band signal.

The earliest frequency multiplier designs used in the 220 GHz band are mainly based on III–V family semiconductors [21]. This is due to the high insulation of group III–V substrates. Therefore, the High-Electron-Mobility Transistor high-electron-mobility Transistor (HEMT) and Heterojunction Bipolar Transistor (HBT) based on the III–V group materials

are used as the substrates' transistor can achieve low insertion loss [22,23], and the passive devices fabricated under the III–V group process have a good quality factor [24]. In recent years, with the increasing cut-off frequency of silicon-based processes, more and more reports have been reported of implementing a 220 GHz frequency multiplier using silicon [25,26]. Among silicon-based processes, the CMOS process is the most commercially valuable [27,28]. It has the advantages of low noise, high reliability, fast response, low power consumption, functionality, and economy. These advantages have led to an increasing number of studies focusing on the design of the frequency multiplier in the CMOS processes. In 2016, Navneet Sharma et al. demonstrated a 160–310 GHz frequency doubler for rotational spectroscopy with a driver amplifier in a 65 nm bulk CMOS process [29]. At 0-dBm input power, the measured output power (Pout) varied from 3 to −8 dBm. In 2021, Akifumi Kasamatsu et al. implemented a ×9 frequency multiplier chain with a 3-dB bandwidth of 213–233 GHz in a 40 nm bulk CMOS. The chain realized a 4.1 dBm peak output power without using power combining [30].

In this paper, an amplifier–doubler chain including an integrated 110 GHz rat race balancer, a driving amplifier (DA), and an active doubler with an output frequency covering 185–215 GHz was designed. The 110 GHz Rat race balancer converted the single-ended signal to a differential signal with low insertion losses. The drive amplifier (DA) used a sixth-order pseudo-differential structure to ensure sufficient power input to the frequency doubler. The structure of the frequency doubler used a single-row interleaved Poly-Diffusion Contact balancing structure to replace the traditional two-separated transistors' topology, which reduced the parasitic components of the frequency doubler. According to the results of the measurement, the output power of the frequency doubler reached 7.9 dBm.

2. Circuit Design

As shown in Figure 1, the presented amplifier–doubler chain was fabricated in commercial 40 nm bulk CMOS technology. The maximum cutoff frequency fmax of the NMOS transistor by this manufacturing process was 290 GHz. The supply voltages of VDD and VB were set to 0.9 V and 0.75 V, respectively.

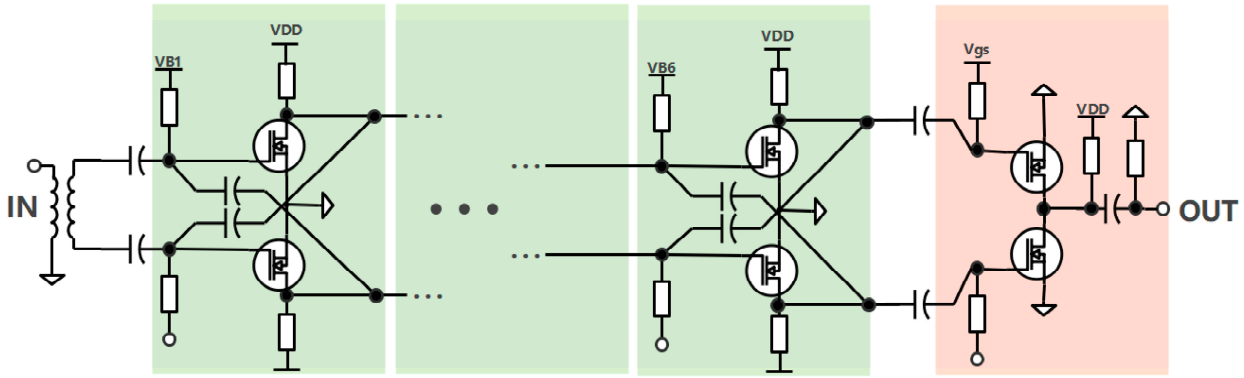


Figure 1. Diagram of the designed module of driver amplifier and frequency doubler.

At the input port of the designed amplifier–doubler chain, the single-ended signal was converted to a differential by an integrated 110 GHz rat race balun. The topology of the DA was given by the pseudo-difference structure, and the topology of the doubler was given by the push–push structure.

2.1. 110 GHz Balun and Driver Amplifier (DA)

Providing equally distributed in-phase and inverted-phase RF signals, rat race balun is a popular microwave passive component. It is used in many RF circuits [31]. Physical dimensions [32], frequency bandwidth [33], and insertion loss [34] are key indicators of balun's performance.

In this design, the rat race balun, which converts the signal from a single end to a differential form, was made of thick copper layers at the top of the chip. In this way, the insertion loss could be effectively reduced.

As shown in Figure 2, the rat-race balun consists of three λ/4 transmission lines and a $\frac{3}{4}\lambda$ transmission line. The performance of the rat-race balun with respect to the magnitude and phase imbalance was simulated, and the simulated results are shown in Figure 3. As shown in Figure 3, the S_{21} and S_{31} were about −4.4 dB and −4.8 dB, respectively, at 110 GHz for the rat-race balun.

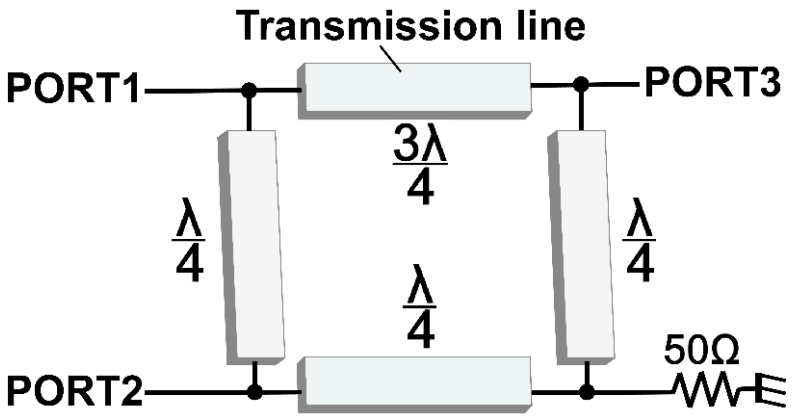


Figure 2. Schematic of the designed rat-race balun.

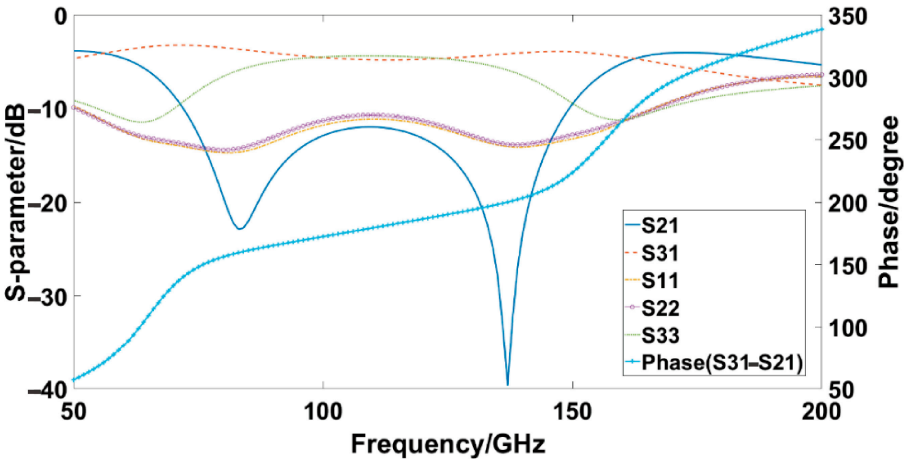
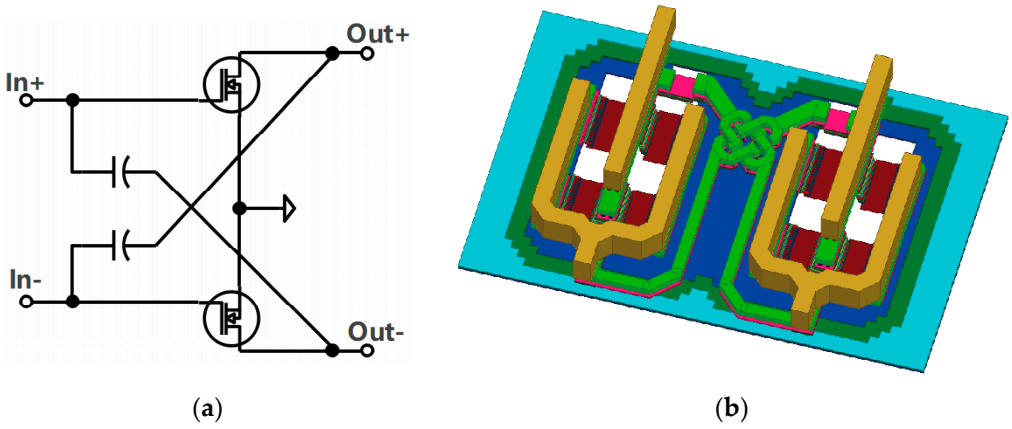


Figure 3. Simulated S-parameter of rat-race balun.

The design of the drive amplifier was similar to the design of the low-power amplifier. However, the signal amplified by the drive amplifier should be ensured to be as distortion-free as possible.

According to Figure 1, the circuit used to amplify the power level of the 110 GHz signal was a six-stage DA. The DA was designed as a pseudo-difference structure. This structure is characterized by the fact that the capacitance C_{gd} between the gate and drain of the transistor can be compensated by the capacitance of the cross-coupling. As shown in Figure 4, the final stage of DA consisted of four NMOS transistors. The input signal at this stage was uniformly distributed to feed the gates of the NMOS transistors. The drains of the transistors were connected at the center, while the source was directly connected to the ground.



(**a**) (**b**)

Figure 4. (**a**) Schematic and (**b**) Diagram of the final stage of the DA.

The output power versus the frequency of the six-stage DA was simulated with an input power level of −10 dBm, and the simulated results are shown in Figure 5. According to Figure 5, the DA gain became saturated at the 110 GHz frequency point. The saturation output power at 110 GHz was 11.5 dBm. Figure 5 shows that if the input power level of the DA was no less than −10 dBm, the power transmitted from the DA end to the frequency doubler could be up to 11.5 dBm.

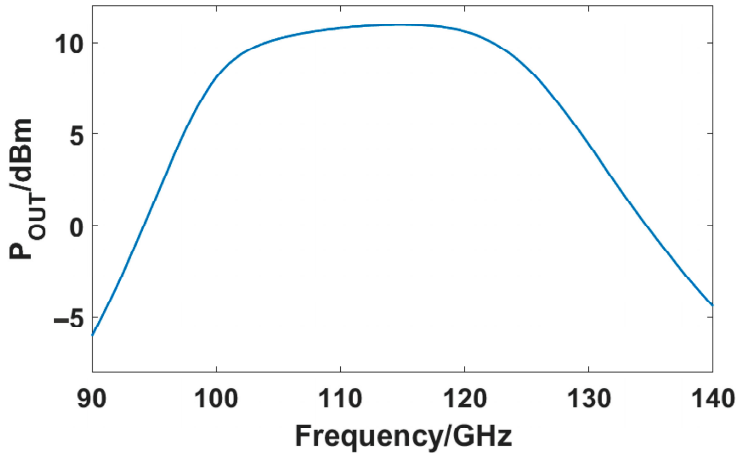


Figure 5. Simulated output power of the DA when input power was −10 dBm.

2.2. 220 GHz Frequency Doubler

As shown in Figure 1, the frequency doubler is a balanced structure that was constructed using NMOS transistors. Due to the nonlinearity of the NMOS transistors, the signal input from the DA into the NMOS transistor excited the high-order harmonics. The output matching network was used to extract the second harmonics among the high-order harmonics, achieving the frequency doubling function.

In the design of the frequency doubler layout, the transistor consists of a single-row of staggered distribution. As shown in Figure 6a, the single row interleaving distribution meant that the policies of two transistors were interleaved, and the diffusion contact used as the ground or output port was placed between two policies. These diffusion contacts were reused by both transistors.

As can be seen from Figure 6, this design had two advantages over the regular two-line design. First, the length of the metal connection line between the ground and output ports was effectively reduced, which effectively reduced the parasitic components. Second, the area of the layout became more compact because the number of diffusion contacts was

halved. The above discussion shows that the single-row interleaving distribution design can achieve more efficient parasitic parameters and a greater compact layout.

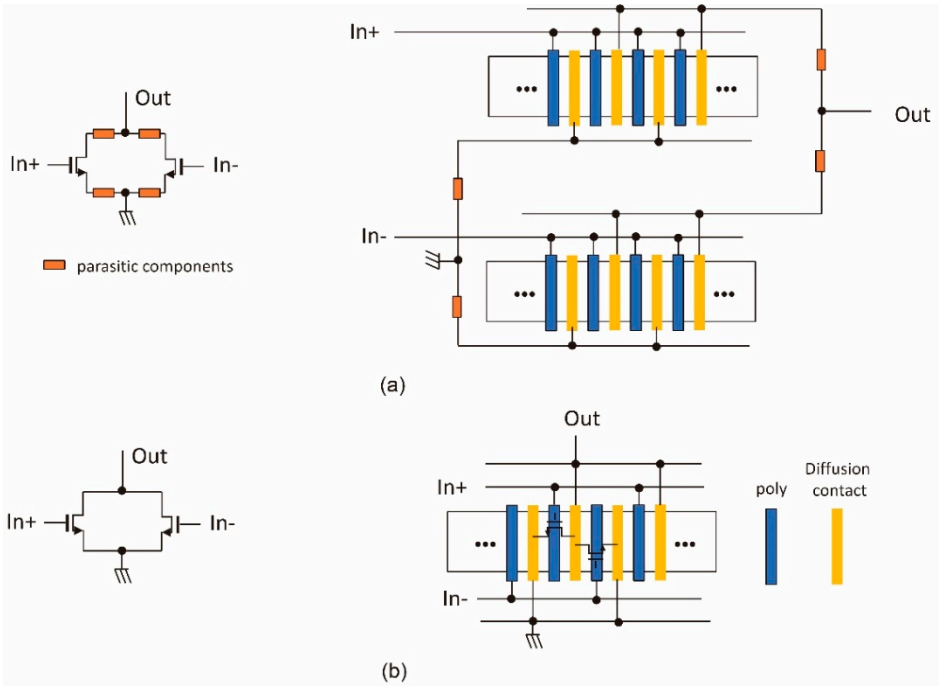


Figure 6. Schematic diagram of frequency doubler transistor design. (**a**) Regular two-line design; (**b**) Single-row interleaving distribution design.

The output power of a frequency doubler with a single-row interleaved Poly-Diffusion Contact balancing structure and a conventional structure at 220 GHz was simulated with different input power levels and different bias voltages. In the simulations, considering the absence of the transistor model in the cadence virtuoso with the structure, as shown in Figure 6b, the parallel connections of multiple single-gate ideal transistors were used equivalent to the single-row interleaving distribution structures. The simulated results of the power contours for different bias voltages are compared in Figure 7. According to Figure 7, the output power of a frequency doubler with the single-row interleaved Poly-Diffusion Contact balancing structure was able to reach a maximum of 7.8 dBm with a drive power of 11.5 dBm and a gate bias voltage V_{gs} of 0 V, while the output power of a frequency doubler with a conventional structure could only reach a maximum of 6.8 dBm with a drive power of 11 dBm and a gate bias voltage V_{gs} of 0 V.

Figure 8 illustrates the simulated output power versus the input power at 220 GHz with a bias voltage of 0 V for two frequency doublers with different structures. As can be seen from Figure 8, the frequency doubler with a single-row interleaved Poly-Diffusion Contact balancing structure can obtain a higher output power than the doubler with a conventional two-line structure when the power of the input doubler exceeds 7 dBm. In addition, the peak output power of the frequency doubler with a single-row interleaved Poly-Diffusion Contact balancing structure was 1 dB higher than that of the frequency doubler with a conventional two-line structure. In short, when the DA provided sufficient power, the frequency doubler with a single-row interleaved Poly-Diffusion Contact balancing structure could obtain higher output power than the frequency doubler with a conventional two-line structure. The difference in the peak output power between the two kinds of frequency doublers exceeded 1 dB. This comparison demonstrates that the presented structure can effectively reduce the parasitic components and achieve higher output power.

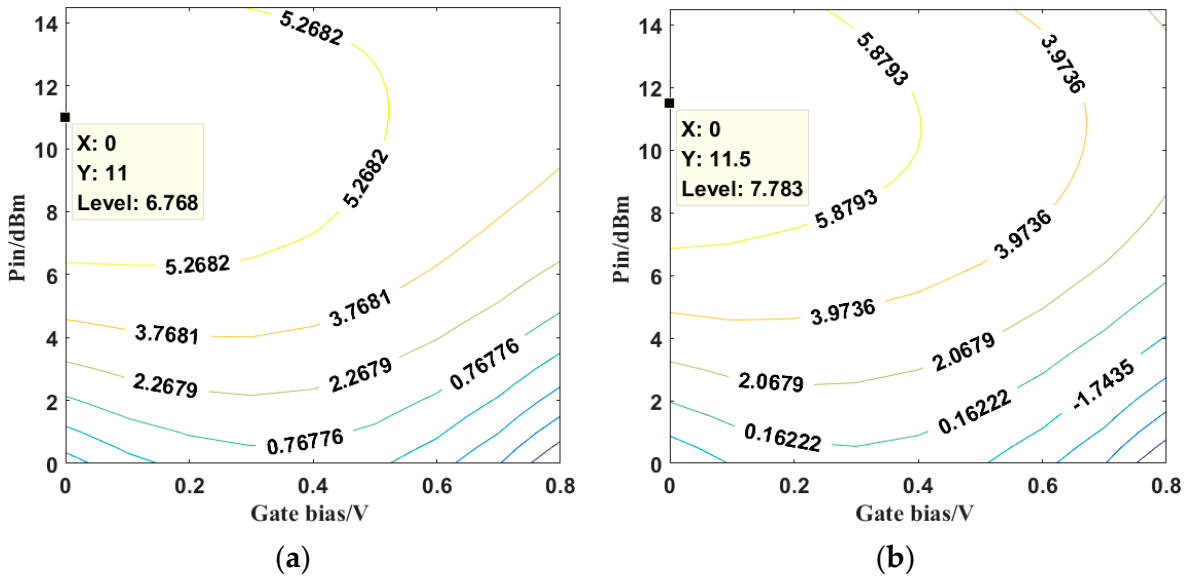


Figure 7. Simulated power contour of the frequency doubler for different input power levels and bias voltages at 220 GHz. (**a**) Single-row interleaving distribution design; (**b**) Conventional two-line design.

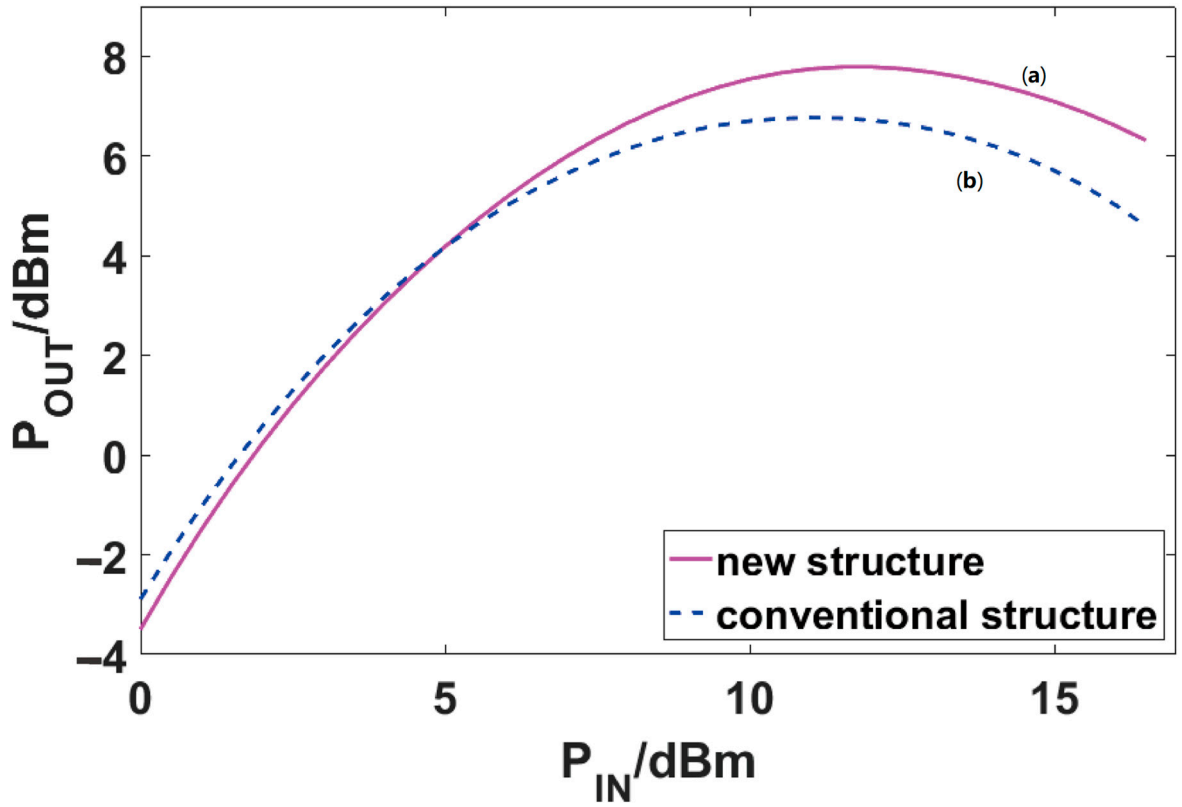


Figure 8. The relationship between the simulated output power and the input power of two kinds of frequency doublers with a different structure at 220 GHz when the bias voltage is set as 0 V. (**a**) Frequency doubler uses a single-row interleaved Poly-Diffusion Contact balancing structure; (**b**) Frequency doubler uses conventional two-line structure.

For a gate bias voltage V_{gs} of 0 V, Figure 9 shows the load pull diagram for a drive power of 11.5 dBm. As can be seen from Figure 9, the output power reached a maximum of 7.8 dBm. The topology of the output impedance matching network was L-C-L.

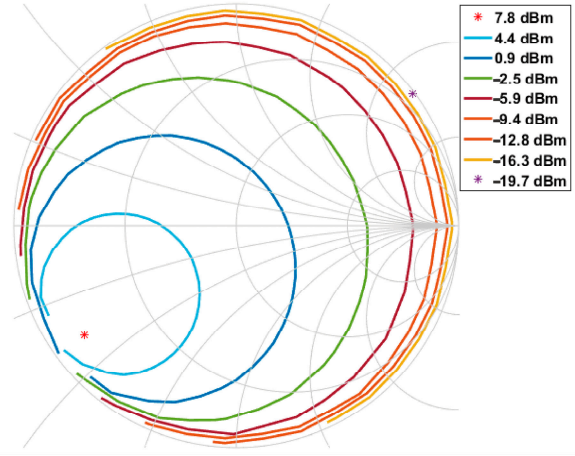


Figure 9. The load pull diagram with a drive power of 11.5 dBm.

3. Measurement

Figure 10 shows a microphotograph of the presented amplifier–doubler chain. According to Figure 10, the total area of the chip, including the pads, was 795 × 1000 μm^2. Measurements of the chip were performed on the wafer. The input port was probed using a Cascade Infinity WR 8 waveguide probe. The input signal generated by the commercial frequency multiplier module was injected into the chip, and the output power was measured by a VDI Erickson PM5 power meter with a waveguide taper. Two different measurement setups were used in the measurement since 220 GHz was the boundary of the WR3 and WR5 waveguides which needed to be probed with Cascade Infinity WR3 and WR5 waveguide probes, respectively.

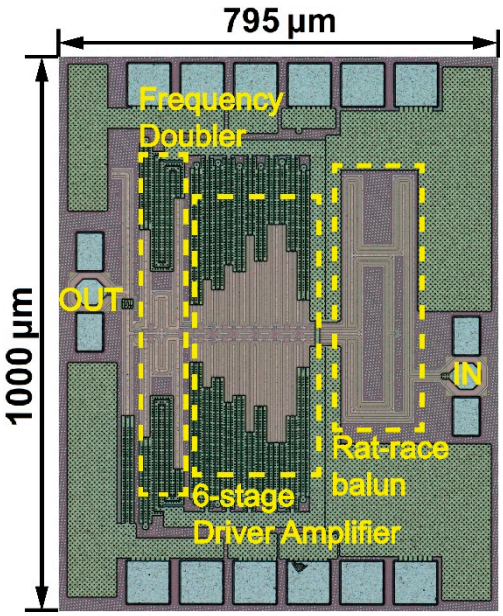


Figure 10. The micrograph of the presented amplifier–doubler chain.

The results of the measurement are shown in Figure 11. According to Figure 11, the presented amplifier–doubler chain reached its peak output power of 7.9 dBm at 200 GHz, and the 3 dB bandwidth was 30 GHz (from 185 GHz to 215 GHz).

Table 1 shows the performance of this frequency doubler compared to state-of-the-art frequency doublers. According to Table 1, the presented amplifier–doubler chain provided the highest peak output power of the reported frequency doublers when fabricated in CMOS technology. A frequency doubler fabricated in SiGe technology obtained a larger peak output power than the presented frequency doubler; however, the chip area of a frequency doubler fabricated in SiGe technology was 2.5 times that of the presented frequency doubler, and the DC power consumption of the frequency doubler fabricated in SiGe technology was more than three times as high as that the presented in the frequency doubler.

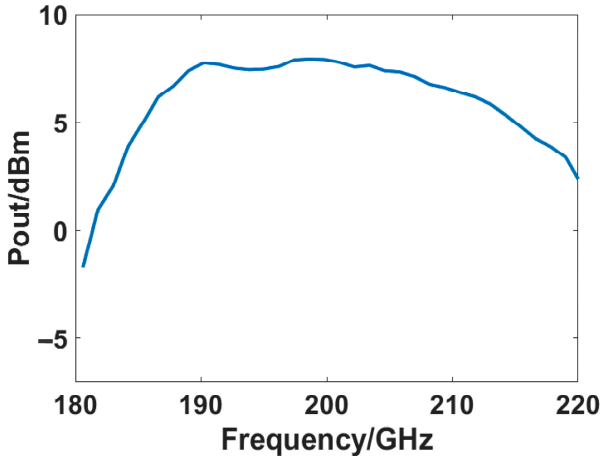


Figure 11. Measurement results of presented amplifier–doubler chain.

Table 1. Comparison with other reported designs in the literature.

	Tech.	f_{max}	Freq [GHz]	Last Multiplier Topology	Multi. Factor	DC-RF [%]	Peak Pout [dBm]	Size [mm^2]	DC [mW]
[35]	90 nm SiGe	350	200–230	DA + Mult.	2	0.23	8	3.63	2700
[36]	130 nm SiGe	500	200–255	DA + Mult. + PA	8	1.60	12 *	2.15	990
[37]	130 nm SiGe	250	165–230	DA + Mult.	2	0.87	5.2	NA	380
[29]	65 nm CMOS	NA	160–310	DA + Mult.	2	2.85	3	0.71	70
[30]	40 nm CMOS	290	213–233	DA + Mult. + PA	9	1.39	4.1	1.7	185
[38]	65 nm CMOS	NA	237–263	Mult.	2	2.87	0.9	0.071	37
This work	40 nm CMOS	290	185–215	DA + Mult.	2	2.0	7.9	0.78	307

* 12 dBm w/o de-embedding the output balun and pad.

4. Conclusions

In this paper, an amplifier–doubler chain is presented. The presented amplifier–doubler chain consists of a rat-race balun, a sixth-stage DA, and a frequency doubler. The frequency doubler was designed with a single-row staggered distribution structure, which effectively reduced the parasitic component. According to the measurements, the presented amplifier–doubler chain provided a peak output power of 7.9 dBm at 200 GHz and a 3-dB bandwidth of 30 GHz. The DC-RF efficiency was 1.87%.

In summary, the presented amplifier–doubler chain provided the highest output power in CMOS technology at 200 GHz. The presented amplifier–doubler chain could be applied to such fields as THz imaging, radar, sensing, biomedicine, and ultra-fast communications.

Author Contributions: Conceptualization, R.D.; methodology, R.D.; software, R.D. and C.Y.; validation, R.D. and C.Y.; formal analysis, R.D. and C.Y.; investigation, R.D. and C.Y.; resources, R.D.; data curation, R.D. and C.Y.; writing—original draft preparation, C.Y.; writing—review and editing, R.D. and C.Y.; visualization, R.D. and C.Y.; supervision, R.D.; project administration, R.D.; funding acquisition, R.D. All authors have read and agreed to the published version of the manuscript.

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