Article

# A Dual-Mode Step-Down Converter with Automatic Mode Switch Circuit for System-on-Chip Applications 

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#### Abstract

In this paper, a dual-mode step-down DC-DC converter with an automatic mode-switching circuit is implemented in a 28 nm digital CMOS process and embedded in an RF transceiver chip to power the digital part. The proposed automatic mode-switching circuit includes a frequency-voltage conversion circuit that is designed according to the principle of charge redistribution on capacitance. The converter can switch modes according to the load without external intervention. This converter, along with a PMU sequencer, can also provide a solution for low-power design for system-on-chip applications. The IC occupies a total die area of $0.378 \mathrm{~mm}^{2}$. The input voltage of the converter is 3.3 V , the output voltage is 1.05 V , and the maximum load current can reach 1 A . The converter shows a conversion efficiency of not less than $81 \%$ at a full load range and can achieve a peak conversion efficiency of $91 \%$ when the load current is 100 mA . The load range of the PWM mode is 1 A to 50 mA , and that of the PFM mode is 100 mA to 1 mA . The combination of zero-crossing detection circuitry and freewheel switches can reduce energy loss and eliminate additional electromagnetic interference.


Keywords: DC-DC; dual-mode control; mode automatic switch; FVC; ZCD; freewheel

## 1. Introduction

As one of the most important members of the integrated circuit industry, power management chips have been widely used in the communication, aerospace, and consumer electronics industries. Power technology is helping the information services industry to grow rapidly. On the other hand, the development of information technology creates higher requirements for power supply technology so as to promote the development of the power supply technology.

Conversion efficiency is an extremely important metric for all types of power systems. In switching power supply design, the power loss mainly comes from switching impedance, parasitic impedance of the energy storage element, non-ideal characteristics of devices, and the static current of the converter control circuit. More importantly, conversion efficiency is different under different working conditions, and the leading influencing factors are also different. There are many ways to improve conversion efficiency, but the focus is on two aspects. One is the loss of the power level, which occurs during an increase in the size of the switch transistor and in the optimization process to reduce on-off resistance of the power transistor. In addition, soft-switching technology is used to reduce the losses during on-and-off switching [1]. Another way is to use synchronous rectification technology to reduce power consumption, that is, to use MOSFETs with a smaller on-voltage drop instead of diodes, but there is a need to design a dead-time control circuit.

Another method is to switch different working modes [2-4] according to the different load situation. Because of advanced manufacturing processes, today's portable electronic devices and microprocessors require a very low operating voltage, about $0.9-1.5 \mathrm{~V}$, characterized by large load current changes, many working modes, and a long time in low-power
mode or sleep mode, so that the DC-DC converter is under light load conditions for a long period of time. In this case, the control system of the converter can switch to a light load control mode, such as Pulse Skip Modulation (PSM) mode, Pulse Frequency Modulation (PFM) mode, and Burst mode. At present, the low-static current products in industrial mass production can reach tens of nanoamperes. Another important loss is the loss on the switch during dead time. This loss may be insignificant under heavy loads, but it becomes a major factor affecting conversion efficiency under light loads.

In order to cope with different operating states and system-on-chip (SOC) modes, such as low power mode, sleep mode, full load mode, and light load mode, the control mode of the converter must also be adjusted to meet the needs of achieving higher conversion efficiency in a wider load range. Hybrid control is an important method to improve the efficiency of a DC-DC converter under full working conditions, and switching the power supply has become a research hotspot. Hong-Wei Huang proposed a DC-DC converter that can work in three modes [5]: pulse width modulation (PWM) mode for heavy loads and PFM mode for light loads. In between, the author introduced a new control mode, Dither Jump Modulation (DSM). Wan-Rone proposed a two-mode Buck converter that can adaptively switch between PWM and PFM with very high conversion efficiency [6]. Dynamic power management technology under light loads is proposed by [7]. It makes some modules of the chip enter into a sleep state, and the quiescent current of the whole chip is reduced to $45 \mu \mathrm{~A}$.

There are many ways to switch modes with different load conditions. A traditional way is sensing the slew rate of switch-node voltage during the dead time, thus indirectly sensing the inductor current, or by sensing the voltage drop Vs across the continuation transistor during its ON-time, which is proportional to the inductor current level [8]. In this paper, a new automatic mode-switching circuit is proposed for PWM and a constant on-time (COT) dual-mode control DC-DC converter. This provides a solution for mode switching between PWM and PFM. Section 2 describes the architecture of choice for this work, and Section 3 describes the details of the automatic mode-switching circuit. Simulation results are presented in Section 4.

## 2. Architecture of Buck DC-DC Converter with Dual-Mode Control

The converter designed in this paper is mostly used in SOC, and it mainly supplies power to the digital module. The design goals in this paper are to achieve a high efficiency at a full load and high integration, which means a smaller size for the peripheral passive devices. For the SOC system, considering the EMI problem caused by the switching power supply, the best control method is to adopt a fixed frequency, so that the frequency range of the switching power supply is narrow enough. As such, the subsequent active filter can further filter the switching frequency. In addition, the digital component of the SOC is in sleep mode for a long time, so it is necessary to consider how to achieve high efficiency in both heavy and light load states. Based on the above points, the Buck converter designed in this paper is finally designed to use PWM and PFM dual-mode control. The constant on time (COT) used in this paper is one of the most typical PFM control modes.

The structure of the PWM/COT dual-mode automatic switching Buck converter is shown in Figure 1. The high side and low side switches are $\mathrm{M}_{\mathrm{P}}$ (PMOS) and $\mathrm{M}_{\mathrm{N}}$ (NMOS). $\mathrm{M}_{\mathrm{N}}$ is also called the synchronous rectifying switch. Inductance L , capacitance C , and load resistor $\mathrm{R}_{\mathrm{L}}$ comprise the power stage. ESR is the equivalent series resistance of the capacitor. VIN is the input voltage supply, and $R_{1}, R_{2}$ are feedback resistors. The dead-time and driver are the dead time control module and the drive module, respectively. The dual-mode controller contains two modes of control circuit, namely, a PWM control circuit and a COT control circuit. These generate PWM duty signals and COT duty signals, respectively. The mode signal controls the switching between the PWM and COT modes. The mode automatic-switching controller consists of a zero-crossing detection circuit (ZCD), a counter, a logic control circuit, and a voltage-frequency conversion circuit (FVC).


Figure 1. Dual-mode Buck converter architecture.

## 3. Circuit Implementation of Automatic Mode Switching

### 3.1. Frequency-Voltage Conversion Circuit

The principle of the circuit is derived from the structure introduced in Djemouai's research, which was first published in 1998 [9]. He proposed a high-performance integrated CMOS frequency-voltage converter in this paper and used it in a frequency-locked loop in 2001 [10]. The circuit works on the principle of charge redistribution on a capacitor and has a small area, which can be easily integrated into other circuit modules. The formula for frequency-voltage conversion in reference [9] is as follows:

$$
\begin{equation*}
\mathrm{V}_{\text {out }}=\frac{\mathrm{I}_{\mathrm{C}} \mathrm{~T}_{1}}{\mathrm{C}}\left(\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\cdots+\frac{1}{2^{\mathrm{N}}}\right)=\frac{\mathrm{I}_{\mathrm{C}} \mathrm{~T}_{1}}{\mathrm{C}}\left(1-\frac{1}{2^{\mathrm{N}}}\right)=\frac{\mathrm{I}_{\mathrm{C}}}{\mathrm{C} \cdot 2 \cdot \mathrm{f}_{\mathrm{in}}}\left(1-\frac{1}{2^{\mathrm{N}}}\right), \tag{1}
\end{equation*}
$$

The circuit structure proposed by Djemouai is slightly improved in this paper, and frequency-voltage conversion is successfully realized. It is applied in the switching control process of PWM and COT mode. The structure in Figure 2 is the circuit structure proposed in this paper, which also uses charge balance redistribution between $C 1$ and $C 2$, but here, C 1 is used to divide half of the charge on C 2 in each cycle, and $\mathrm{C} 1=\mathrm{C} 2=\mathrm{C}$. The following specific mode-switching process illustrates the application principle of the FVC circuit. Figure 3 is a structural diagram of the automatic mode-switching circuit, which consists of two parts. One is the frequency and voltage conversion circuit FVC, and the other is a logic control circuit. The signals between the Buck circuit and the logic control circuit is also marked in Figure 3.


Figure 2. Frequency-voltage converter.


Figure 3. Schematic diagram of automatic mode switching.
The working principle of the automatic mode-switching circuit of the PWM/COT dual-mode control Buck DC-DC converter is as follows. Firstly, the conditions for triggering zero crossing in PWM mode are described by inequality (2):

$$
\begin{equation*}
\frac{2 \mathrm{~L}}{\mathrm{R}_{\mathrm{L}} \mathrm{~T}_{\mathrm{s} 1}}<\left(1-\frac{\mathrm{V}_{\mathrm{o}}}{\mathrm{~V}_{\mathrm{IN}}}\right) \tag{2}
\end{equation*}
$$

The conditions for triggering zero crossing in COT mode are described by inequality (3):

$$
\begin{equation*}
\frac{2 \mathrm{~L}}{\mathrm{R}_{\mathrm{L}} \mathrm{~T}_{\mathrm{s} 2}}<\left(1-\frac{\mathrm{V}_{\mathrm{o}}}{\mathrm{~V}_{\mathrm{IN}}}\right) \tag{3}
\end{equation*}
$$

where $R_{L}$ is the load resistor, and Vo is the output voltage of this converter. $V_{\text {IN }}$ is the input voltage of this converter, and $L$ is the inductor. $T_{s 1}$ is the switching period in PWM mode and is a fixed value. $\mathrm{T}_{\mathrm{s} 2}$ is the switching period of continuous current mode (CCM) in COT mode, which varies with the input and output voltages. The formula is as follows:

$$
\begin{equation*}
\mathrm{T}_{\mathrm{s} 2}=\frac{\mathrm{V}_{\mathrm{IN}}}{\mathrm{~V}_{\mathrm{o}}} \mathrm{~T}_{\mathrm{ON}} \tag{4}
\end{equation*}
$$

Here, $\mathrm{T}_{\mathrm{ON}}$ is the constant on time, which is fixed in the traditional COT mode. When the output load $\mathrm{R}_{\mathrm{L}}$ is large enough, so that the Buck converter triggers zero crossing and operates in discontinuous current mode (DCM), regardless of PWM or COT mode. At this time, there will be a continuous zero-crossing signal ZCD in the logic control circuit, and the counter is started. When the counter has counted 24 switching cycles $\left(\mathrm{T}_{\mathrm{s} 1}\right)$, the counter output signal (high logic level) is sent to MUX2. At this time, MODE = 1, and the Buck converter switches to COT mode and immediately starts the frequency-voltage conversion circuit. The reference current source I is under the control of switching signal HS with the double selector MUX1 to periodically charge and discharge while redistributing the charge and discharge capacitor C 1 and C 2 . The period is $\mathrm{T}_{\mathrm{s} 2 \_\mathrm{d}}$ when the Buck circuit works in the COT mode of DCM:

$$
\begin{equation*}
\mathrm{T}_{\mathrm{s} 2 \_\mathrm{d}}=\frac{\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{o}}}{\mathrm{~L}} \frac{\mathrm{~V}_{\mathrm{IN}}}{\mathrm{~V}_{\mathrm{o}}} \frac{\mathrm{~T}_{\mathrm{ON}}^{2}}{2 \mathrm{I}_{\mathrm{o}}} \tag{5}
\end{equation*}
$$

The signal on capacitor C 2 obtains a DC value after passing through the RC filter circuit. According to Figure 4, the charging time of the first stage is $t_{1}$, and the starting voltage of C 2 is $\mathrm{V}_{1}$. The charging time of the second stage is $\mathrm{t}_{2}$, and the voltage at the end of $t_{2}$ is $V_{2}$. The upper electrode plates of the two capacitors C 1 and C 2 are connected again at the end of $t_{2}$, and the charge is redistributed almost instantly. The voltage is reduced from $V_{2}$ to $V_{1}$, and then the previous charging process is repeated. $C 1$ is equal to $C 2$ is equal to $C$, so $V 1$ is equal to $1 / 2 V_{2}$, which means that from $V_{1}$ to $V_{2}$, the voltage changes by $1 / 2 \mathrm{~V}_{2}$. The voltage changes in this process:

$$
\begin{equation*}
\Delta \mathrm{V}=\frac{\mathrm{I} \cdot \mathrm{t}_{1}}{2 \mathrm{C}}+\frac{\mathrm{I} \cdot \mathrm{t}_{2}}{\mathrm{C}}=\frac{1}{2} \cdot \mathrm{~V}_{2}=\mathrm{V}_{1} \tag{6}
\end{equation*}
$$



Figure 4. Waveform of the frequency-voltage conversion circuit.
Here, $\mathrm{t}_{1}+\mathrm{t}_{2}=\mathrm{T}_{\mathrm{s} 2 \text { _d }}, \mathrm{t}_{2}=\mathrm{T}_{\text {on }}$.
Since the DC value of a signal is the average of the signal, taking the average of the signal over a period delivers the DC value:

$$
\begin{equation*}
V_{c}=\frac{1}{t_{1}+t_{2}} \int_{t_{1}}^{t_{1}+t_{2}} V(t) d t \tag{7}
\end{equation*}
$$

After calculation, the expression formula of the DC value of $\mathrm{V}_{\mathrm{C}}$ can be obtained:

$$
\begin{equation*}
\mathrm{V}_{\mathrm{C}}=\frac{\mathrm{I}}{4 \mathrm{C}}\left[\frac{\mathrm{~T}_{\mathrm{s} 2 \_\mathrm{d}}^{2}+\mathrm{T}_{\mathrm{ON}}^{2}}{\mathrm{~T}_{\mathrm{s} 2 \_\mathrm{d}}}+2\left(\mathrm{~T}_{\mathrm{s} 2 \_\mathrm{d}}+\mathrm{T}_{\mathrm{ON}}\right)\right] \tag{8}
\end{equation*}
$$

Under a light load, $\mathrm{T}_{\mathrm{ON}} \ll \mathrm{T}_{\mathrm{S} 2 \text { _d }}$, and combined with Formula (5), we can obtain:

$$
\begin{equation*}
\mathrm{V}_{\mathrm{C}} \approx \frac{3 \mathrm{I}_{\mathrm{s} 2 \_\mathrm{d}}}{4 \mathrm{C}}=\frac{\mathrm{K}}{\mathrm{I}_{\mathrm{o}}} \tag{9}
\end{equation*}
$$

The parameter K is:

$$
\begin{equation*}
K=\frac{3 I\left(V_{I N}-V_{O}\right) V_{I N} T_{O N}^{2}}{8 C V_{O} L} \tag{10}
\end{equation*}
$$

This DC voltage of $\mathrm{V}_{\mathrm{C}}$ is fed into a comparator and compared with the reference voltage Vref to obtain the mode-switching signal VF. According to the above two Formulas (9) and (10), the switching period $\mathrm{T}_{\mathrm{s} 2 \_\mathrm{d}}$ is inversely proportional to the load current Io when the output voltage $\mathrm{V}_{\mathrm{O}}$ and input voltage $\mathrm{V}_{\text {in }}$ are constant. In addition, the conversion of $\mathrm{V}_{\mathrm{C}}$ and the switching period $\mathrm{T}_{\mathrm{s} 2 \text { _d }}$ are in an approximately linear proportional relationship. Thus, an inverse relationship between the conversion voltage $\mathrm{V}_{\mathrm{C}}$ and the load current Io can be established. Even if the relationship is not linear, it can be used to make a judgment for mode switching as long as it has monotonicity.

### 3.2. Mode-Switching Control Circuit

The obtained conversion signal VF is fed into the control logic circuit, as shown in Figure 5, then sampled into the flip-flop DFF3 at the rising edge of the switching clock. Its output is fed into MUX2 after passing through an inverter. MUX2 chooses channel 0, and $\mathrm{V}_{\mathrm{C}}$ is sent to flip-flop DFF2 at the rising edge of the switch clock, thus obtaining the final mode signal MODE. If $\mathrm{VF}=0, \mathrm{MODE}=1$, and the Buck is locked in COT mode; if $\mathrm{VF}=1$, MODE $=0$, and BUCK switches back to PWM mode and continues to monitor the zerocrossing signal. Therefore, it can be seen that in order to avoid the phenomenon of periodic switching between the two modes, it is necessary to carefully calculate the value of the setting reference voltage Vref according to the conditions of triggering zero-crossing detection.


Figure 5. Control and logic circuit.
The MODE signal is fed into the Buck circuit and connected to the selection control S of a MUX dual selector, which selects the duty ratio signal. When MODE $=1$, select the duty ratio signal generated by COT mode; when $\mathrm{MODE}=0$, select the duty ratio signal
generated by PWM mode, so as to complete the automatic switching of the control mode. The above process is summarized in a flow chart shown in Figure 6.


Figure 6. Flow chart of automatic mode switching.

### 3.3. Zero-Crossing Detector with Freewheel Switch

As described in Section 3.1, if the Buck works under a light load, and the amplitude of the inductor current ripple is greater than the load current, the inductor current will reverse flow into the low side switch $\mathrm{M}_{\mathrm{N}}$ and result in a current back-flow phenomenon with a large power loss. In order to prevent the above phenomenon of current inversion in the DC-DC converter and to make the converter work in DCM mode under a light load, a detection and control circuit is needed. This circuit closes the low side switch $\mathrm{M}_{\mathrm{N}}$ before the direction of the inductor current is changed. This is the purpose of designing a zero-crossing detection circuit.

The voltage at the switching node SW is negative when $\mathrm{M}_{\mathrm{N}}$ is open. As the inductor current decreases with a certain slope, the voltage at the SW point gradually increases, but it is usually less than zero. If the voltage at the SW point is greater than zero while $\mathrm{M}_{\mathrm{N}}$ remains open, this means that current backflow occurs. Therefore, it is necessary to detect when the voltage at the SW point passes through zero and to close $\mathrm{M}_{\mathrm{N}}$ at the appropriate time.

There are two design ideas for the zero-crossing detection circuit. One is to connect a resistor [11] in a series on the branch of the synchronous rectifying switch $\mathrm{M}_{\mathrm{N}}$ and determine whether the current backflow occurs by detecting the voltage at both ends of the resistor. However, this method will cause additional losses and reduce the conversion efficiency of the converter. The second method is to use the sampling circuit to copy the current on the synchronous rectifying switch, convert it into voltage, and then use the operational amplifier for processing [12,13]. This method has higher requirements on the operational amplifier and occupies a large chip area, which increases the complexity of the circuit.

Therefore, a simple zero-crossing detection circuit is designed in this paper that adopts the common gate current comparator structure and uses the substrate replacement circuit to improve the sensitivity of the zero-crossing detection circuit and speed up the turn-off process of the power switch. The structure of the circuit is shown in Figure 7.


Figure 7. Zero-crossing detection circuit diagram.
The resistor $R_{2}$ is used to sample the current flowing through $S W$. When $M_{N}$ is open and SW voltage is negative, then it increases gradually. When SW is small enough, $\mathrm{V}_{\mathrm{GS} 4}>\mathrm{V}_{\mathrm{GS} 3}$, and since $\mathrm{I}_{1}=\mathrm{I}_{2}$ always holds, and $\mathrm{M}_{\mathrm{N} 3}$ works in a saturated region, $\mathrm{M}_{\mathrm{N} 4}$ must enter a linear region, so that VDS is very small and almost equals to 0 at this time. Therefore, the value of $V_{Z C D}$ is also very small. This will not exceed the threshold voltage of the back-stage inverter and will not trigger the zero-crossing detection signal ZCD. When SW gradually increases, $\mathrm{V}_{\mathrm{GS} 4}$ gradually decreases, and $\mathrm{M}_{\mathrm{N} 4}$ also enters the saturated region. The width-length ratio of $\mathrm{M}_{\mathrm{N} 3}$ and $\mathrm{M}_{\mathrm{N} 4}$ is the same, that is, the process coefficient $\mathrm{k}_{3}=\mathrm{k}_{4}$. In addition, the substrate replacement circuit is not considered at this time, and the threshold voltage of the two transistors are assumed to be the same, $V_{\text {th } 3}=V_{\text {th } 4}$.

$$
\begin{align*}
& I_{1}=\frac{1}{2} k_{4}\left(V_{G S 4}-V_{t h 4}\right)^{2}=I_{2}=\frac{1}{2} k_{3}\left(V_{G S 3}-V_{t h 3}\right)^{2}=I  \tag{11}\\
& V_{G S 4}=V_{G}-S W-I \cdot R_{2}=V_{G S 3}=V_{G}-I \cdot R_{1}
\end{align*}
$$

The above equation shows that the condition for zero-crossing detection to be triggered is:

$$
\begin{equation*}
S W=I\left(R_{1}-R_{2}\right) \tag{12}
\end{equation*}
$$

Setting $R_{1}$ and $R_{2}$ can adjust the zero-crossing trigger point of SW. Generally, considering the inevitable delay from triggering the zero-crossing detection signal ZCD to actually turning off $\mathrm{M}_{\mathrm{N}}, R_{1}-R_{2}<0$ is deliberately set, so that the zero-crossing signal can be triggered slightly in advance, and $\mathrm{M}_{\mathrm{N}}$ can be turned off in time. Now, consider the substrate displacement circuit. It is obvious that both $\mathrm{M}_{\mathrm{N} 3}$ and $\mathrm{M}_{\mathrm{N} 4}$ are substrate-biased, and the threshold voltage of both cannot be the same. The purpose of the substrate replacement circuit is to set the substrate potential of $M_{N 3}$ and $M_{N 4}$ to the value of SW when the low side switch is conducted. The above formula is rewritten:

$$
\begin{align*}
& I_{1}=\frac{1}{2} k_{4}\left(V_{G S 4}-V_{t h 4}\right)^{2}=I_{2}=\frac{1}{2} k_{3}\left(V_{G S 3}-V_{t h 3}\right)^{2}=I \\
& V_{G S 4}-V_{t h 4}=V_{G}-S W-I \cdot R_{2}-V_{t h 4}=V_{G S 3}-V_{t h 3}=V_{G}-I \cdot R_{1}-V_{t h 3}  \tag{13}\\
& S W=I \cdot\left(R_{1}-R_{2}\right)+\left(V_{t h 3}-V_{t h 4}\right)
\end{align*}
$$

The relationship between the threshold voltage and the substrate bias is known:

$$
\begin{equation*}
V_{t h}=V_{t h 0}+\gamma\left(\sqrt{\left|2 V_{\Phi}\right|+V_{S B}}-\sqrt{\left|2 V_{\Phi}\right|}\right) \tag{14}
\end{equation*}
$$

Formula (15) is as follows:

$$
\begin{align*}
& V_{S B 3}=I \cdot R_{1}-S W \\
& V_{S B 4}=I \cdot R_{2} \tag{15}
\end{align*}
$$

Therefore, when SW increases, $V_{S B 3}$ decreases. This results in $V_{T H 3}$ decreasing, and the current remains constant, so VG becomes smaller, thus $\mathrm{V}_{\mathrm{GS4}}$ becomes smaller, $\mathrm{M}_{\mathrm{N} 4}$ enters the saturation area faster, and ZCD, a zero-crossing detection signal, is triggered faster. The zero-crossing detection circuit is simple and sensitive, and it does not need to occupy a large amount of chip area.

When zero-crossing detection is triggered, the relictor closes, and the energy on the inductor is not fully released. As a result, this part of the energy oscillates back and forth between the inductor and the parasitic capacitance of the relictor, and ringing occurs at the switching node, as shown in Figure 8.


1

Figure 8. Ringing phenomenon without a freewheel switch in ZCD.
The frequency of this damped oscillation is:

$$
\begin{equation*}
f_{\text {ring }}=\frac{1}{2 \pi \sqrt{L C_{N}}} \tag{16}
\end{equation*}
$$

The $C_{N}$ here is the parasitic capacitance of $\mathrm{M}_{\mathrm{N}}$. Although such oscillation will stabilize at the output voltage Vo, it will have an extra EMI effect on the system noise and bring interference to other analog modules in a system on chip, or it may even affect their normal operation. Therefore, it needs to be eliminated. Since the energy of the inductor is not released completely, we can find a way to let this part of the energy flow back to the output end, so as to avoid the ringing phenomenon without energy loss [14]. A schematic diagram of the circuit structure with the freewheel switch is shown in Figure 9.

The simulation results are shown in Figure 10. It can be seen that the ringing phenomenon disappears. The flip point of zero-crossing detection is -755 uV , and the inductor current is -76 uA . The zero-crossing detection circuit works normally, and the results meet the design expectations.


Figure 9. Zero-crossing detection circuit diagram with freewheel switch.


Figure 10. Simulation results after eliminating the ringing phenomenon with freewheel switch.

## 4. Simulation Results

The simulation results of the frequency and voltage conversion circuit are shown in Figure 11. Depending on the different frequency of HS, from 285 kHz to 2 MHz , the FVC circuit will generate different voltage values. From this, we establish a relationship between the frequency and voltage, and the frequency is related to the load current. Finally, the relationship between the load current and the voltage can be obtained. Based on this correspondence, the mode-switching circuit can automatically complete the modeswitching process according to the load current, as shown in Figure 12. The transfer point can also be adjusted by setting the reference voltage of the comparator in the FVC circuit. Vref is set to 0.6 V .


Figure 11. Simulation of frequency-voltage conversion circuit.


Figure 12. Mode-switching result.
A simulation of the automatic mode-switching process of the converter in normal operation according to the load conditions is shown in Figure 13. The load current is dynamically switched from 300 mA to 50 mA and then back to 300 mA . The mode signal shows a low level in PWM mode. When the load current is reduced to 50 mA , after a certain period of time, the converter automatically switches to COT mode. At this time, the mode signal is high, and the switching frequency of the converter working in COT mode has obviously changed. After that, the load jumps to 300 mA . At this time, the converter is still working in COT Mode. However, after a certain amount of time, the converter switches to PWM mode. It is shown that the mode signal is on a low level, and the switching frequency of the converter also becomes higher. According to the simulation results, the converter conforms to the design scheme described in Section 3.2.


Figure 13. Waveform of automatic mode switching.
The converter is simulated under the max load current in PWM mode, as shown in Figure 14. The input decoupling capacitance is 4.7 uF , and the output capacitance is 10 uF . The inductor is 2.2 uH , and here, we assume $\mathrm{ESR}=100 \mathrm{~m} \Omega$ and $\mathrm{DCR}=60 \mathrm{~m} \Omega$. The input voltage is 3.3 V . The output port is mounted with $1.05 \Omega$. As shown in Figure 14, the converter works stably at $\mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}$, and the average output voltage is 1.048 V . The voltage ripple is 17.3 mV , the inductor current ripple is 171.8 mA , and the switching period is 490 ns .


Figure 14. Steady-state simulation result in PWM mode at $\mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}$.
The converter is in COT mode, which is under the condition of a light load, as shown in Figure 15. The simulation conditions are as in the previous section, and the control system automatically switches to the COT mode when the converter is working under a light load. The resistance mounted on the output becomes $35 \Omega$. As can be seen is Figure 15, when the converter works stably, it works in DCM mode. The output voltage is 1.05 V , and the voltage ripple is 30 mV , which is larger than the voltage ripple in PWM mode. The constant on time is 434 ns . In addition, the switching period is about 9 us, which is much
larger than the PWM's switching cycle. The switching loss can be reduced by lowering the frequency, but the cost of this is that the ripple of the output voltage becomes larger, and the band of the switching frequency becomes wider.


Figure 15. Steady-state simulation result in COT mode at $\mathrm{I}_{\mathrm{O}}=30 \mathrm{~mA}$.
The converter designed in this paper uses 28 nm CMOS process to complete the layout. The chip area is $0.378 \mathrm{~mm}^{2}$, as shown in Figure 16. The simulation verification work is based on the Cadence platform and the Spectre tool. The results show that the chip can start normally at a full load and at no load, the starting process is smooth, the working state is stable after starting, and the automatic mode-switching process is smooth. The simulation results show that the input voltage of the converter is 3.3 V , and the output voltage is 1.05 V . The maximum load current can reach 1 A , and conversion efficiency can reach $81 \%$ at a full load, as shown in Figure 17. The peak conversion efficiency is $91 \%$ at 100 mA . The specifications of the converter are shown in Table 1.


Figure 16. The layout picture.


Figure 17. The conversion efficiency of the converter in all load ranges.
Table 1. Specifications of Buck converter.

|  | Basic Information |
| :---: | :---: |
| Technology | 28 nm process |
| Input voltage | 3.3 V |
| Output voltage | 1.05 V |
| Output current range | $1 \mathrm{~mA}-1 \mathrm{~A}$ |
| Peak efficiency | $91 \%$ |
| Pulse-Width Modulation Mode |  |
| Load region | $1 \mathrm{~A}-50 \mathrm{~mA}$ |
| Switching frequency | 2 MHz |
| Output ripple voltage | $<20 \mathrm{mV}$ |
| Full load efficiency | $81 \%$ |
| Constant On-Time Modulation Mode |  |
| Load region | $100 \sim 1 \mathrm{~mA}$ |
| Constant on time | 400 ns |
| Output ripple voltage | $<40 \mathrm{mV}$ |

## 5. Conclusions

In this paper, a frequency-voltage conversion circuit is designed according to the principle of charge redistribution on the capacitor, and it is successfully applied to the automatic mode switching circuit of a PWM/COT dual-mode control converter. In addition, the traditional zero-crossing detection circuit is improved by adding a substrate replacement circuit and matching a freewheel switch to ensure that the converter can turn off the low side switch accurately and quickly when working in DCM mode without wasting power consumption. With the use of a freewheel switch, additional electromagnetic interference is eliminated, and the efficiency of the converter is further improved. An automatic mode-switching circuit and a zero-crossing detection circuit were applied in the Buck converter designed in this paper. The simulation results show that the converter can perform automatic mode switching accurately and smoothly according to the load condition without the need for digital control or other external intervention. Furthermore, the conversion efficiency of the converter in light load conditions is improved, and an effective solution is proposed for the power supply of SOC.


#### Abstract

Author Contributions: Y.L. designed the circuit structures, carried out the simulations, analyzed the data, and wrote the paper. T.M. provided critical feedback and improved the final design. B.W. provided modification methods and suggestions. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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