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A 1.8 V Low-Power Low-Noise High Tunable Gain TIA for CMOS Integrated Optoelectronic Biomedical Applications

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Abstract: This paper reports on a novel solution for a transimpedance amplifier (TIA) specifically designed as an analog conditioning circuit for low-voltage, low-power, wearable, portable and implantable optoelectronic integrated sensor systems in biomedical applications. The growing use of sensors in all fields of industry, biomedicine, agriculture, environment analysis, workplace security and safety, needs the development of small sensors with a reduced number of electronic components to be easily integrated in the standard CMOS technology. Especially in biomedicine applications, reduced size sensor systems with small power consumption are of paramount importance to make them non-invasive, comfortable tools for patients to be continuously monitored even with personalized therapeutics and/or that can find autonomous level of life using prosthetics. The proposed new TIA architecture has been designed at transistor level in TSMC 0.18 μm standard CMOS technology with the aim to operate with nanoampere input pulsed currents that can be generated, for example, by Si photodiodes in optical sensor systems. The designed solution operates at 1.8 V single supply voltage with a maximum power consumption of about 36.1 μW and provides a high variable gain up to about 124 dBΩ (with fine- and coarse-tuning capabilities) showing wide bandwidth up to about 1.15 MHz and low-noise characteristics with a minimum noise floor level down to about 0.39 pA/$\sqrt{\text{Hz}}$. The overall circuit is described in detail, and its main characteristics and performances have been analyzed by performing accurate post-layout simulations.

Keywords: low-voltage; low-power; low-noise; tunable gain; CMOS Integrated Technology; optoelectronics; transimpedance amplifier (TIA); biomedical applications

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1. Introduction

The development of specific wearable, portable, and implantable sensor devices are the key elements for the most demanding applications in biomedicine that aim to implement novel reliable means for personalized telemedical diagnostic and therapeutic [1–4]. Even if today sensors find large applications in many other industrial areas (i.e., from automotive and robotics to environment analysis and agriculture) for their capability to probe many physical and chemical properties (like temperature, humidity, chemical reactions, distances, surface rugosity, etc.), those ones related to biomedicine involve the special requirements to acquire, elaborate, transmit and receive data by using very low electrical power. Biomedical sensors, in fact, must be dressed from or implanted in persons (many times elderly patients) who are often suffering important diseases. For this, the sensor on board front-end electronic architectures must be designed to operate under low-voltage,

low-power conditions with a reduced number of active and passive components and with the possibility to be implemented at transistor level in the standard CMOS technology.

In general, medical sensors for clinical recordings make use of conductive gel wet electrodes or dry electrodes to be worn continuously, even for long-term periods [5]. In particular, dry electrodes have the advantages to permit longer measurements and shorter preparation times, resulting as more comfortable for the patient. Among the dry electrodes, otprodes [6] are finding applications as optical sensors in photoplethysmography (PPG) [7,8], transcutaneous blood gas monitoring [9,10], and neural interfaces [6,11]. Additionally, in other fields strictly connected to medical applications, single sensors or array of sensors play a crucial role. This is the case of wearable robot and exoskeletons for prosthetics [12,13] where different kinds of sensors allow the patient to find a comfortable and autonomous level of life. Another important application of wearable gas and particle sensors is the monitoring of environment to guarantee health and safety of persons in workplaces where hazardous gases or nano–micro-sized pollutants are employed [14–16].

From the above-mentioned applications, it is evident that the electronic front-end of the sensors must be designed to comply with demanding characteristics for what concerns the minimum detectable current/voltage signal that is directly related, for example, to the determination of the lowest concentration of chemical/biochemical substances to be detected and/or to the smallest displacement to be actuated in wearable prosthetics. Independently from the specific application, the front-end of sensor devices is generally based on specific transimpedance amplifiers (TIA) as the first conditioning circuits that, for all the applications outlined before, need to operate under low-voltage and low-power conditions [17–30].

With this aim, this paper presents a novel TIA architecture that has been specifically designed at transistor level in TSMC 0.18 μm standard CMOS technology to manage nanoampere input pulsed currents generated by Si photodiodes (PDs) that, together with semiconductor lasers or LEDs, are the key elements of optical sensors. The proposed solution is capable to operate at 1.8 V single supply voltage with a maximum power consumption of about 36.1 μW and allows to achieve variable gains up to about 124 dBΩ (with fine- and coarse-tuning capabilities) with a wide bandwidth up to about 1.15 MHz and low-noise characteristics, thus resulting as particularly suitable for integrated optoelectronic sensing systems in biomedical applications. Moreover, the complete theoretical analysis of the proposed circuit discussed in the paper opens the possibility to employ the same circuit architecture by a suitable sizing of the passive and active components, also for other kinds of input signals coming from wireless sources, such as RF antennas operating at wider bandwidths [31–34].

2. Circuit Design and Theory

The overall block scheme illustrating the main stages of the proposed electronic circuit is shown in Figure 1. The photocurrent I_{PD} generated by a PD is the input signal of the TUNABLE CURRENT PRE-AMPLIFIER stage, based on a current mirror architecture, capable to amplify the incoming current signal with a specific gain settable through the external voltages V_1, V_2 and V_3 that are the digital control signals for the electronic circuit coarse gain tuning. An additional external analog control voltage signal V_{AN} is also included to perform fine-tuning of the current gain so providing the amplified output current I_{OUT}. This is the input signal of the subsequent TIA stage and the generated output voltage signal V_{OUT} is obtained by a current-to-voltage amplifier based on a modified Regulated Cascode TIA (RGC-TIA) circuit topology [17–21].

The complete schematic circuit designed at transistor level in TSMC 0.18 μm standard CMOS technology is reported in Figure 2. The circuit has been implemented, simulated, and analyzed in CADENCE Design System environment considering a 1.8 V single supply voltage. More in detail, referring to Figure 2, the first stage of the architecture is the standard electrical model emulating a Si PD that operates in photoconductive regime that is composed by the following elements: an ideal current generator providing the

photocurrent I_{IN} proportional to the light power impinging on the PD sensitive area, a junction capacitance C_J, a shunt resistance R_{SH}, and an in-series resistance R_S. In addition, the PD cathode terminal represented by the voltage node V_{BIAS} is connected directly to the overall supply voltage VDD = 1.8 V. The PD Anode provides the photocurrent I_{PD} that is the input signal for the subsequent TUNABLE CURRENT PRE-AMPLIFIER block based on a current mirror architecture composed by the transistors M1-M2-M4 and M5 (or M7, or M9) selected by the digital control signal V_1 (or V_2, or V_3, individually activated). These digital control voltages operate on transistors M6, M8, and M10, so allowing to set three different current gains to be selected as a function of the light power illuminating the PD sensitive area. Moreover, the diode-connected transistors M11 and M12 implement the active load of the current mirror architecture. In addition, the analog control signal V_{AN} acts on transistor M3 providing a more accurate and fine-tuning of the overall current gain achieved by this block. The presence of this analog control permits to continuously adjust the effective current gain needed to compensate current offsets and other circuit non-idealities (e.g., current mirror mismatches). Then, the amplified current I_{OUT} flows through the diode-connected transistor $M0_T$ of the last stage of the TIA where $M2_T$, having $M3_T$ as active load and the source connected to the same TIA input, is properly regulated by a common source voltage amplifier implemented by the $M1_T$ and $M4_T$ transistors. Finally, the stability of the system is guaranteed by the two capacitances C1 and C2 in feedback connections.

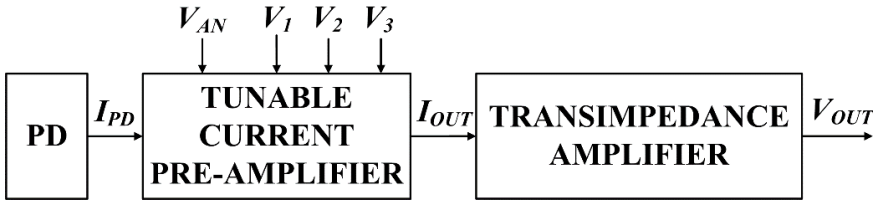

Figure 1. Overall block scheme of the proposed electronic circuit.

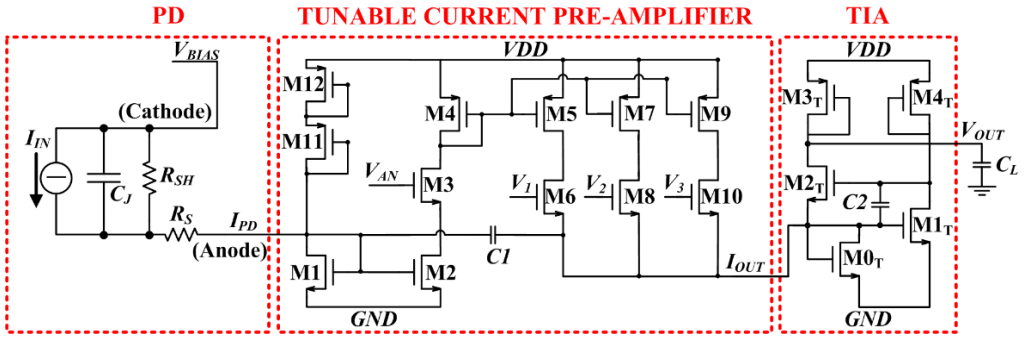

Figure 2. Schematic of the proposed electronic circuit designed at transistor level.

From the complete theoretical analysis, the transimpedance gain of the electronic circuit as function of the frequency is given by the following equation:

$$Z_{TOT}(f) = \frac{N}{g_m(M3_T)} \frac{1}{\left[1 + \frac{j2\pi f C_{IN} g_m(M4_T)}{g_m(M2_T)[g_m(M4_T)+g_m(M1_T)]}\right]\left[1 + \frac{j2\pi f C_{OUT}}{g_m(M3_T)}\right]} \quad (1)$$

where N is the current gain of the TUNABLE CURRENT PRE-AMPLIFIER block and g_m's are the transconductances of each specified transistor. Moreover, C_{IN} and C_{OUT} are the total capacitances at the circuit input and output nodes, respectively. Referring to Figure 2, they are equal to:

$$\begin{cases} C_{IN} = C1 + C2\left[1 + \frac{g_m(M1_T)}{g_m(M4_T)}\right] + C_{PAR\_IN} \\ C_{OUT} = C_L + C_{PAR\_OUT} \end{cases} \quad (2)$$

where C_{PAR_IN} is the parasitic capacitance at the input of the TIA block and C_{PAR_OUT} the parasitic capacitance at the final output node of the system combined with the load capacitance C_L.

The complete layout of the described optoelectronic circuit has been designed in standard TSMC 0.18 µm CMOS technology and is shown in Figure 3a,b, requiring a Si area of 2070 µm^2. The overall layout also includes in panel (c) an integrated PD based on a PNP junction with a Si area of 10,000 µm^2. The size of the PD sensitive area has been chosen to guarantee a small junction capacitance C_J (8 pF) and standard values of R_{SH} (100 MΩ) and R_S (50 Ω) so making this device suitable to detect light pulses in optical biosensing applications. Table 1 reports the sizes of all the employed transistor and the values of the main parameters of the CMOS designed electronic circuit.

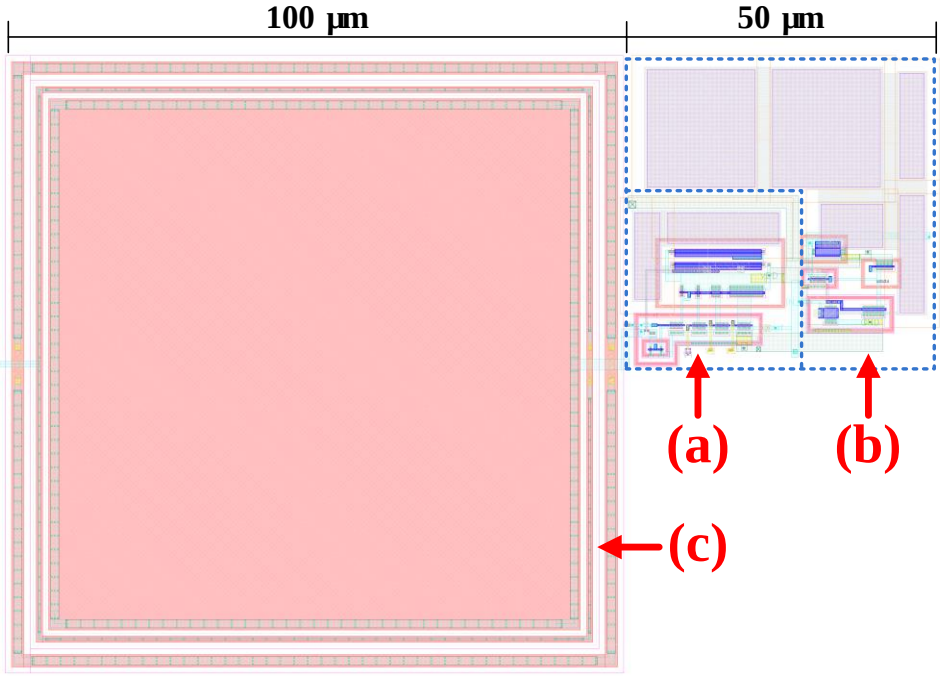

Figure 3. Layout of the CMOS optoelectronic circuit: (**a**) the TUNABLE CURRENT PRE-AMPLIFIER block; (**b**) the TIA block; and (**c**) the integrated PD based on a PNP junction.

Table 1. Transistor sizes and values of the passive components of the electronic circuit.

Transistor	**Size W/L (µm/µm)**
M1, M2, M4	0.22/0.18
M5	0.28/0.36
M3, M6, M8, M10	2.2/0.18
M7	1.4/0.36
M9	5.4/0.36
M11, M12	0.22/14
$M0_T$	2/1.6
$M1_T$	3.6/0.36
$M4_T$, $M2_T$	2.65/0.18
$M3_T$	1/4
C_L	0.7 pF
Component	**Value**
*C*1	0.3 pF
*C*2	1.8 pF
C_J	8 pF
R_{SH}	100 MΩ
R_S	50 Ω

3. Circuit Simulation Results and Discussion

The characteristics and performances of the designed circuit have been evaluated in CADENCE Design Systems environment by performing complete post-layout simulations. More in detail, the transistor sizes and the values of the passive components of the complete circuit reported in Table 1, have been properly chosen and optimized consequentially to the complete theoretical analysis of the circuit and by fully applying standard microelectronic design techniques. In this way, it has been possible to obtain the finest trade-off among all the parameters of the designed circuit with the aim to achieve its best characteristics, especially in terms of: (i) low power consumption; (ii) low noise; (iii) small silicon area; (iv) suitable bandwidth; (v) very high and tunable gain of the circuit powered at 1.8 V single supply voltage; and (vi) capability to operate with nanoampere input current pulses. In addition, the validity and correctness of Equation (1) has been also proven and confirmed through the results achieved by the performed post-layout simulations.

In particular, the small signal frequency analysis of the electronic circuit has been studied and analyzed in the range from 10^0 Hz to 10^{11} Hz under three different current gain conditions achieved by varying the external control voltages V_1, V_2, V_3 and V_{AN} of the TUNABLE CURRENT PRE-AMPLIFIER block (see the circuit block scheme of Figure 1 and the schematic of Figure 2). The resulting magnitude and phase values of the transimpedance gain, as a function of the frequency of the input signal, are reported in Figure 4. More in detail, as shown in the upper panel of Figure 4, fixing the value of the analog control voltage V_{AN} = 1.8 V, the resulting circuit bandwidth is about: (i) 555 kHz, corresponding to the maximum transimpedance gain of about 124 dBΩ obtained by setting the control voltages V_3 = 1.8 V, V_2 = V_1 = GND (the purple line); (ii) 650 kHz related to the transimpedance gain of about 113 dBΩ obtained by setting the control voltages V_2 = 1.8 V, V_3 = V_1 = GND (the red line); and (iii) 1.15 MHz associated to the minimum transimpedance gain of about 102 dBΩ obtained by setting the control voltages V_1 = 1.8 V, V_2 = V_3 = GND (the green line). Moreover, for these three values of the transimpedance gain, the inset of the upper panel of Figure 4 also shows the effects of the gain fine-tuning provided by varying the V_{AN} external control voltage. In particular, the continuous lines are the maximum transimpedance gains obtained as previously described, while the dashed and the dotted lines have been obtained by setting V_{AN} = 1.5 V and V_{AN} = 1.2 V, respectively. This fine-tuning capability allows us to control the circuit gain up to about ±2 dBΩ with respect to the maximum/nominal values reported above. Finally, referring to these simulations, the resulting circuit GBW is about 30 GHz with a corresponding phase margin for each gain value of about −78°, as indicated in the low right corner of the lower panel of Figure 4. This result demonstrates that the circuit stability is guaranteed by the presence of the feedback capacitors *C*1 and *C*2 that provide a phase response always lower than −130°.

The influence of each circuit parameter on the transimpedance gain has been also investigated and evaluated. Referring to Equation (1), the transimpedance gain mainly depends on the transconductances g_m of the transistors composing the circuit and, among them, the most significant one is the transconductance of the transistor $M3_T$ (i.e., $g_m(M3_T)$). In this regard, specific parametric post-layout simulations have been performed to demonstrate the influence of the variation of the $g_m(M3_T)$ on the resulting transimpedance gain of the circuit. Therefore, changes of $g_m(M3_T)$ have been considered by varying of ±50% the transistor width W (i.e., W_{M3T}, from which the $g_m(M3_T)$ depends on), with respect to its nominal value reported in Table 1. As shown in Figure 5, any variation (positive or negative) of W_{M3T} (and so, of the corresponding $g_m(M3_T)$) always provides a significant reduction of the overall transimpedance gain (121.7 dBΩ and 122 dBΩ, for positive and negative variations of W_{M3T}, respectively), with respect to its best value of 124 dBΩ achieved under the chosen operating conditions and circuit device sizes reported in Table 1. In the inset of Figure 5, a magnification of the transimpedance gain, in the reduced range of frequencies from 1 Hz to 1 MHz, has been also reported. Similar analyses have been also performed by changing the transconductance values of the other circuit transistors (i.e., $g_m(M1_T)$, $g_m(M2_T)$ and $g_m(M4_T)$), always considering variations of ±50% of the transistor widths W, with

respect to their nominal values reported in Table 1. In all these last cases, any positive or negative variation of the g_m values provides a maximum change of the transimpedance gain lower than ±0.5 dBΩ, with respect to its best value of 124 dBΩ achieved under the chosen operating conditions and device sizes reported in Table 1. Consequently, the dependence of the resulting transimpedance gain from these circuit transistors parameters can be considered negligible. Additionally, these results confirm the best/optimum choice of the complete circuit components and parameters as well as demonstrate the robustness, the stability, and the strong independence of the designed circuit from the technological spread and the process variations [35,36].

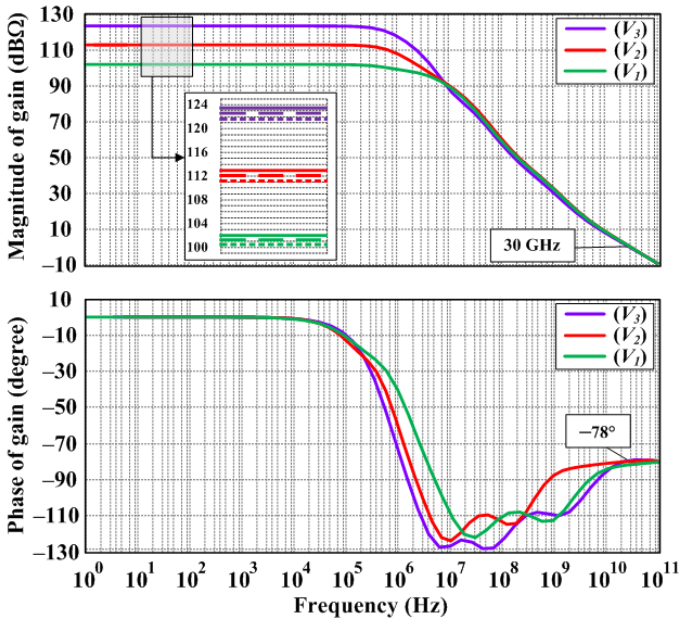

Figure 4. Upper panel: magnitude of the circuit transimpedance gain as function of the frequency for different gain settings by acting on the external control voltages V_1, V_2, and V_3. In the inset, the corresponding fine tuning achieved by varying the control voltage V_{AN}. Lower panel: the corresponding values of the phase of the circuit transimpedance gain.

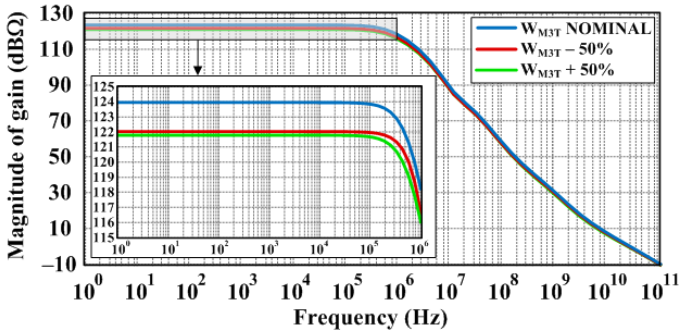

Figure 5. Magnitude of the circuit transimpedance gain as function of the frequency and by varying of ±50% the $M3_T$ transistor width W_{M3T} (from which the $gm(M3_T)$ depends on), with respect to its nominal value reported in Table 1. In the inset, the magnification in the reduced range of frequencies from 1 Hz to 1 MHz.

In Figure 6, the achieved equivalent input-referred current noise of the circuit is reported. It has been evaluated considering the same frequency range used for the simulations of Figures 4 and 5 and for the three circuit gains controlled by the voltages V_1, V_2, V_3 and fixing V_{AN} = 1.8 V. In the inset of Figure 6 is reported a magnification of the data in a reduced frequency range (i.e., from 100 kHz to 1 MHz) so demonstrating that its minimum value (i.e., the noise floor level), mainly related to the thermal noise contribution,

is about: (i) 0.39 pA/$\sqrt{\text{Hz}}$ activating the control voltage V_3; (ii) 0.53 pA/$\sqrt{\text{Hz}}$ activating the control voltage V_2; and (iii) 1.2 pA/$\sqrt{\text{Hz}}$ activating the control voltage V_1. Furthermore, the robustness of the circuit response has been studied by performing Corner Analysis simulations, also including process variations. In this sense, the analysis has been performed by considering temperature variations ranging between −25° to +75 °C and changes of the supply voltage of ±5% with respect to its nominal value (i.e., *VDD* = 1.8 V). The results of the simulations demonstrate that magnitude and phase of the transimpedance gain, as well as the equivalent input-referred current noise, have a maximum statistical uncertainty of about ±2%.

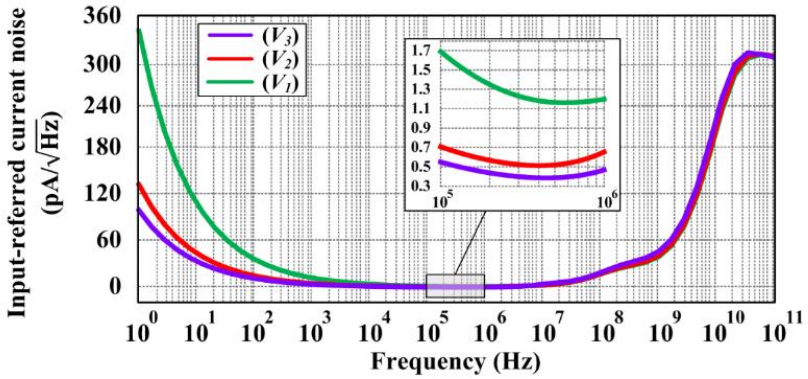

Figure 6. Input-referred noise current for the three transimpedance gains activated by the control voltages V_1, V_2, V_3. In the inset, the magnification in the reduce range of frequencies from 100 kHz to 1 MHz.

Additionally, as a case example of the analysis of the electronic circuit response in the time domain, a further series of simulations has also been performed. In particular, a pulsed photocurrent I_{IN} at a repetition rate of 50 Hz has been generated as the ideal current source of the Si PD electrical model shown in Figure 2 [10,37–41]. According to the upper panel of Figure 7, the considered I_{IN} as a function of time has the following main characteristics: rise- and fall-times equal to of 1 µs and 100 µs, respectively; 10 µs pulse-width; 400 nA current peak amplitude; 1 nA minimum current amplitude corresponding to the typical Si PD dark current. These parameters of the photocurrent I_{IN} have been chosen to emulate the behavior of fluorescence or phosphorescence emissions from biomarkers excited by laser pulses used as label-free aptasensors in many applications in biology and medicine for diagnosis and therapeutic control [10,37–41]. Recalling the considered standard values of the PD shunt and series resistances R_{SH} = 100 MΩ and R_S = 50 Ω, as well as of the junction capacitance C_J = 8 pF, and taking into account their filtering effect on the pulsed photocurrent I_{IN}, the corresponding effective input current signal I_{PD} of the electronic circuit (see Figure 2) is reported in the middle panel of Figure 7. Moreover, the lower plot of Figure 7 shows the TIA output voltages V_{OUT} as a function of time and for the three different circuit transimpedance gains (as described above), considering the fine-tuning control voltage V_{AN} fixed to 1.8 V. As shown in Figure 7, the circuit output voltage offset is about 810 mV, corresponding to the PD dark photocurrent I_{IN} = 1 nA, while the peak values of the output voltage signals V_{OUT} are about: (i) 860 mV (i.e., 810 mV + 50 mV) by activating the control voltage V_1 corresponding to the transimpedance gain of about 126 kΩ (i.e., 102 dB); (ii) 980 mV (i.e., 810 mV + 170 mV) by activating the control voltage V_2 corresponding to the transimpedance gain of about 447 kΩ (i.e., 113 dB); and (iii) 1390 mV (i.e., 810 mV + 580 mV) by activating the control voltage V_3 corresponding to the transimpedance gain of about 1585 kΩ (i.e., 124 dB). These results are in very good agreement with the transimpedance gain values achieved by performing the frequency domain simulations previously reported in Figure 4. Moreover, referring to the circuit setting with its maximum transimpedance gain of about 124 dB, the achieved equivalent input-referred current noise is about 16.4 pA/$\sqrt{\text{Hz}}$ evaluated at the repetition rate equal to 50 Hz of the input pulsed photocurrent I_{IN}.

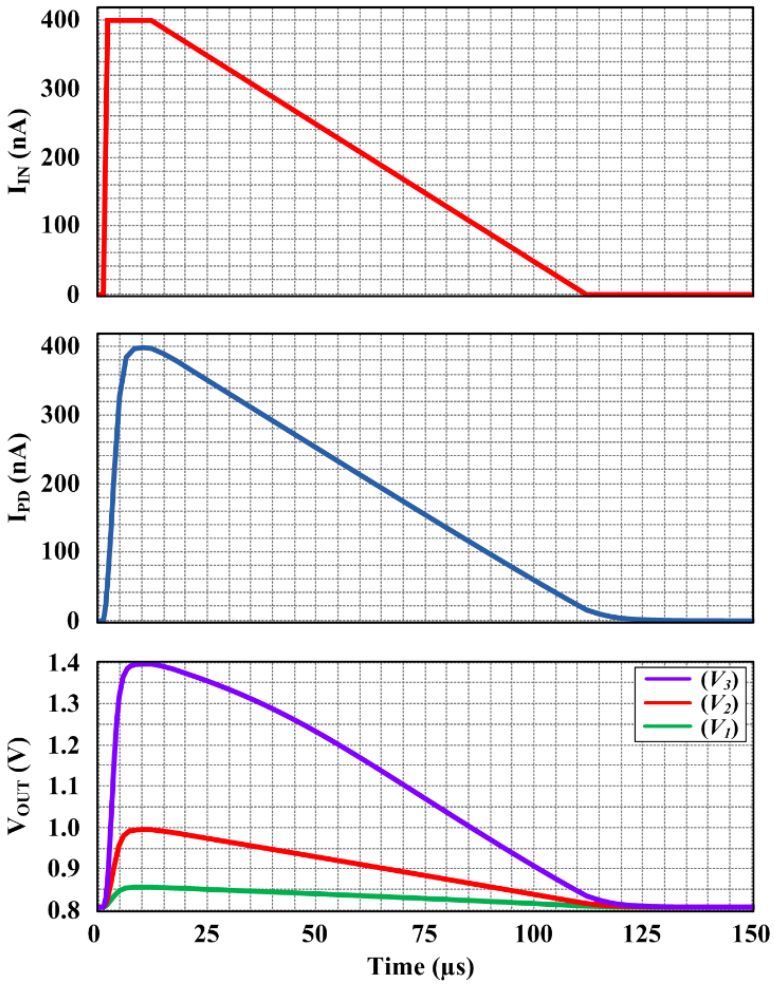

Figure 7. Upper panel: pulsed photocurrent I_{IN} generated the PD. Middle panel: input pulsed current signal of the electronic circuit. Lower panel: circuit output voltage for different values of the circuit transimpedance gain.

Besides, from the bias point analysis, the resulting stand-by power consumption of the circuit is about 33 µW with a DC input current I_{IN} = 1 nA (i.e., the PD dark photocurrent). In order to evaluate the circuit power consumption under the AC pulsed regime, the PD pulsed photocurrent I_{IN} previously described has been also considered and under these operating conditions the circuit power consumption varies from 33.1 up to 36.1 µW for the transimpedance gain equal to 102 dB and 124 dBΩ, respectively.

Finally, Table 2 summarize the main characteristics, performances and parameters of the proposed circuit together with those ones of similar solutions reported in the literature. In particular, by comparing the present results with those ones from comparable solutions specifically designed for biomedical applications [24,26], the proposed TIA demonstrates significant improvements especially in terms of the resulting low-power consumption, low input noise, high and tunable transimpedance gain, wide bandwidth, small Si area and Figure of Merit (FOM, as defined in Table 2).

Table 2. Main circuit characteristics and its comparison with the state-of-the-art.

[Ref] Year	[22] 2019	[23] 2018	[24] 2016	[25] 2020	[26] 2019	[This Work] 2021
CMOS Technology (μm)	0.35	0.35	0.18	0.18	0.35	0.18
Supply Voltage (V)	2.0–3.7	2.7–4	1.2–1.8	±0.9/1.8	3.3	1.8
Si Area (mm^2)	0.64	1.68 + 0.74 (PD)	37.7	0.12	N.A.	0.002 + 0.01 (PD)
Achieved Results	Measured	Measured	Measured	Measured	Simulated	Simulated
Circuit Operating Mode	Continuous	Pulsed	Pulsed	N.A.	Sinusoidal	Pulsed
Transimpedance Gain (dBΩ)	135–142	144	84–127	107	120	102–124
Bandwidth (Hz)	10	50	64	7 M	8.2 M	1.15 M (@ 102 dBΩ) 555 k (@ 124 dBΩ)
Power Consumption (μW)	15	3360	135	5200	330	33.1 (@ 102 dBΩ) 36.1 (@ 124 dBΩ)
Input Noise $\left(pA/\sqrt{Hz}\right)$	42	79	27	1.7	3.5	0.39 (@ 124 dBΩ) 1.2 (@ 102 dBΩ)
FOM (Ω × GHz/mW)	8.4	0.24	1.06	301	24.8k	24.4k (@ 124 dBΩ) 4.4k (@ 102 dBΩ)

4. Conclusions

The paper reports on the detailed description of a novel architecture of a transimpedance amplifier as an analog front-end circuit operating in low-voltage, low-power regime for wearable, portable and implantable sensor systems capable to operate with nanoampere input current pulses. The circuit has been designed at transistor level in TSMC 0.18 μm standard CMOS technology with a reduced number of components and with an integrated photodiode needed for optoelectronics sensor applications in biomedicine. The complete implemented circuit layout, with a Si area equal to 2070 μm^2, is powered at 1.8 V with a maximum power consumption of about 36.1 μW. Moreover, the circuit is capable of providing variable transimpedance gains ranging from 102 to 124 dBΩ, achieved by both coarse- and fine-tuning operations, showing a wide bandwidth up to 1.15 MHz. The main performances of the circuit have been evaluated by performing post-layout simulations in CADENCE Design System employing as input pulsed currents the typical ones generated by a photodiode in optical biosensors optoelectronic sensing systems. Moreover, a complete Corner Analysis including process variations has been performed to validate the robustness of the response of the proposed circuit to variations of the operating temperature from −25° to +75 °C as well as of the power supply voltage of 5% respect to its nominal value. Finally, a summary table is also provided to compare the performances and the characteristics of the proposed circuit with respect to those ones of other similar systems and solutions reported in the literature designed for biomedical applications.

Author Contributions: The authors contributed equally to this work. In particular: G.D.P.S. simulated and implemented the circuit in Cadence, and he contributed to writing and editing the manuscript. A.D.M. developed the new technique/solution and its theory, and he contributed to writing and editing the manuscript and coordinated the manuscript elaboration. G.B. simulated and implemented the circuit in Cadence, and he contributed to writing and editing the manuscript. M.F. analyzed the result data of the system contributing to theoretical discussions, and he contributed to writing and editing the manuscript. E.P. developed the optoelectronic/photonic components for sensing applications and analyzed the result data, and he contributed to writing, editing and supervising the manuscript. U.G. supplied the overall system specifications and constrains and analyzed the result data, and she contributed to writing and editing the manuscript. All authors have read and agreed to the published version of the manuscript.

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