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Broadband Modeling and Simulation Strategy for Conducted Emissions of Power Electronic Systems Up to 400 MHz

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Abstract: Energy efficiency is becoming one of the most important topics in electronics. Among others, wide band-gap semiconductors can raise efficiency and lead to shrinking volumes in power conversion systems. As different markets have regulations that require different designs, it is necessary to cope with a large variety of similar designs. By using effective modeling and simulation strategies, the efforts of building these variants can be diminished, and re-designs can be avoided. In this paper, we present a universally valid way to come to reasonable simulation results for conducted emissions of a power electronic system in the frequency range from 150 kHz up to 400 MHz. After giving an overview of the state-of-the-art, the authors show how to implement and set up a simulation environment for a gallium-nitride (GaN) power converter. It shows how to differentiate between important and not that important components for Electromagnetic Compatibility (EMC), how to model these components, the printed circuit board, the load, and the setup, including the Line Impedance Stabilization Networks (LISNs), etc. Multiport S-parameter strategies as well as vector fitting methods are employed. Computational costs are kept low, and all simulations are verified with measurements; thus, this model is valid up to 400 MHz.

Keywords: electromagnetic interference (EMI); power electronic systems; simulation methodology

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1. Introduction

As decarbonization requires a higher share of electric power, the importance of power electronics also increases. Most power electronics use switching transistors, and the application of new types of transistors such as silicon-carbide (SiC) and gallium-nitride has led, due to the possibility of much faster switching and, consequently, less heat dissipation, to a significant volume reduction in power electronic systems. However, fast switching comes at the cost of higher electromagnetic emissions: a factor of 10 faster rise time results in 20 dB more emissions at large frequencies [1].

To avoid expensive redesigns when emission requirements are not met, computer simulation has become an indispensable tool in designing and optimizing the electronic and electromagnetic properties of power electronics. Often, circuit simulations are used, which are augmented by parasitic elements to include electromagnetic properties of the electromechanical setup of the test system.

Rondon-Pinilla et al. [2] used this approach to model a buck converter with an SiC junction-gate field-effect transistor (JFET). To predict its conducted emissions up to 30 MHz, they propose to model the parasitics by means of impedance-measurement-based circuit models, whereas a behavioral model based on known physical properties was used to model the transistor. Conducting time domain simulations, the authors achieved devi-

ations between measurement and simulation below 5 dB up to 10 MHz and up to 10 dB between 10 MHz and 30 MHz.

In [3], Ishii et al. propose a similar strategy to model the parasitics, but they used a measurement-based behavioral model for their transistors. Similar deviations are observed up to 10 MHz, whereas higher deviations, as in [2], are reported for frequencies between 10 MHz and 30 MHz.

In contrast to the two previously summarized papers, Chen et al. [4] propose developing circuit model descriptions for the paracitics of a switched-mode power supply by means of 3D full-wave finite element (FE) simulations. However, they restrict their FE simulations to the description of the mutual coupling of specific components. It turns out that for frequencies up to 10 MHz, good agreement between simulation and measurement is observed. For higher frequencies, deficiencies in their models are given.

Schröder et al. [5] investigate the switching behavior of a power module in a double-pulse setup. They compare the impact of three different FE simulation-based models: two models developed at fixed frequencies (10 Hz and 1 MHz) and a broadband macro-model based on vector fitting (VF) [6]. A significant impact from the model types is reported. The parasitics model obtained from the 10Hz simulation in particular is not able to predict prominent effects such as skin effects. Furthermore, it is reported that for frequencies higher than 100 MHz, the used transistor models are insufficient.

Zhang et al. [7] report the radiated electromagnetic interference of a 7.2 W dual active bridge DC–DC converter. The circuit model, which is used to prescribe the emissions, is developed by means of measurements of the entire setup in an anechoic chamber. The switching device is characterized by measurements, too. Up to frequencies of 500 MHz, this solely measurement-based model of a DC–DC converter is able to predict the radiated emissions with a 5 dB deviation from the measurement.

A similar approach is used in [8] to predict the radiated emissions of an automotive converter up to 500 MHz. In addition to the measurement-based models of cabling, etc., an FE simulation-based model of the converter's PCB is incorporated in the model-based EMI prediction. The main advantage of this approach is that the impact of changes in the layout can easily be investigated. Nevertheless, coupling effects between components on the PCB are not taken into account.

The RF interference in mobile platforms caused by switched-mode power supplies is addressed in [9,10]. Here, current paths that enable the transistor to create noise are identified and modeled using HSPICE circuit descriptions. The transistor is also modeled in HSPICE, which requires corresponding libraries.

In [11], the radiated emissions analysis of switching regulators used in laptops is performed on the basis of simulation only. The PCB is modeled using the 3D solver of the CST Studio Suite® [12]. This software uses vector fitting to obtain a circuit representation of the computed structure, which is then solved in a transient simulation. With the known currents and voltages at the circuit ports, the radiated fields around the 3D structure can be computed. The authors use a SPICE model of the switches and investigate resonances in the radiated fields up to 1 GHz.

The same approach is chosen in [13], where Ansys tools [14] are used for a power module with wide band-gap SiC MOSFETs of 1200 V/36 A. A behavioral model of the transistors is created based on data-sheet information. This model is used in a circuit simulation, which is complemented by circuit parasitics obtained from a 3D electromagnetic solver, and a comparison to measurements is made up to 100 MHz. It is reported that the frequencies of the spectral peaks are approximately matched, but the amplitude differs by several orders of magnitude.

Whereas modeling electromagnetic emissions in the range of up to 100 MHz is well-established, we conclude that above 100 MHz, many different approaches exist. Lots of effort is spent on the examination of the impact of the 3D geometry and on modeling the transistor as noise source. References to the measurement of the device under test are needed to verify assumptions and calibrate the computer model.

In this paper, we develop a universally valid approach to simulate the conducted electromagnetic interference (EMI) of power systems. According to the standard CISPR25 [15], conducted emission measurements are performed up to a frequency of 108 MHz to cover the FM radio range. However, comparably new services are found at higher frequencies (e.g., Digital Audio Broadcasting (DAB) is performed between 170 MHz and 230 MHz), and conducted measurements are often performed far beyond 108 MHz to obtain an estimate of the emission. For this reason, our model aims to extend the very high-frequency (VHF) band which ends at 300 MHz [16].

We particularly pick up on the description of the impact of the 3D geometry and on transistor models. As a demonstration, we use a four-layer printed circuit board (PCB) with a halfbridge composed of two gallium-nitride (GaN) semiconductors, which drive a resistive–inductive load. We show that the PCB can be completely modeled in a 3D simulator without any further, time-consuming simplifications. Additionally, we propose a simple model that accurately describes the GaN semiconductor based on datasheet information and the measurement of the switching event. More precisely, we answer the following questions:

- Which parts of the system are best characterized by solving Maxwell's Equations, and which method must be to solve them?
- Which parts of the system must be characterized by measurement?
- What is needed to efficiently generate a transistor model, and what are its accuracy limits?
- With which method are all the above-mentioned components combined into a system simulation that predicts emissions?

Answering these questions, we establish a 10-point procedure using the CST Studio Suite that allows us to conveniently set up robust simulation models for many types of power electronic systems. We validate our model by measurements up to a frequency of 400 MHz.

2. Measurement Setup

This work considers a measurement setup in resemblance to standardized automotive tests [15] to obtain reliable and reproducible measurement results. The frequency range of interest is from 9 kHz–400 MHz, and a bandwidth of 9 kHz was used for EMI measurements with an EMI receiver.

2.1. Device under Test (DUT)

The device under test (DUT) is a printed circuit board (PCB) equipped with a GaN halfbridge (HB) stage. Figure 1 is a photo of the populated PCB, pointing out the relevant components. The 4-layer board is intended for general demonstration purposes, hence, it is built in a modular manner and offers multiple test structures to enable access to various signals, which are not used for this work. The functional circuit can be simplified to the view given by Figure 2. The halfbridge is made from two 600 V CoolGaN^{TM} IGOT60R070D1 by Infineon [17]. The Gate signal is generated with an external waveform generator and processed on the board with an auxiliary gate driving circuit. Two DC link capacitors [18] of nominally 1 µF (designated C_{100}, C_{101}) are connected between the DC+ and DC− nodes. The load is an RL series circuit attached between the switched node and DC+. It is composed of a power resistor with aluminum housing and a high current power inductor with nominal values of 10 Ω and 10 µH and approximately 15 cm wire on both ends, see Figure 3.

Typical time domain waveforms are displayed by Figure 4. Visible is the signal period of 5 µs and hence the fundamental switching frequency of 200 kHz, as well signal distortions when switching the inductive load. The supply line current drawn from the positive supply, DC+, is the relevant quantity for the conducted emission measurement described in the following section.

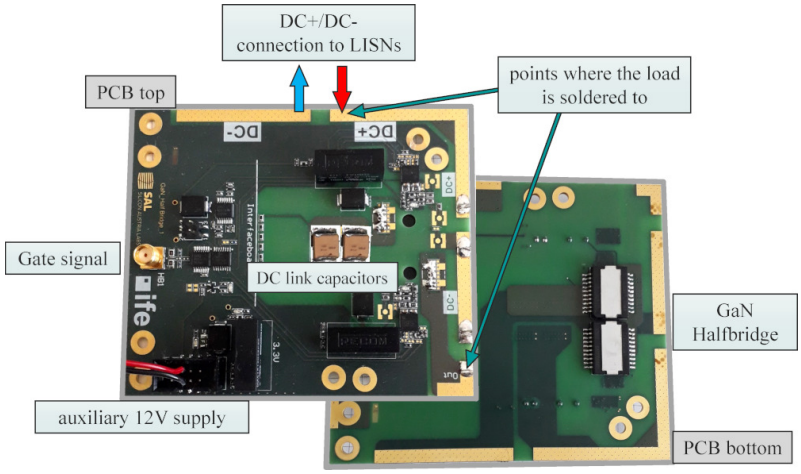


Figure 1. Photo of the DUT PCB top and bottom side.

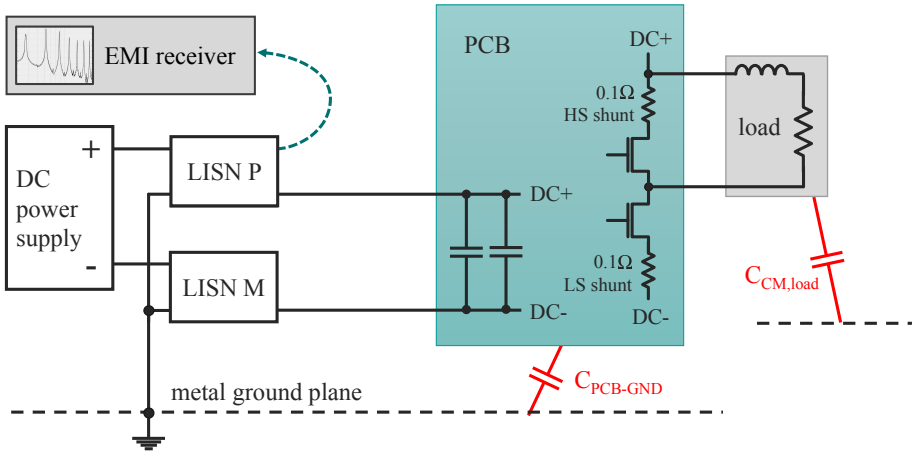


Figure 2. Schematic view of the conducted emission test setup. Parasitic coupling capacitances between PCB, load, and underlying GND plane are displayed in red. The EMI receiver is connected to the output of the positive supply LISN P. The unused output of LISN M is terminated by 50 Ω.

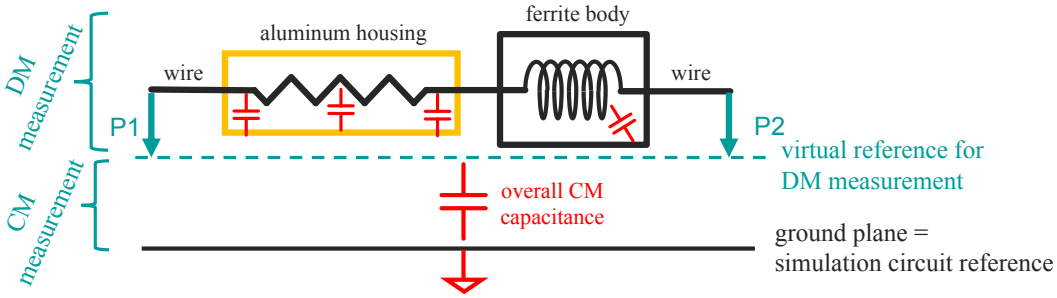


Figure 3. Measurement concept to obtain DM and CM load impedance for circuit simulations, reflecting the setup of interest. The CM measurement captures the overall coupling capacitance towards the common ground plane.

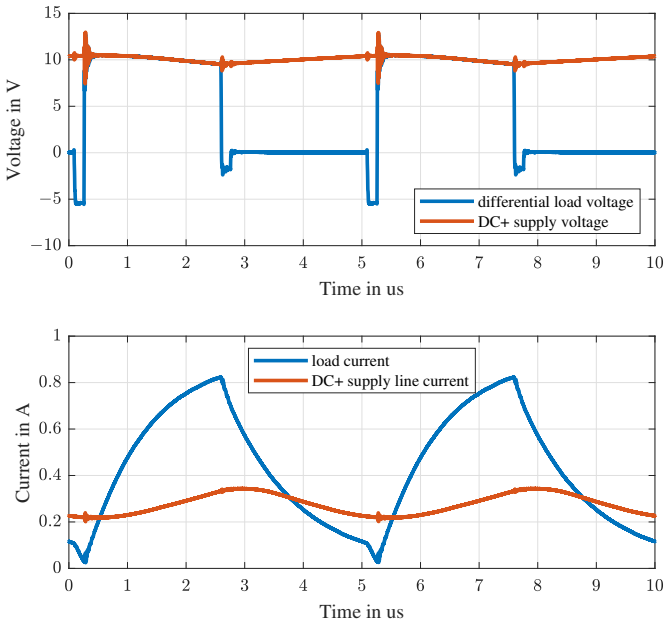


Figure 4. Time domain signals captured with an oscilloscope while the DUT was supplied with 10 V. The differential voltage at the load is measured between DC+ and the switched node.

2.2. Conducted Emission (CE) Measurement Setup

In resemblance to standardized automotive tests, the measurement of the supply line conducted emission is setup as illustrated by Figures 2 and 5. DUT and load are placed 5 cm above a 1 m × 2 m GND plane, but are not locally grounded. Thus, there is parasitic capacitive coupling between the floating PCB, load, and underneath GND plane, as denoted by the elements $C_{\text{PCB-GND}}$ and $C_{\text{CM,load}}$ in Figure 2. During CE simulation, both need to be considered, as will be discussed later.

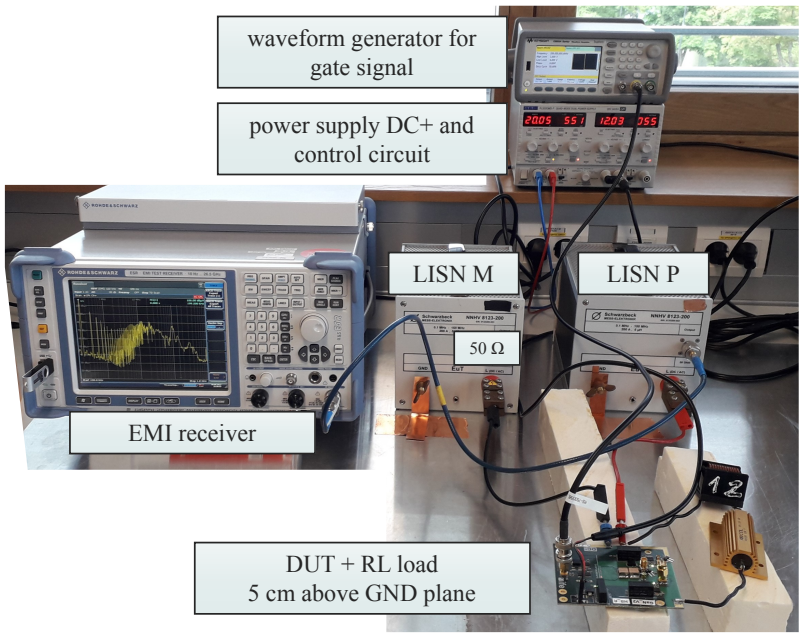


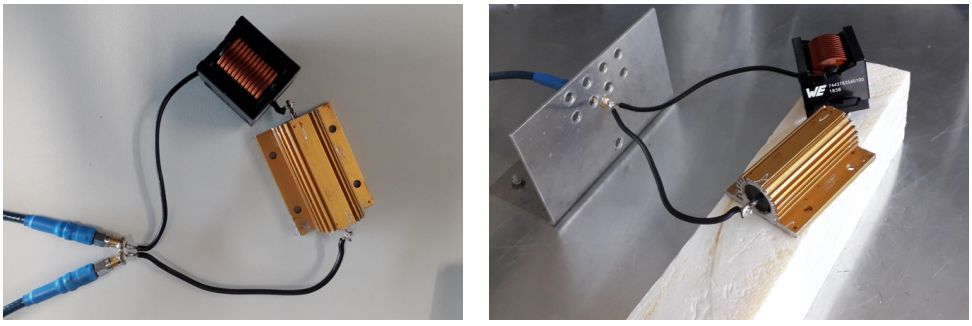
Figure 5. Photo of the conducted emission measurement setup. The EMI receiver was connected to the output of the positive supply LISN P. Common GND is the metallic plane. The unused output of LISN M was terminated by 50 Ω. Wires between DUT PCB and LISNs were 30 cm long.

DC+ and DC− supply lines are routed via so-called Line Impedance Stabilization Networks (LISN) [19]. The LISNs' electrical characteristics are mainly defined by an internal 5 µH series inductance. Further details are discussed in Section 3.6.3. Conducted emission measurement results for DC+ voltages of 10 V and 60 V are shown in Section 4, where they are compared to the simulated values obtained by the procedure presented in this work.

2.3. Differential and Common Mode Impedance of the Load

The load's differential mode (DM) impedance affects the HB switching transient behavior, e.g., the rise/fall times and ringing. As the load's geometry is big in size compared to the DUT PCB, its capacitive coupling towards the GND plane has a major impact on the system's overall common mode (CM) impedance. Thus, an accurate and broadband load model is needed for simulation. Detailed geometrical and electrical information of such components is rarely available. Instead, such a model is conveniently obtained by S-parameter measurement from 9 kHz to 400 MHz using a 2-port vector network analyzer (VNA). The measurement results of such loads can conveniently be stored in a library and reused whenever new power electronic prototypes are developed. The derivation of simulation models is detailed in Section 3.6.4.

Figures 3 and 6 show the measurement concept and setup used to measure the load impedance (DM measurement) and the parasitic coupling between the load and common ground plane (CM measurement). The results are displayed in Section 3.6.4, which gives a direct comparison to the impedances of the simulation models which were derived from the measured data.



(**a**) (**b**)

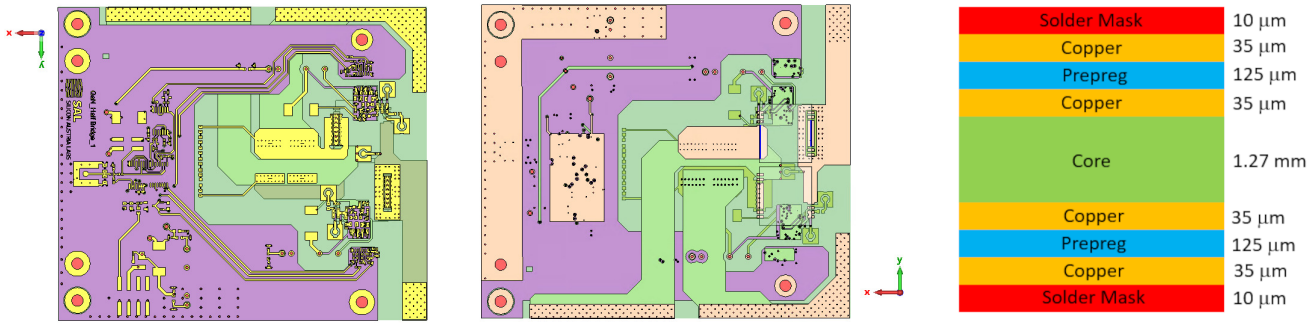
Figure 6. (**a**) Measurement of the load's series impedance with a 2-port VNA. (**b**) Measurement of the coupling capacitance between load and GND plane to obtain the value of $C_{CM,load}$. Here, only one port of the VNA is used, with both wires soldered to the inner conductor of the SMA connector. Reference is the metal fixture connected to the GND plane.

3. Modeling

In this section, the development of a numerical 3D model of the DUT and the measurement setup presented above is discussed. These models can be utilized to predict the conducted EMC behavior from 9 kHz up to 400 MHz.

3.1. Three-Dimensional EM Model of PCB and Measurement Setup

First, a 3D model of the PCB is generated by importing the respective ODB++ data files into the CST Studio Suite. The result is depicted in Figure 7a,b. The board comprises four conductive copper layers, a substrate core material, and two prepreg insulation layers (see Figure 7c). The PCB material parameters are summarized in Table 1, where the values for the relative permittivity of the substrate core material, the dielectric prepreg, and the solder mask are manufacturer recommendations.



(**a**) (**b**) (**c**)

Figure 7. (**a**,**b**) are the top and bottom views of the 3D model of the test PCB. The 3D geometry of the PCB is imported from odb++ data files. (**c**) detailed stackup of the test PCB using 4 metal layers.

Table 1. Material parameters used for the test PCB.

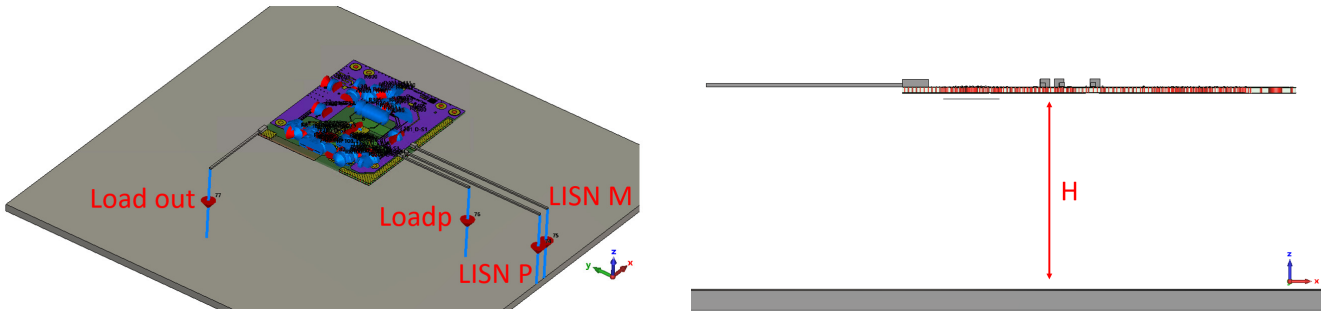
Material	Material Parameters
Copper	$\sigma_{cu} = 5.8e7 \frac{S}{m}$
Core	$\varepsilon_{r_{core}} = 4.4$
Prepreg	$\varepsilon_{r_{prepreg}} = 3.9$
Solder mask	$\varepsilon_{r_m} = 3.5$

The conducting layers are modeled by using a surface impedance material model available in the CST Studio Suite [20]. This model significantly reduces the computational effort because it only requires numerical solutions on the conductor surface. Hence, there is no discretization of the region needed within the conductor. However, this surface impedance model is only accurate if the skin depth within the conductor is smaller than its thickness. Therefore, one must estimate the model inaccuracies exhibited by this simplified material model where the skin depth exceeds the conductor's thickness. For our simulations, we considered that copper exhibits a conductivity $\sigma_{cu} = 5.8e7 \frac{S}{m}$ and a relative permittivity $\mu_r = 1$; hence, one can calculate the lower frequency limit of the surface impedance model as follows:

$$f_{min} = \frac{1}{\pi(\frac{d}{2})^2 \mu_0 \mu_r \sigma_{cu}} \tag{1}$$

where d is the conductor thickness. By substituting the values from Figure 7c and Table 1 for d, σ_{cu}, and μ_r, one obtains a lower frequency limit of f_{min} = 14.26 MHz; hence, the conductor losses are not estimated properly up to 14.26 MHz by the surface impedance model. However, these losses were investigated by means of numerical simulations, and they do not exceed 10 mΩ. Therefore, they are presumed negligible compared to the losses caused by the external shunt resistors mounted on the PCB (see Figure 2).

To obtain simulation results that are comparable to CISPR25 [15] measurements, one has to model not only the investigated PCB but also the test bench setup, including the metal reference table and supply cables connected to the LISN networks (see Figure 8a, LISN M/P) and the load (see Figure 8a, Load out/p), respectively. This work considers a test setup, where the PCB is placed 50mm above a metal table, as shown in Figure 5.



(**a**) (**b**)

Figure 8. Three-dimensional model of the complete test setup including the test PCB, the metal reference table with a distance of $H = 50$ mm, and the supply cables. The LISN networks are connected to LISN M/P, and the load is connected between Load out and Loadp. (**a**) top view; (**b**) front view.

3.2. Component Modeling

To fully characterize the behavior of a PCB, one must also consider the electromagnetic behavior of external components which are mounted on the PCB to operate the circuit. The investigated test PCB has in total 176 mounted components (see Figure 1) which may influence the conducted EMC's behavior. One may investigate the influence of all single components on the overall EMC behavior, but this approach is computationally very expensive; therefore, it is not feasible. The presented approach categorizes the components into two groups. The components which are not part of the halfbridge circuit shown in Figure 2 comprise the first group. These components do not experience fast-switching, high-load currents; therefore, it is presumed in a first approximation that their impact on the conducted emissions due to parasitic and non-linear effects is negligible for the frequency range of interest.

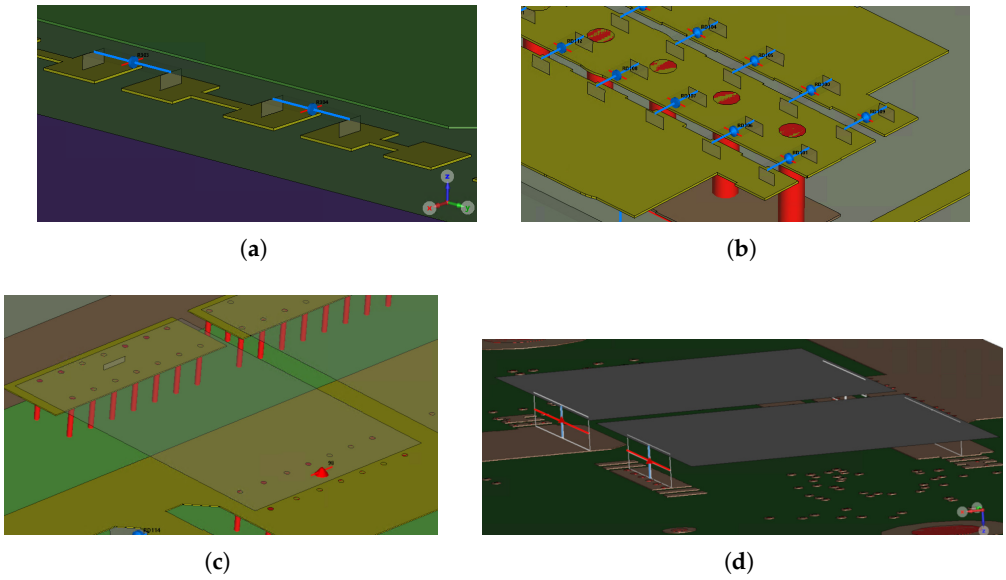
The components which are part of the halfbridge circuit (see Figure 2) comprise the second group, and they are considered critical since they experience fast switching load currents; hence, their impact on the conducted EMC behavior is investigated very carefully. An exception are the shunt resistors present in the halfbridge circuit since the manufacturer ensures a tolerance of 1% and a high reliability [21]. Therefore, these resistors are included in the first component group.

The two component groups are treated differently in the 3D model. The electromagnetic behavior of the first component group is considered directly in the 3D FEM simulation in terms of impedance boundary conditions (face lumped elements). Therefore, component variations are not considered in the simulations. The electromagnetic behavior of the critical components is not directly considered in the 3D FEM simulation. Instead, an interface to a SPICE simulation framework is defined (face lumped port) for each of these components where arbitrary external circuit elements can be attached. The two modeling approaches for the components are discussed in detail in Sections 3.2.1 and 3.2.2.

3.2.1. Face Lumped Elements

All components that are part of the first component group are treated as ideal components; hence, they are modeled as face lumped elements with ideal electrical behavior, as depicted in Figure 9a,b. With this modeling approach, one can consider the electrical R, L, and C behaviors of the corresponding component within the 3D simulation using surface impedance boundary conditions. Although the simulated parasitic self-inductance of these lumped element models, as well as their mutual inductive coupling, exhibits certain inaccuracies. they are still feasible to approximate parasitic inductive effects, as discussed in [22]. The significant advantage of these models is their simplicity in terms of computational effort and that they can be generated automatically from the imported

odb++ database in the CST Studio Suite. Therefore, a large number of external components can be considered with very low modeling and computational effort.



(**a**) (**b**)

(**c**) (**d**)

Figure 9. (**a**,**b**) Face lumped elements to model the ideal electrical behavior of resistors, inductors, and capacitors which are not part of the halfbridge circuit. (**c**) Face lumped ports to investigate the impact of the capacitors between DC+ and DC− on the EMC's behavior. (**d**) Face lumped ports to investigate the impact of the transistors on the EMC behavior.

3.2.2. Face Lumped Ports

The components that are part of the second component group are of special interest since it is presumed that they dominate the conducted EMC characteristics up to 400 MHz due to fast switching load currents through the devices. To verify this presumption, we modeled these components with face lumped ports (see Figure 9c,d) to investigate their impact on the overall conducted EMC characteristics. These face lumped ports enable an interface between 3D FEM simulation and SPICE simulation; hence, arbitrary circuit models of the components can be attached to identify the source of conducted emission peaks. The CST Studio Suite provides a feature that allows the automatic generation of such face lumped ports from the imported odb++ database. The generation of face lumped ports is very similar to the generation of face lumped elements, and hence their modeling effort is also low. However, the number of ports significantly influences the computational effort since each port must be excited by the electromagnetic solver to determine its reflection and transmission behavior. Therefore, one should keep the number of ports as small as possible to facilitate a computationally efficient 3D simulation.

3.3. EM Solver and Computational Effort

The 3D numerical simulations were performed in the CST Studio Suite using the finite element method (FEM) in the frequency domain with tetrahedral mesh cells. In the frequency domain, the Maxwell's equations are [23]:

$$\nabla \times \vec{E} = -j\omega\vec{B} \tag{2}$$

$$\nabla \times \vec{H} = \vec{J} + j\omega\vec{D} \tag{3}$$

$$\nabla \cdot \vec{D} = \rho \tag{4}$$

$$\nabla \cdot \vec{B} = 0 \tag{5}$$

where $\vec{E}$ and $\vec{H}$ are the electric and magnetic field strengths, respectively; ω is the angular frequency; $\vec{J}$ is the total current density comprising conduction current density $\vec{J_c}$ and source current density $\vec{J_s}$; $\vec{D}$ and $\vec{B}$ are the electric and magnetic flux density, respectively; and ρ is the electric charge density. The constitutive equations are as follows [23]:

$$\vec{H} = \mu_0^{-1}\mu_r^{-1}\vec{B} \tag{6}$$

$$\vec{D} = \varepsilon_0\varepsilon_r\vec{E} \tag{7}$$

$$\vec{J_c} = \sigma\vec{E} \tag{8}$$

where μ_0 and ε_0 are the permeability and permittivity of free space, respectively; μ_r is the relative permeability; ε_r is the relative permittivity; and σ is the conductivity.

Combining Equations (2) and (3) with the constitutive equations lead to the wave equation for the electric field intensity $\vec{E}$:

$$[\nabla \times \mu_0^{-1}\mu_r^{-1}\nabla \times + j\omega\sigma - \omega^2\varepsilon_0\varepsilon_r]\vec{E} = -j\omega\vec{J_s} \tag{9}$$

that is solved in its weak form by the FEM Solver provided in CST. The 3D model is discretized by using a hp adaptive mesh refinement [24] for tetrahedral elements. The adaptive mesh procedure calculates an estimation error of the field solution and improves the mesh quality where the estimation error is high until a convergence criterion is reached [12]. A convergence criterion of 0.04 was recommended by the CST support. The equation system was solved by a direct solver, and a broadband convergence criterion was satisfied after calculating 13 frequency samples. Table 2 summarizes the computational effort for mesh generation and for solving the equation system. As shown, the 3D simulations are computationally comparably expensive; hence, it is not feasible to consider the impact of component variations directly in the 3D simulation model. However, the expensive 3D simulation needs to be run only once, and hence this approach is also valid for electronic-based systems which are more complex than the one investigated in this paper since a computation time of several hours up to one night does not slow down product development time.

Table 2. Computational effort of the 3D numerical simulations using an Intel Xeon E5-2680V2 (10 × 2.8 GHz) and a peak memory usage of 18.9 GB. The results were obtained by using FEM in the frequency domain with tetrahedral mesh cells.

Mesh Cells	Mesh Generation Time (4 Mesh Adaption Runs)	Computational Time (One Frequency Sample)	Total Simulation Time
588,687	30 min	approx 4 min	1 h 17 min

To facilitate detailed studies on the influence of the critical components (component group two) on the EMC characteristic, one can generate a multi-port S-Parameter model (Touchstone.SNP) of the PCB from the 3D simulation results in CST. This multi-port model approximates the electromagnetic behavior of the PCB (including component group one) between the defined ports very accurately within the specified frequency range. The advantage of multi-port models over 3D models is their significantly reduced computational time (2s), and one may connect arbitrary circuit models at the individual ports. The usage of such multi-port S-Parameter models and how they may be used to predict the conducted EMC behavior are discussed in the following section.

3.4. S-Parameter Model

Figure 10 shows the extracted S-Parameter model from the 3D simulation results of the 3D model in Figure 8. The 3D model has in total 10 face lumped ports; hence, the extracted S-Parameter model also has 10 ports where the external components, LISNs, and output load can be connected. Before one starts to connect all the components of interest to the S-Parameter model, it is important to validate its behavior by using AC simulations to avoid systematic errors. Therefore, we considered the following two test cases. First, the HS- and LS ports (drain, source) are shorted and a broadband AC current source with 1 A is connected between LISN P and LISN M (see Figure 11a). The input impedance seen from the current source is analyzed, and since two 0.1 Ω resistors are present in series (see Figure 2), the resulting real part of the input impedance at low frequencies should be approx. 0.2 Ω, which matches the simulation result in Figure 12a. In the second test case, the capacitors C_{100} and C_{101} are connected to the S-Parameter model, while the same current source is connected between LISN P and LISN M (see Figure 11b). The two capacitors have a value of 0.55 µF at the given operation condition, and they are connected in parallel; hence, the resulting imaginary part of the input impedance at f = 100 kHz should be approx. 1.5 Ω, which also matches the simulation result (see Figure 12b).

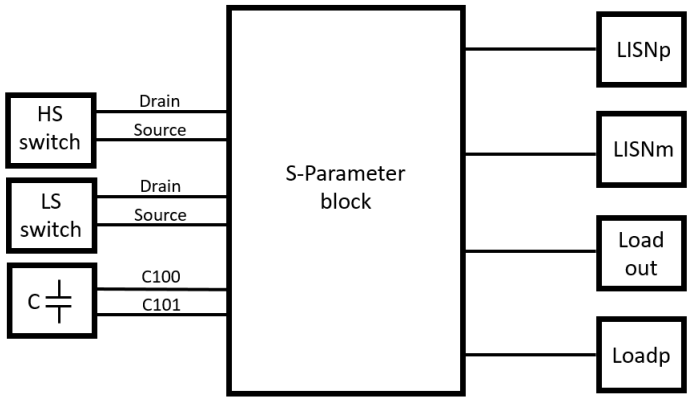


Figure 10. Extracted S-Parameter model from 3D FEM simulations.

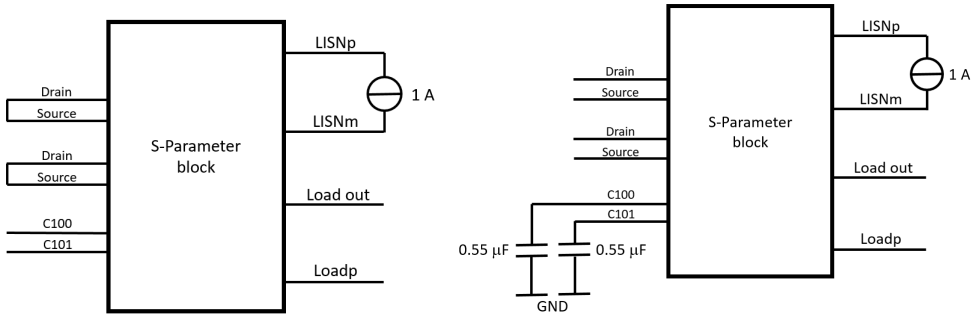
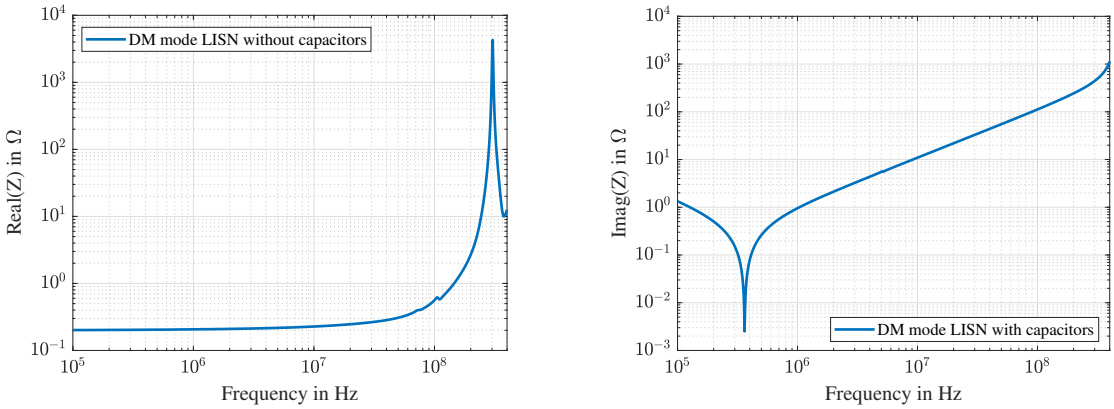


Figure 11. Block diagram for the Validation of the S-Parameter model by using an AC analysis. (**a**) Drain and Source of HS- and LS-switch are shorted and other ports are left open. (**b**) Capacitors C_{100} and C_{101} are connected and the other ports are left open.



(**a**) (**b**)

Figure 12. Validation of S-Parameter model by using an AC analysis. (**a**) Input impedance observed between LISN P and LISN M when Drain and Source of HS- and LS-switch are shorted (see Figure 11a). (**b**) Input impedance observed between LISN P and LISN M when the capacitors C_{100} and C_{101} are connected and the other ports are left open (see Figure 11b).

After validating the S-Parameter model, one is almost ready to simulate the conducted emissions of the test PCB. The final required step is the generation of a SPICE model from the S-Parameter block to enable transient simulations. This SPICE model can be generated by using the vector fitting feature in CST.

3.5. Vector Fitting

Because S-Parameters are frequency domain data, they can not be used directly for transient circuit simulations. In the past years, the vector fitting method has emerged as a powerful method to convert S-Parameter data into a passive and causal circuit ready for circuit simulation in the time domain [6]. It has become a de facto standard for signal integrity simulations [25], and we will also use this method for the application at hand. This methodology allows us to process the S-parameters and extract a corresponding reduced-order model by computing the state-space matrices A, B, C, and D. Computations of such matrices are performed by rational curve fitting. The model will be available in pole/residue form, and a realization process constructs the associated system of ODE's in form of a state-space equation. Passivity enforcement is then applied to such state-space realization, and the final passive model can be then easily synthesized as an equivalent circuit ready to be used in any standard circuit simulation environment such as SPICE [26]. The model generated by the vector fitting methodology allows us to directly apply arbitrary waveforms as excitations in a circuit simulation; thus, the impact of switching frequencies and switching slopes can be directly estimated.

However, the vector fitting process and the required passivisation step underlie certain inaccuracies that must be analyzed carefully to ensure reliable and accurate simulation results. During the fitting process, S-parameters at a fixed port reference impedance are fitted by iteratively increasing the number of poles until sufficient accuracy is obtained (an error criterion of 1×10^{-3} is recommended by the CST support). However, this accuracy is only maintained in the circuit simulation if the same impedances are used as loads in the time domain simulation. If the component models attached to the vector-fitted SPICE model have a frequency dependent impedance that significantly deviates from the impedance that was used in the fitting process, the fitting error might be amplified and lead to inaccurate results in the transient circuit simulation. Our tests have shown that this amplification is more probable with an increasing number of ports.

Therefore, we propose to test the fitting quality not only on individual S-Parameters but also on the system response. For the conducted emission simulations, the coupling

from the noise source to the LISN is of interest. Hence, we set up a test-schematic that allows us to compare the transfer function from the transistor to the LISN ports for the unfitted and fitted case, see Figure 13. To do so, an AC simulation is set up. In the AC simulation, a broadband 1V source is placed on the high side transistor, and the low side transistor is shorted. This setup creates a current loop through all components of the bridge and allows us to quantify the accuracy of the fitted model in system simulations. Figure 14 depicts the comparison of the transfer function from the high side transistor to LISN P for the fitted and unfitted model. We observe great accuracy over the complete frequency band of interest. For clarity, only LISN P is plotted; however, the accuracy for LISN M was also checked.

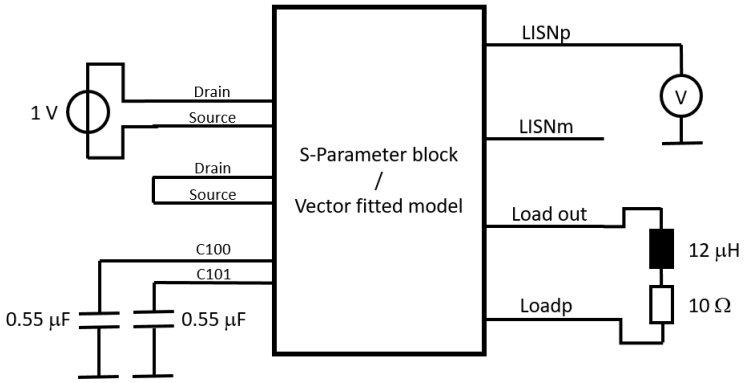


Figure 13. Block diagram for the Validation of the vector-fitted model.

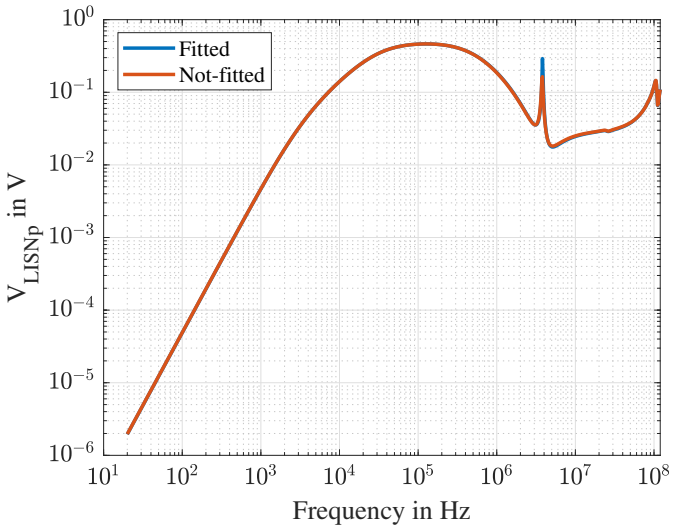


Figure 14. Comparison of transfer function for the vector-fitted and unfitted (S-Parameter) models.

This vector-fitted SPICE model can now be used to perform system level simulations to predict the conducted EMC behavior of the complete test PCB comprising LS- and HS-switches, capacitors, LISNs, and output load.

3.6. Assembly

This section describes the assembly of the complete test PCB, including circuit models for the mounted components, LISN, and the connected load (see Figure 15). The external components are modeled with equivalent circuit models, and their parameter values are extracted from their datasheet if not stated differently.

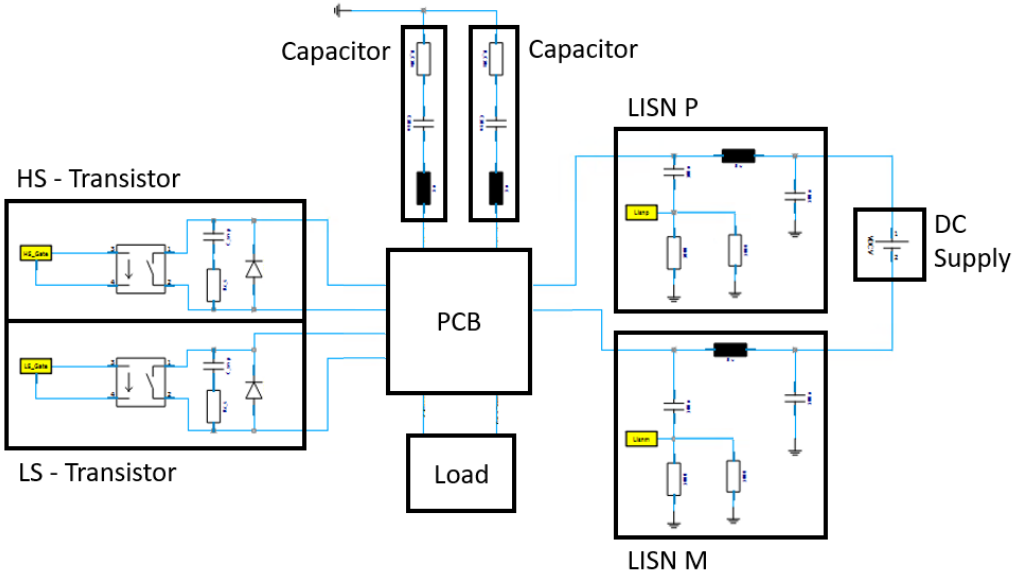


Figure 15. Top-level circuit schematic for the system simulation including the vector-fitted PCB model discussed in Section 3.5 and component models for transistors, capacitors, LISNs, and load.

3.6.1. Transistor Model

The transistor is a critical component when the conducted emissions up to 400 MHz are of interest [1]. Very often, there is no reliable transistor model available from the vendor; hence, one must develop a suitable model by oneself. The development of an accurate transistor model may be difficult due to the voltage-dependent non-linear effects and limited information in the datasheet. Therefore, a simplified equivalent circuit model of the mounted transistors is proposed which only considers the output characteristics between the drain and source. The electromagnetic coupling between the gate and drain/source is neglected in a first approximation. Figure 16 depicts such an equivalent circuit model using an ideal switch with an on-resistance R_{on}, an output capacitance C_p, and a reverse diode D_p. The parameter values R_{on} = 70 mΩ, C_p = 200 pF, and D_p (R_{on}) = 100 mΩ were taken from the datasheet provided by the vendor [17]. One issue which arises by using this equivalent circuit transistor model is the high slew rate of the ideal switch when it is triggered (see Figure 17). To overcome this issue, CST allows the definition of a transition width in the switch model to achieve a smoother switching behavior of the output [12]. Another inaccuracy that must be considered when using the equivalent circuit model is the excessive current oscillation through the transistor model (drain current) when it is switched on, see Figure 18. As shown in Section 4, these excessive currents lead to a significant overestimation of the conducted emissions at 82 MHz. Therefore, an additional resistor R_p is proposed that is placed in series to C_p to dampen the observed current overshoots. Reducing the current overshoots also reduces the simulated conducted emissions at 82 MHz, as shown later (see Section 4). A value of R_p = 10 Ω was chosen arbitrarily to overdamp the switching current, as shown in Figure 18. The two values R_p = 0 Ω and R_p = 10 Ω are considered to investigate the impact of current overshoots on the conducted emissions. The simulation results indicate that the value of R_p should be voltage-dependent to model the transistor behavior at various supply voltages accurately. However, the development of a sophisticated transistor model, including voltage-dependent effects, is not within the scope of this work; rather, we aim to identify how to simplify its behavior to still obtain a reasonable approximation of the conducted emissions. The parameter values for the transistor model are summarized in Table 3. We would like to point out once more that we do not consider voltage-dependent effects with our transistor model, only its switching characteristic.

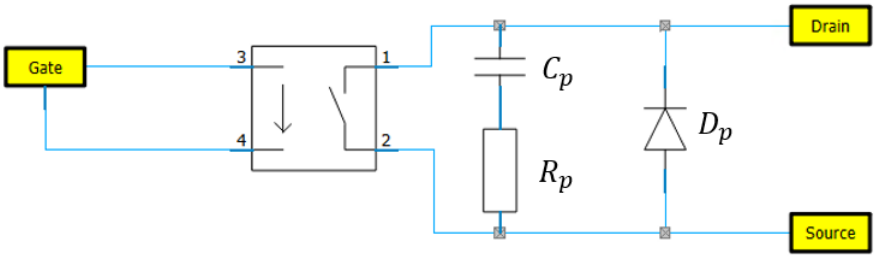


Figure 16. Equivalent circuit model of the mounted transistor. The parameter values are comprised in Table 3.

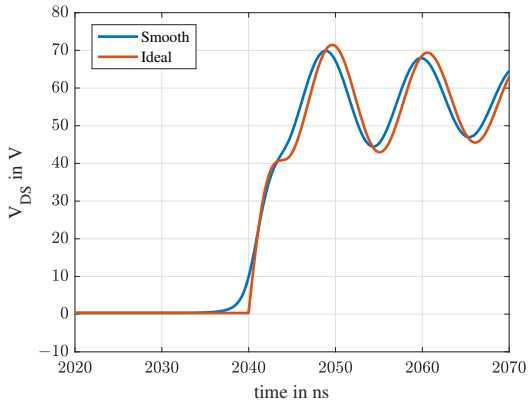


Figure 17. Drain -Source voltage of the high side (HS) transistor (see Figure 15) with an ideal and smooth switching behavior.

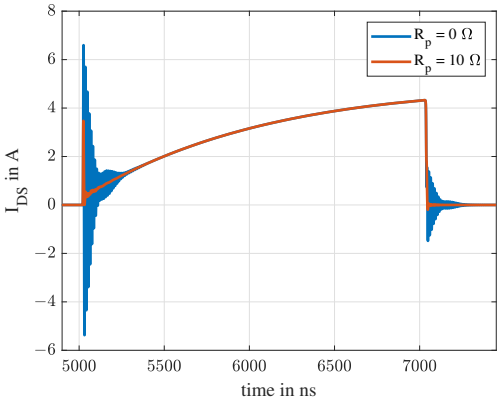


Figure 18. Drain current through the high side (HS) transistor (see Figures 15 and 16) using a smooth switching behavior for different values of R_p.

Table 3. Parameters of the transistor model depicted in Figure 16. Two different values for R_p are considered to study their impact on the conducted emissions.

R_{on}	C_p	R_p	D_p (R_{on})
70 mΩ	200 pF	0 Ω 10 Ω	100 mΩ

3.6.2. DC Link Capacitors

Figure 19 depicts an equivalent circuit model of the DC link capacitors. The parameter values listed by Table 4 reflect the typical characteristics obtained from the datasheet [18]. Although the nominal capacitance of the used high-voltage-rated components is 1 µF, it decreases to about 0.55 µF at the low operation voltage used in this work.

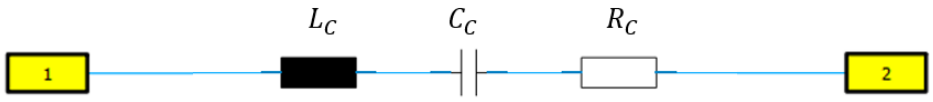


Figure 19. Equivalent circuit model of the mounted capacitors. The parameter values are shown in Table 4.

Table 4. Parameters of the capacitor model depicted in Figure 19 obtained from the datasheet [18].

C_C	L_C (ESL)	R_C (ESR)
0.55 µF	3 nH	12 mΩ

3.6.3. LISN Model

Figure 20 depicts an equivalent circuit model of the used LISNs [19] which is validated up to 150 MHz. The resistor R_{EMI} describes the input and termination resistance of the connected measurement equipment, and the parameter values are summarized in Table 5. Although the equivalent circuit model is only validated up to 150 MHz, it can still be used up to higher frequencies, as shown in Figure 21. Figure 21a compares the simulated and measured impedance at port 1 of the LISN. As shown, the measured impedance deviates from the simulated impedance above 100 MHz. However, this difference in the impedance characteristic does not have a significant impact on the overall conducted emissions, as shown in Figure 21b. To obtain the simulation results in Figure 21b, a vector-fitted SPICE model was extracted from three-port S-Parameter measurements and included in the assembly depicted in Figure 15. Further details regarding the simulation setup are discussed in the next section.

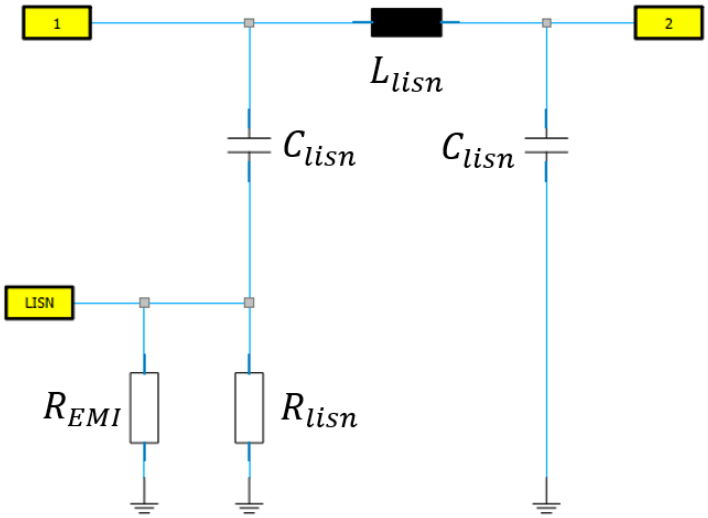
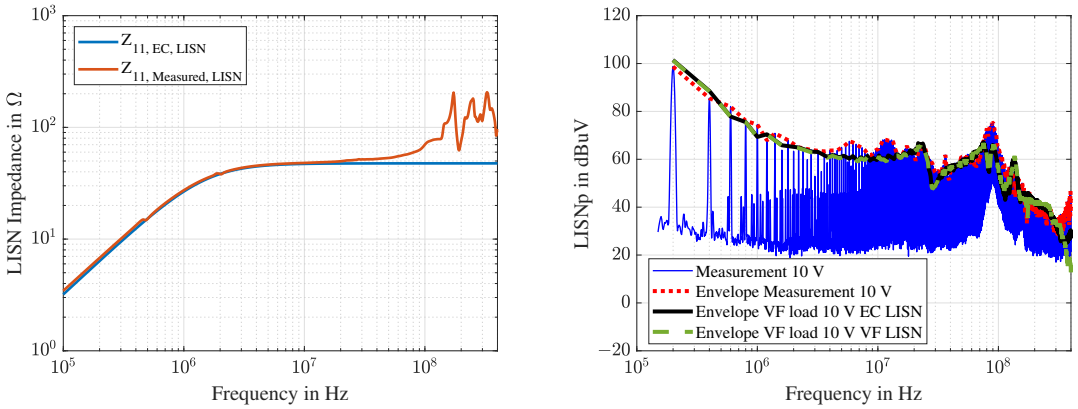


Figure 20. Equivalent circuit model of the LISN [19]. The parameter values are listed in Table 5.



(**a**) (**b**)

Figure 21. (**a**) Simulated and measured LISN impedance of port 1 (Z_{11}). (**b**) Comparison of simulated conducted emissions using the equivalent circuit (EC) LISN model from Figure 20 and a vector-fitted (VF) LISN model extracted from 3-port S-Parameter measurements of the LISN. Up to 350 MHz no difference between EC LISN model and VF LISN model can be observed.

Table 5. Parameters of the LISN model depicted in Figure 20. The parameter values were taken from the datasheet [19], and the parameter R_{EMI} describes the input resistance of the connected measurement equipment (EMI receiver).

L_{lisn}	C_{lisn}	R_{lisn}	R_{EMI}
5 µF	100 nF	1 kΩ	50 Ω

3.6.4. Load Model

Figure 22 depicts two different equivalent circuit models of the load. Figure 22a is a simple circuit model considering only the the load resistor R_{load} = 10 Ω and the first parallel self resonance of the load inductor. The parameter values L_{load} = 12 µH, C_{load} = 12 pF and R_{par} = 4000 Ω are extracted from the DM measurement depicted in Figure 6a. The capacitance $C_{CM,RLCload}$ = 3.6 pF describes the common-mode capacitance between load and metal table and is extracted from the CM measurement shown in Figure 6b. The parameter values are summarized in Table 6.

Figure 22b is an equivalent circuit model extracted from the DM measurement using vector fitting, as described in Section 3.5. This approach provides a sophisticated load model; however, it requires suitable S-parameter raw data, i.e., a sufficient number of frequency points, low noise, etc., and thus careful measurement and potentially pre-processing. The capacitance $C_{CM,VFload}$ = 14.4 pF describes the common mode capacitance between load and metal table and is extracted from the CM measurement to fit the measured CM impedance above 1 MHz. Figure 23a,b compare the DM and CM impedance of the RLC circuit model and the vector-fitted (VF) SPICE model to the measurement data.

Table 6. Parameters of the load model depicted in Figure 22. The parameters R_{load} and L_{load} describe the connected resistor and inductor. The values for C_{load}, R_{par}, $C_{CM,RLCload}$, and $C_{CM,VFload}$ were extracted from DM and CM measurements to model the first parallel self-resonance of the inductor and the capacitive coupling towards the metal table.

R_{load}	L_{load}	C_{load}	R_{par}	$C_{CM,\ RLC\ load}$	$C_{CM,\ VF\ load}$
10 Ω	12 µH	12 pF	4000 Ω	3.6 pF	14.4 pF

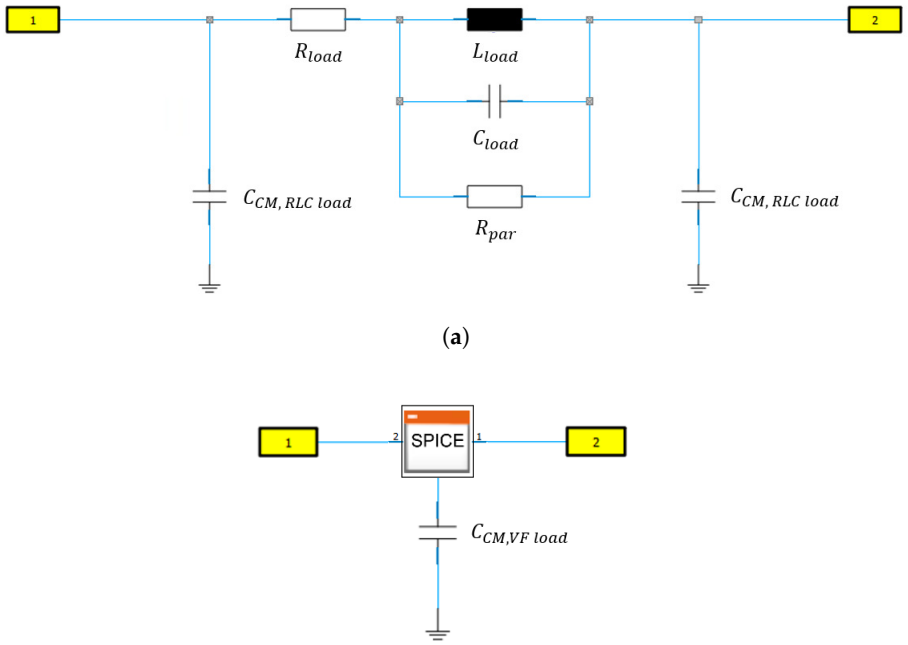


Figure 22. Equivalent circuit model of the connected load. (**a**) Simple RLC circuit model describing only the first parallel resonance and the CM capacitance towards the metal table. (**b**) Equivalent circuit model generated from the DM measurement utilizing vector fitting. The parameter values are comprised in Table 6.

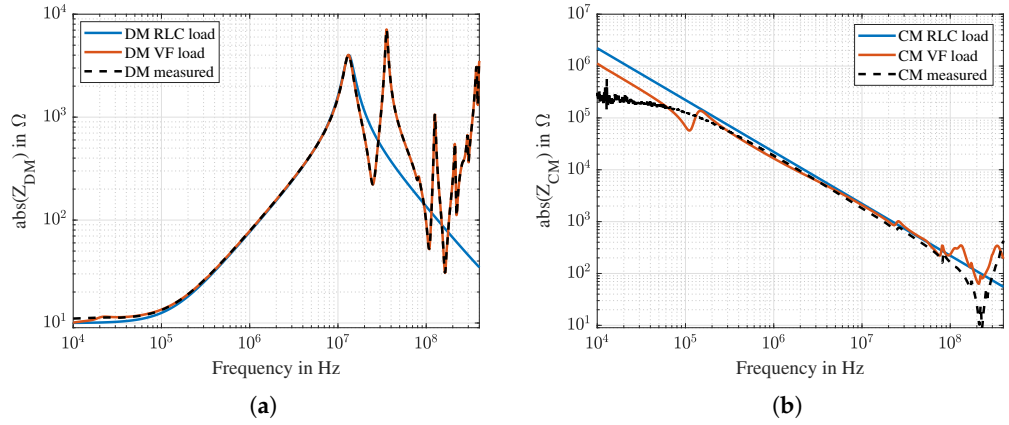


Figure 23. Comparison of the impedance characteristic between RLC load model and VF load model. Respective schematics are displayed in Figure 22. Black dashed lines are the measurement results obtained with the setups from Figure 6. (**a**) DM impedance; (**b**) CM impedance.

3.7. Time Domain Simulation

The time domain simulations of the assembly in Figure 15 are performed in CST Design Studio and are based on a SPICE implementation. The simulation is set up with a duration of 1 ms to ensure that initial transient effects subside. A maximum frequency of f_{max} = 400 MHz and an adaptive time stepping are used in the transient simulator ($t_{step_{max}}$ = 125 ns and $t_{step_{min}}$ = 125 fs). The control voltage at the gate terminal of the transistor model uses an amplitude of 5 V, a frequency of 200 kHz and a duty cycle of 40% (compare Figure 24). Furthermore, the halfbridge uses a break-before-make switching scheme, and hence a dead time of 500 ns is used. The resulting simulated switching behavior of the HS transistor, LS transistor, and the positive supply voltage V_{DC+} are shown in Figure 24a,b. When the HS transistor is either switched on or off, a significant

voltage spike can be observed at the output of LISN P (see Figure 24c). Finally, to obtain the simulated conducted emissions at LISN P, an EMI receiver model [27] is applied to V_{LISN}. The simulated and measured conducted emissions are compared in Section 4.

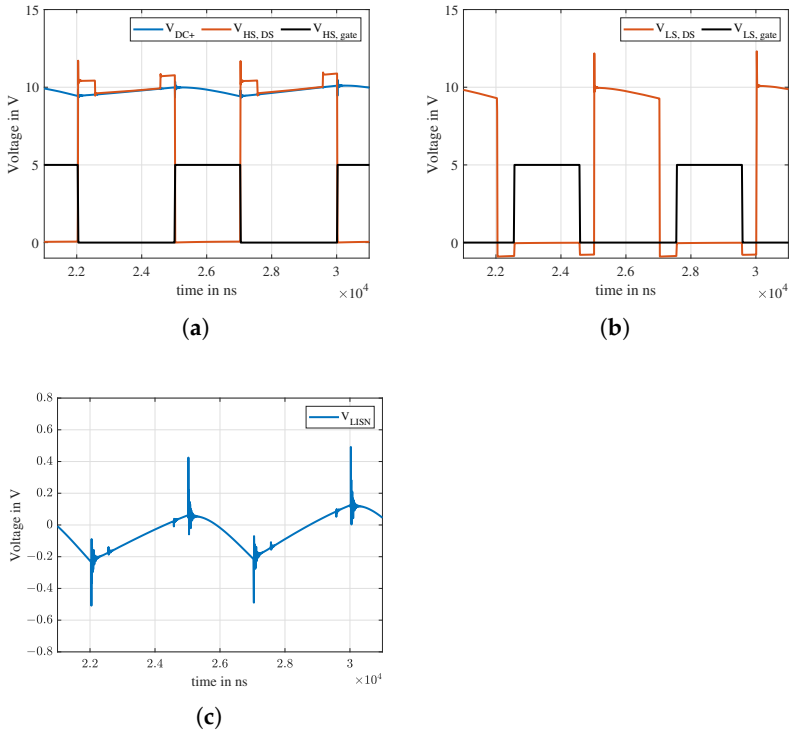


Figure 24. Simulated time domain signals of the assembly shown in Figure 15 with a supply voltage of 10 V. (**a**) High side transistor gate voltage $V_{HS,\,gate}$, drain-source voltage $V_{HS,\,DS}$, and the positive supply line voltage V_{DC+}. (**b**) Low side transistor gate voltage $V_{LS,\,gate}$ and drain-source voltage $V_{LS,\,DS}$. (**c**) LISN P output voltage.

3.8. Summary Workflow

The modeling workflow discussed above can be summarized into the following steps:

1. Import the odb++ database of the PCB into the CST Studio Suite.
   - Define material properties in the 3D model.
2. Define surface lumped elements for all external components which:
   - Are known to exhibit an accurate and reliable behavior;
   - Do not experience fast switching load currents;

   and define their electrical R, L, and C behavior.
3. Define surface lumped ports for all external components that experience fast switching load currents.
4. Run 3D FEM simulations to obtain the S-Parameters of the defined ports and export the results into a S-Parameter model (Touchstone file). The usage of a direct solver is recommended to increase computational efficiency.
5. Validate the S-Parameter model using AC simulations.
6. Generate a SPICE model from the S-Parameter model by using vector fitting and monitor the fitting error.
7. Develop a suitable equivalent circuit model of the transistors, capacitors, and LISN.
8. Characterize the load in terms of differential mode and common mode measurements and extract:
   - A simplified equivalent circuit RLC load model; or
   - A vector-fitted load model.

9. Connect models of the transistor, capacitor, LISN, and load to the vector-fitted SPICE model of the PCB and run a transient simulation with the desired supply voltage and control signals.
10. Apply a suitable EMI receiver model to the transient simulation results to obtain your conducted EMC behavior.

4. Results

Figures 25 and 26 depict the simulated and measured conducted emissions at port LISN P of the assembly shown in Section 3.6. The simulation results were obtained by using DC power supplies of 10 V and 60 V when deploying the simplified RLC load model (see Figure 22a) and the vector-fitted load model (see Figure 22b). Figure 25a,b show the simulation results for the simplified RLC load model and the transistor model with $R_p = 0\,\Omega$. As shown, the simulated conducted emissions up to 3 MHz are in good agreement with the measurement, and the error is less than 5 dB for both supply voltages. As the supply voltage increases, the conducted emissions also increase (approx. 15 dB) due to a higher current through the load. From 3–30 MHz, the simulation slightly underestimates the emissions but the difference is less than 12 dB. At 82 MHz/60 V (see Figure 25b) the emissions are significantly overestimated (approx. 18 dB). These excessive emissions are caused by the transistor model due to its current overshoots when $R_p = 0\,\Omega$ (see Figure 18). Changing the value of R_p to 10 Ω reduces these current overshoots; hence, the model can be improved at 82 MHz, as shown in Figure 25c,d (error < 12 dB). Furthermore, we would like to point out that changing the value of R_p only affects the emissions peak at 82 MHz, whereas the emissions at other frequencies do not change (compare Figure 25).

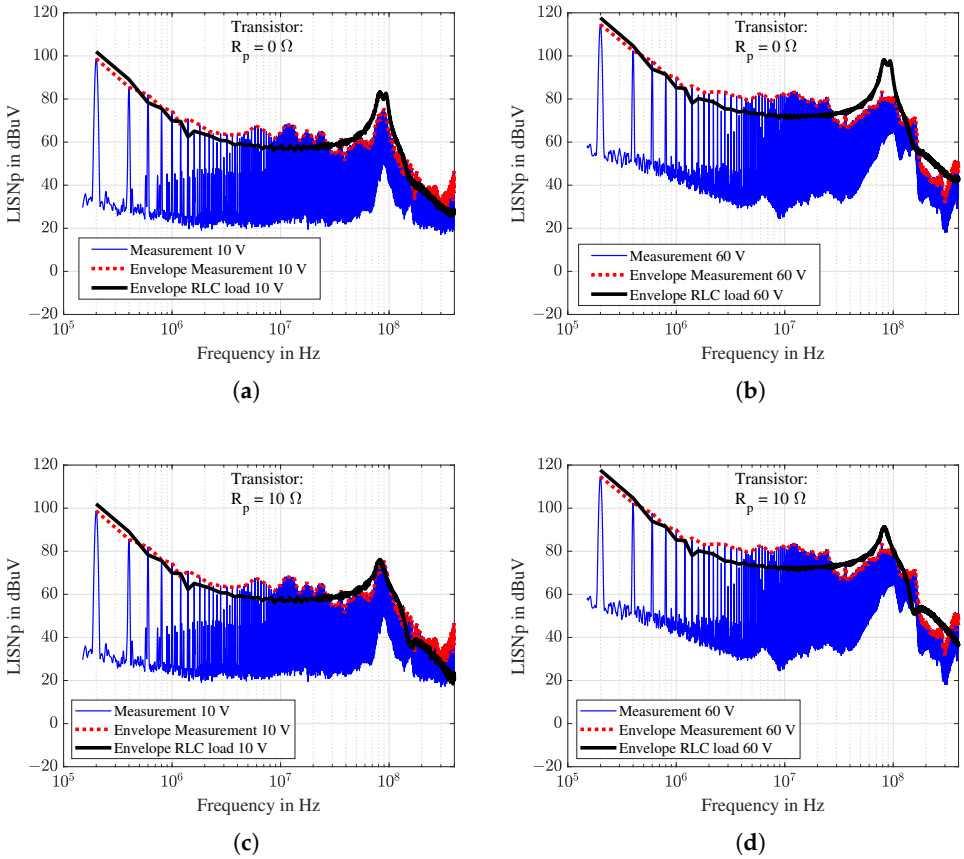


Figure 25. Comparison between measured and simulated conducted emissions with V_{DC} = 10 V and V_{DC} = 60 V. (**a**,**b**) Simplified RLC load model and $R_p = 0\,\Omega$. (**c**,**d**) Simplified RLC load model and $R_p = 10\,\Omega$.

Using the simplified RLC load model already leads to a good agreement between simulation and measurement, especially if we consider the simplicity of the load- and transistor model. The difference between simulation and measurement does not exceed 5 dB up to 3 MHz and 12 dB from 3–400 MHz, respectively. However, the accuracy can be further improved by using the discussed vector-fitted load model.

Figure 26a,b show the simulation results for the vector-fitted load model and the transistor model with R_p = 0 Ω. As shown, the accuracy of the simulated emissions from 3 MHz–60 MHz improves significantly (error < 7 dB) compared to Figure 25c,d. However, the vector-fitted load model still overestimates the emissions at 90 MHz/60 V, see Figure 26b. Changing the value of R_p to 10 Ω suppresses these excessive emissions (see Figure 26d), leading to a good agreement between simulation and measurement up to 170 MHz (error < 7 dB). For frequencies above 170 MHz, both values for R_p (0 Ω, 10 Ω) lead to an overestimation of the emissions (approx. 12 dB). This issue may be explained by the simplified transistor model using a fixed value for R_p that does not consider any voltage-dependent effects since the simulated emissions are in excellent agreement with the measurement when a DC supply voltage of 10 V is applied (see Figure 26a,c).

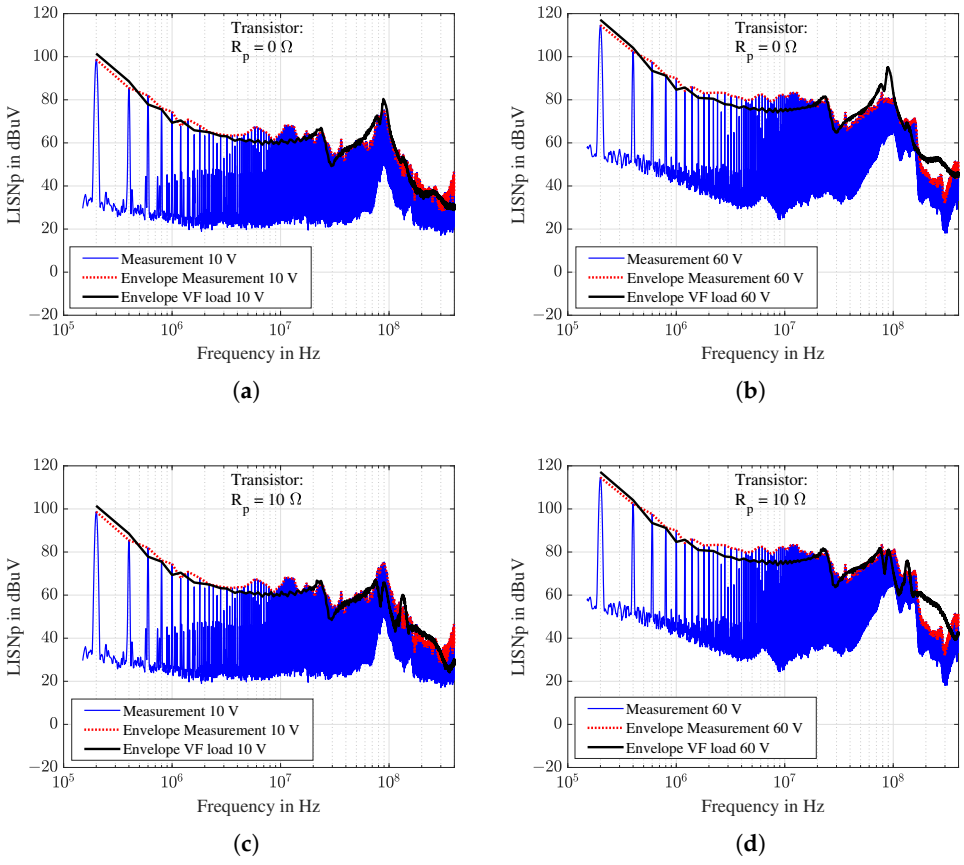


Figure 26. Comparison between measured and simulated conducted emissions with V_{DC} = 10 V and V_{DC} = 60 V. (**a**,**b**) VF load model and R_p = 0 Ω. (**c**,**d**) VF load model and R_p = 10 Ω.

5. Discussion

This paper presented a modeling workflow for simulating the conducted emissions of a power electronic system using a halfbridge circuit to switch an inductive load at its output. The methodology combines 3D FEM simulations, measurements, and SPICE circuit simulations to consider the electromagnetic parasitic effects introduced by the PCB, components, and load. It was shown that a simple equivalent circuit transistor model that only considers its output characteristic (drain-source) is suitable to approximate its conducted emission behavior up to 400 MHz with an accuracy of 12 dB. Furthermore, a

simple equivalent circuit model of the LISN network which is validated up to 150 MHz was deployed up to 400 MHz, and hardly any impact on the overall conducted emissions accuracy was observed. The obtained simulation results are in good agreement with measurements, especially if one considers the simplicity of the used transistor and load models. The presented approach does not require a physical demonstrator to fit model parameters; therefore, one may use this approach to approximate the conducted emissions of a power electronic system up to 170 MHz with an accuracy of 7 dB and above 170 MHz with an accuracy of 12 dB. Certain inaccuracies could be observed especially between 3 and 20 MHz and above 170 MHz/60 V. From 3–20 MHz, the conducted emissions are slightly underestimated (approx. 7 dB), but it is presumed that this issue arises due to measurement inaccuracies in the CM measurement. The measured CM load impedance, and hence the extracted CM load capacitance $C_{CM,\,load}$, is very sensitive to parasitics introduced by the measurement setup due to its small value (few pF). Changing the value of $C_{CM,\,load}$ also changes the simulated emissions from 3–20 MHz. Therefore, we expect a model improvement when the accuracy of the CM measurement is increased. The simulated conducted emissions above 170 MHz for a DC power supply of 60 V are overestimated by approx. 12 dB due to the simplified transistor model neglecting voltage-dependant effects.

6. Conclusions

The presented methodology approximates the conducted emissions of power electronic systems with low computational and modeling costs. Although the approach exhibits inaccuracies, especially above 170 MHz, it is still very powerful as a first estimator when there are no transistor or load models available. Above 170 MHz, the emissions decay already very fast; hence, we consider the observed model inaccuracies as tolerable. Finally, the overall accuracy of the methodology might be significantly improved if:

- The accuracy of the common mode load measurements is enhanced;
- The transistor model includes voltage-dependent effects of the drain-source resistor R_p.

These two topics are part of ongoing investigations, and we would like to point out that they can be addressed before a particular hardware prototype is available. Furthermore, models for various loads and components might be developed and stored in a library for further usage. Transistor models that are derived from their switching behavior might be improved and reused for a different hardware when similar load conditions are given. Finally, we conclude that this approach allows a true prediction of the EMC behavior of power electronic systems without specific knowledge about the device under test as simulation input.

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