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A New Nano-Scale and Energy-Optimized Reversible Digital Circuit Based on Quantum Technology

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Abstract: A nano-scale quantum-dot cellular automaton (QCA) is one of the most promising replacements for CMOS technology. Despite the potential advantages of this technology, QCA circuits are frequently plagued by numerous forms of manufacturing faults (such as a missing cell, extra cell, displacement cell, and rotated cell), making them prone to failure. As a result, in QCA technology, the design of reversible circuits has received much attention. Reversible circuits are resistant to many kinds of faults due to their inherent properties and have the possibility of data reversibility, which is important. Therefore, this research proposes a new reversible gate, followed by a new 3 × 3 reversible gate. The proposed structure does not need rotated cells and only uses one layer, increasing the design's manufacturability. QCADesigner-E and the Euler method on coherence vector (w/energy) are employed to simulate the proposed structure. The 3 × 3 reversible circuit consists of 21 cells that take up just 0.046 μm^2. Compared to the existing QCA-based single-layer reversible circuit, the proposed reversible circuit minimizes cell count, area, and delay. Furthermore, the energy consumption is studied, confirming the optimal energy consumption pattern in the proposed circuit. The proposed reversible 3 × 3 circuit dissipates average energy of 1.36 (eV) and overall energy of 1.49 (eV). Finally, the quantum cost for implementing the reversible circuits indicates a lower value than that of all the other examined circuits.

Keywords: nano-electronic; reversible logic; quantum-dot; optimization; QCADesigner-E; quantum cost

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1. Introduction

Despite the fact that people require the usage of electronic devices based on voltage, there are flaws in available digital networks and circuits based on CMOS technology [1]. Short-channel effects, short-circuit fault, and high lithography costs are a few drawbacks of this technology [2]. Electronic circuit designers try to develop alternatives such as carbon nanotube field-effect transistors, nanowires, hexagonal boron nitride (h-BN), and quantum-dot cellular automaton (QCA) [3,4]. Given the new structure offering unique measurements, QCA can compensate for the drawbacks of CMOS technology [5]. As a result, researchers focus on both hardware and software components to attain efficiency.

Electronic information and signal processing occur on every computer. The QCA processing approach is based on magnetism and uses networks of cooperating sub-micrometer magnetic dots to carry out logic operations and spread information at room temperature. The magnetization direction of the single-domain magnetic dots, which couple to their closest neighbors through magnetostatic interactions, serves as a signal for the logic states [6]. Information is transmitted via the networks by magnetic solitons, and the system's applied

oscillating magnetic field also functions as a source of energy [7]. Compared to existing microelectronic technology, these networks promise an increase in the integration density of several thousand times and a reduction in power dissipation. On the other hand, the majority and inverter gates are at the heart of QCA circuits and directly impact the system's overall efficiency [8,9]. In addition, circuits in QCA technology can be developed in two types: normal and reversible [1]. Many researchers have used QCA to study reversible logic; this means that improving the performance of reversible gates and circuits can improve the overall system efficiency [10]. Any time-reversible paradigm of computation is referred to as reversible computing. A fundamental criterion for reversibility is that mapping states to their successors must be one-to-one [11]. Quantum circuits are reversible due to quantum physics' unitarity, as long as the quantum states do not collapse [12]. Reversible circuits have received attention as components of quantum algorithms and in photonic and nano-computing technologies, where specific switching devices provide no signal gain. On the other hand, QCA technology generally offers new objects because the logic value model is based on electron placement in each cell [13,14]. CMOS's '−1' and '1' logic models are based on low and high voltages, respectively. Overall, input information is lost with irreversible logic, which might enhance power consumption. When this happens, we cannot recover it from the output information. Thus, we must recover data from the main memory. On the other side, a circuit must be made up of reversible gates to avoid energy dissipation. Additionally, reversible logic generates 1-to-1 correspondence between input and output vectors and thus decreases energy dissipation.

As a result, we offer a reversible circuit design approach based on QCA cells in this research. Only the majority gates create the outputs of the proposed reversible circuits. The three main constraints in reversible computing are limiting input constants, employing the smallest number of gates, and minimizing the quantum cost. The QCADesigner-E program was used to model the proposed building. In terms of the number of cells, operations, and quantum cost, it also outperforms prior architectures. In summary, the original contributions of this paper are:

- Proposing a new reversible block in QCA technology;
- Simulating the proposed block using the QCADesigner-E tool; and
- Calculating some parameters, such as the number of constant inputs, garbage outputs, latency, and quantum cost, and comparing to current designs.

This paper contains the following. Section 2 provides background information on QCA technology. Section 3 proposes new designs. Section 4 provides simulation results and compares the proposed designs to other available designs. Finally, Section 5 concludes this paper.

2. Basic Concepts and Related Works

2.1. QCA Cell and Wire

Recently, nano-designs and nano-circuits have received much attention in a wide range of applications. The basic building block of every QCA design is the cells. The logic state of a QCA cell is stored based on the electron location. There are four quantum-dots in each cell [15]. Between the quantum-dots, there is a tunneling junction. Quantum-dots are occupied by electrons tunneling to them [16]. Because of the Coulombic repulsion, these electrons occupy sites in a cell and are diagonal to one another. Figure 1a shows that a QCA cell has two polarization states that correspond to the values '0' and '1'. A QCA wire is a collection of cells arranged in the shape of an array [15]. Figure 1b shows how data are transferred between QCA wires owing to the Coulombic interaction between cells.

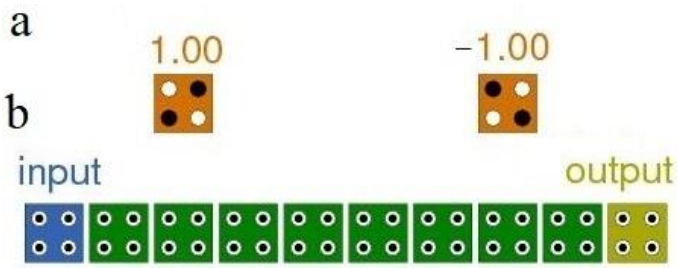

Figure 1. (**a**) QCA cell and (**b**) wire.

2.2. Majority and Inverter Gates

The majority gate is the most fundamental gate in QCA. Figure 2a shows the fundamental structure of the majority gate using the QCA cell. Five QCA cells are utilized in a majority gate with three inputs, one output, and one driving cell to create a majority voter function for M (X, Y, Z) = XY + YZ + XZ. By permanently setting the input of one cell to '0' or '1', the majority gate can serve as an AND or an OR gate [17]. One of the other essential gate components of a higher degree of QCA design is the inverter gate. Figure 2b depicts the QCA arrangement of the inverter gate [18]. The inverter is a key component in the majority of logical operations. It signifies the output cell's polarization, which is the polar opposite of the input cell.

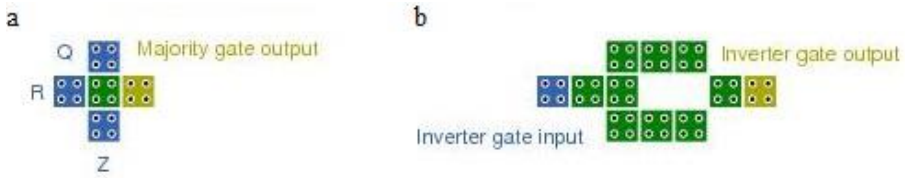

Figure 2. (**a**) Majority gate and (**b**) inverter gate in QCA technology.

2.3. QCA Clocking

The clock controls the movement of electrons in cells in QCA circuits. The cycle of the clock is classified into four sections:

- Switch: The cell exits non-polar mode and gradually approaches the input value of the cell before it.
- Hold: During this phase, the cell's energy level is high, the cell is active, and it can act as an input for the following cell.
- Release: The cell's energy level gradually drops such that it does not affect its neighbors.
- Relax: The cell loses energy and enters a state of relaxation.

2.4. QCA Faults

A missing cell (Figure 3a), extra cell (Figure 3b), displacement cell (Figure 3c), and rotated cell (Figure 3d) are some of the issues in QCA technology. One or more cells can be eliminated in the case of a missing cell. Multiple cells can be added to the circuit in some circumstances in the case of an extra cell. The situation of a cell being moved from its appropriate position is referred to as cell dislocation. A defect in which a faulty cell is rotated is known as a rotated cell [19].

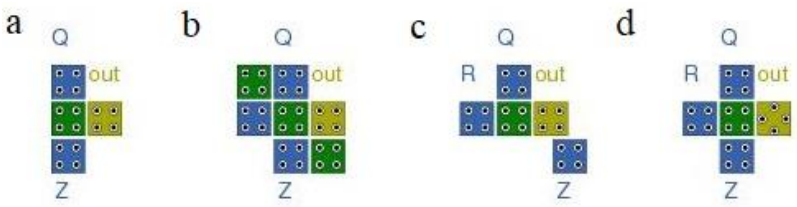

Figure 3. QCA faults; (**a**) missing cell, (**b**) extra cell, (**c**) dislocation cell, (**d**) rotated cell.

2.5. Reversible QCA

There are more than a billion computers in use globally, and they consume more energy than ever. The power consumption of several computer components, including memory and the CPU, can be reduced by using reversible functions. A computer process must break the calculation into manageable pieces in order to run. When we have reversible hardware, no result is lost since sometimes each portion needs the previous parts or other process outcomes to finish. Therefore, there is no need to fetch data from the main memory. For instance, middle registers do not need to store the results of previous computations when a CPU based on reversible hardware executes instructions; this reduces a device's energy usage and overall calculation time. To further assist computer designers, this study presents a novel and incredibly effective way of generating crucial reversible features.

2.6. Related Works

Logical reversibility refers to the ability to compute the output from the input and vice versa. Reversible gates and circuits have the same number of outputs as they simply create the outputs. An inverter gate, for example, is conceptually reversible. Depending on how the inverter gate is implemented, it may or may not be physically reversible. In addition to the inverter gate, many circuits and gates are built for reversible logic, the most important of which are discussed in this section. However, due to the quick access to inputs and outputs, a small number of cells, a small area, and short clock phases are all critical in QCA technology, and it is urgently required to build circuits with these features. In this section, we review some essential papers in this area.

Bagherian Khosroshahy, Abdoli [20] proposed a reversible and fault-tolerant parity-based arithmetic circuit for nano-communications. The nano-communication includes one parity checker gate and one parity generating gate. QCADesigner software was used to simulate their proposed structures. Their structure has only two trash outputs and no rotating cells, and it has only one layer, which enhances the design's manufacturability.

Seyedi, Otsuki [21] presented an optimized reversible double Feynman gate that employed efficient arithmetic elements as essential structural elements also used in this study. They also employed a basic modeling approach to make it more consistent and noise-resistant. Furthermore, they compared the proposed model to earlier models in terms of complexity, timing, cell count, and latency. They also used QCADesigner to keep track of the suggested gate's shape and performance. Even though this design is faster and has a low area, it requires many consumed cells.

Sasamal, Singh [22] proposed low-energy and area-efficient QCA-based reversible logic gates. The suggested schematizations were more efficient after incorporating a small two-input XOR gate. They used traditional criteria to assess the efficacy of the proposed schematizations and previous related ones. Simulating the proposed structures was realized with QCADesigner software. This design has a low speed and large cell consumption; however, low cell consumption and high speed are critical in nano-circuit design.

Singh and Sharma [23] proposed a robust reversible gate with enhanced efficiency to perform QCA-based RAM schematization. In the constraints of the traditional RAM architecture, RAM cell schematization using a combination of QCA technology and reversible logic will excel. The suggested 33 reversible gate's QCA configuration has been schematized with the use of a unique multiplexer circuit. By looking at the proposed circuit more closely, it can be seen that it has a large consumption area and a high number of cells, making it hard to utilize in the other reversible circuits. In addition, the gate's standard cost function, Boolean functions, and energy loss have all been investigated.

Using QCA technology, Bahar, Waheed [24] developed two new approaches for schematizing the double Feynman gate. With the help of the QCADesigner, these recommended circuits were simulated. These designs were also evaluated in terms of area and complexity (cell count). The utilization of a high number of cells and large consumption area are both clear downsides of these designs.

3. The Proposed Designs in This Study

In a digital system, a reversible function can reduce power consumption in several components such as memory, ALU, and CPU. Data loss in reversible hardware cannot happen. As a result, retrieving data from the main memory is not required, and it reduces the device's energy usage and total calculation time. This study presents the design of reversible circuits for constructing basic reversible arithmetic parts. Figure 4 shows an ideal QCA schematization for the 3 × 3 reversible circuit, using different cell colors to determine the QCA architecture and QCA hardware implementation of this circuit. The governing Boolean equations for the 3 × 3 reversible circuit are represented by Equations (1)–(3):

$$P = A \tag{1}$$

$$R = (A \; XOR \; B) \tag{2}$$

$$Q = (A \; XOR \; C) \tag{3}$$

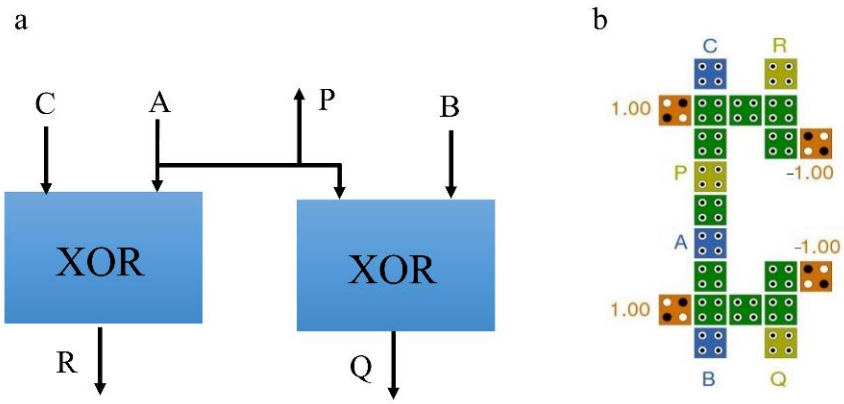

Figure 4. (**a**) The schematic of the proposed 3 × 3 reversible circuit, (**b**) The QCA layout of the proposed 3 × 3 reversible circuit.

Output *P* does not require an extra gate in this design. Unlike the previous layouts, the proposed design for the 3 × 3 reversible circuit uses three-input majority gates. In this circuit, the three outputs are *P*, *Q*, and *R*, and the three inputs are *A*, *B*, and *C*. One output is identical to one input in the 3 × 3 reversible circuit, while the other outputs are the XOR function of the inputs. The three inputs can be combined in eight different ways, and the outputs vary depending on the input combinations. The proposed 3 × 3 reversible circuit topology is more productive, with a cell count of 21 cells and a clock delay of 0.25 clock phases.

Additionally, an *AND* gate was explored for the two inputs *A* and *C* and an *OR* gate was investigated for the two inputs *A* and B, and the output *P* was reversed using an inverter gate to demonstrate the expandability of the presented circuit. The output of the *AND* gate and the output *OR* gate both output after the 0.25 clock phase. The design and hardware implementation of this circuit are illustrated in Figure 5, and it is evident that this circuit generates the final output following a complete clock phase cycle. Although this approach is executed in one layer, access to inputs and outputs is convenient and simple. Additionally, the proposed tested reversible circuit is more productive, with a cell count of 63 cells and a clock delay of 1 (4/4) clock phase. The governing Boolean equations for the test circuit are represented by Equations (4)–(6):

$$PP = P' \tag{4}$$

$$AB = (A \; OR \; B) \tag{5}$$

$$AC = (A \; AND \; C) \tag{6}$$

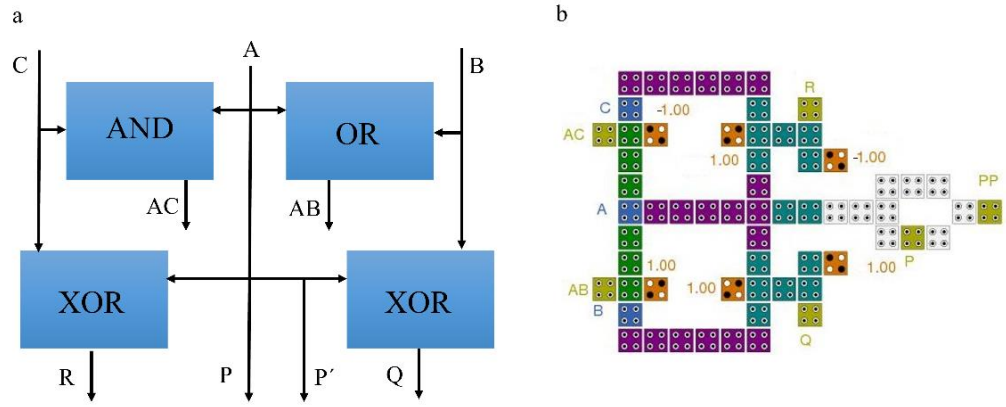

Figure 5. (**a**) The schematic of a reversible test circuit, (**b**) The QCA layout of a reversible test circuit.

4. Simulation Tools, Parameters, and Results

QCADesigner-E software was used to model the QCA circuits presented in this paper. QCADesigner-E is the most popular software for circuit simulation using QCA technology [25]. This tool simulates the circuits using two simulation engines: 'Bistable Approximation' and 'Coherence Vector'. Both have been used, and the results are nearly identical [25–28]. Energy in QCA cells is treated as a 'bath' of energy in QCADesigner-E or QDE's energy estimating tool. It is a method for estimating energy based on coordinates. If the energy of a QCA cell is EIO, it is written as EIO = EIN − EOUT, with EIN and EOUT representing the input and output energies, respectively.

Accuracy Analysis and Comparisons

In contrast, Figure 6 shows the simulation results for the total integration of *A*, *B*, and *C* inputs for a 3 × 3 reversible circuit. According to the figure, it can be seen that all possible inputs have been applied to the circuit, and the circuit has produced the correct and appropriate amount of output for all input modes after 0.25 clock phases. Finally, Figure 7 displays the simulation outcomes for the reversible test circuit. The figure shows that all possible inputs have been applied to the circuit, and the circuit has produced the right and appropriate amount of outputs for all input modes. Energy dissipation would not happen if computations were performed reversibly, as the quantity of energy wasted in a system is directly proportional to the number of bits erased during computing, as shown by the outputs and simulation findings. According to the simulation results, reversible circuits do not lose information. Only when the circuit contains reversible gates can the reversible computation be conducted. These circuits may create unique output vectors from each input vector and vice versa, implying that input and output vectors have a one-to-one mapping. Identifying every input or output in these circuits is simple based on its assigned counterpart. Simulation results confirm that the reversible circuits operate well and designate relevant production. All waveforms received from outputs in Figure 6 are produced at the 0.25 clock phase in both circuits. This design is coplanar, and the intended outputs are collected from the coplanar layer.

Researchers use the QCADesigner-E tool in QCA technology to assess energy dissipation. As a result, the proposed reversible circuits' energy dissipation is calculated using the QCADesigner-E. The average and total energy dissipation of the reversible circuits and previous circuits provided by other researchers in QCA technology, which are formed using typical gates and cells and feature reversible qualities, are depicted in Figure 8. After designing the circuits inside the software and applying all the inputs and specifying all the outputs, the software calculates these items and generates the output values to calculate the average and total energy dissipation. According to the results, it can be seen that the proposed circuits in this study have the lowest value of the average and total energy dissipation (see the bottom of Figure 8).

Table 1 shows the analysis results for the proposed reversible circuit and earlier designs. It compares previous works to the proposed reversible circuit in terms of area, cell count, latency, and quantum cost. Compared to previous designs, the suggested QCA 3 × 3 reversible circuit and reversible odd-parity generator offer considerable improvements in layout complexity (cell count), effective area, and clock latency.

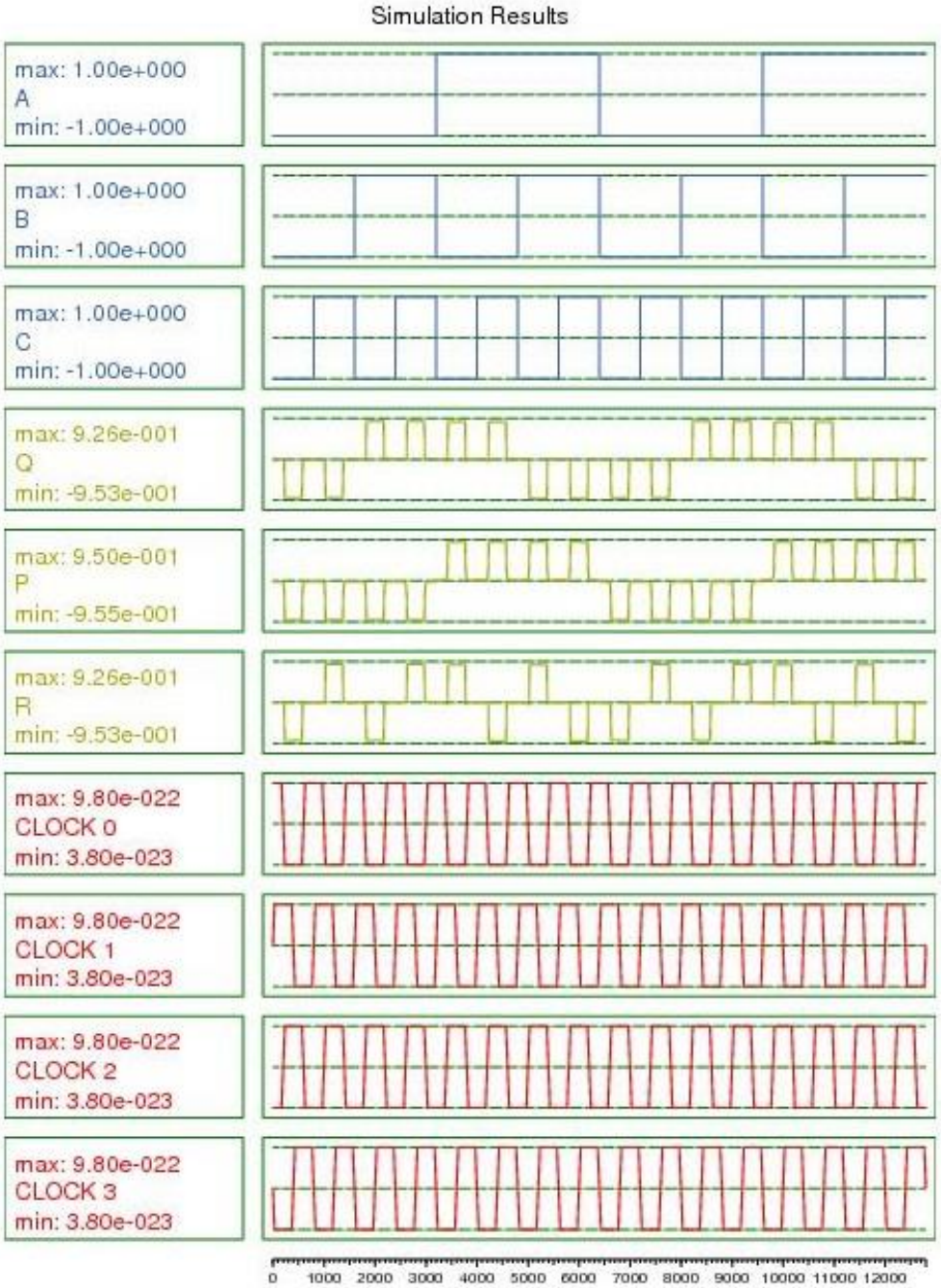

Figure 6. The proposed 3 × 3 reversible circuit simulation results.

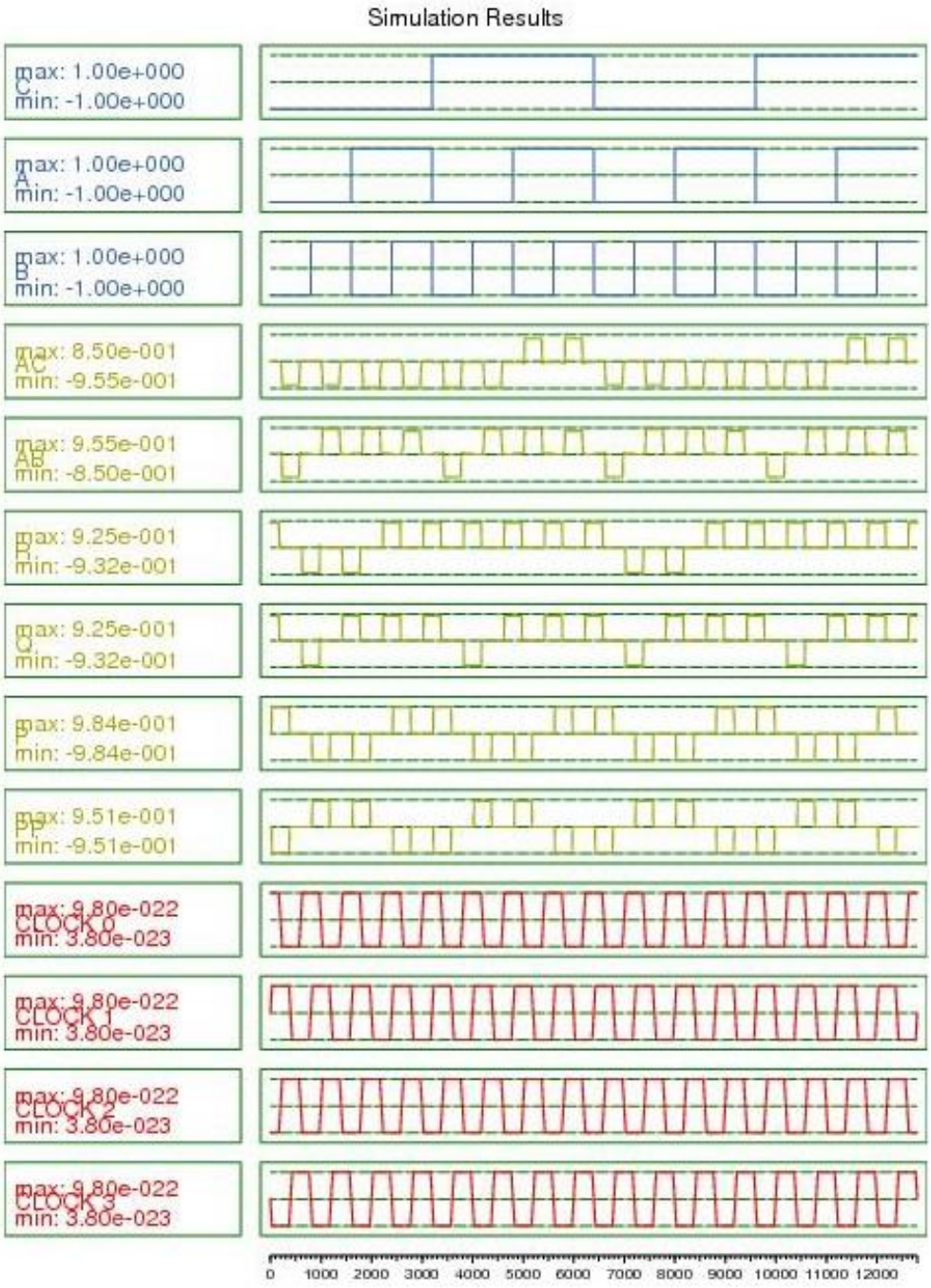

Figure 7. The proposed reversible test circuit simulation results.

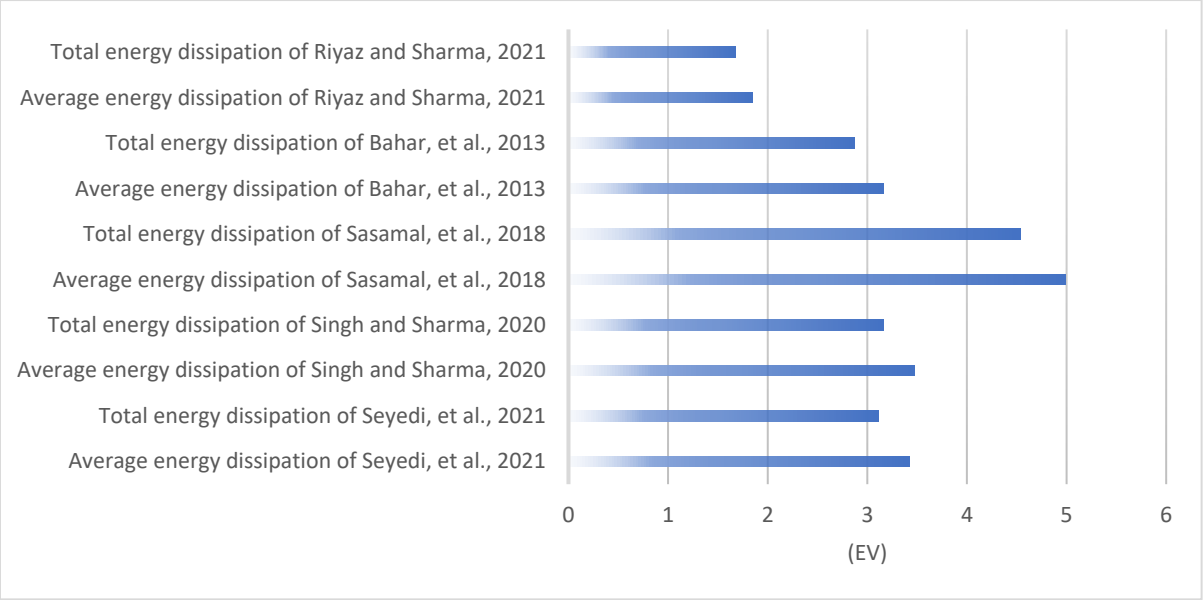

Figure 8. Energy dissipation of the proposed circuit [21–24,29].

Table 1. Comparison of the proposed and literature layouts.

	Designs	Area (μm^2)	Cells	Delay	Quantum Cost (Area × Delay^2)
3 × 3 reversible circuit	Proposed layout in this study	0.046 μm^2	21	0.25	0.0025
	Seyedi, Otsuki [21]	0.05 μm^2	46	0.5	0.0125
	Singh and Sharma [23]	0.05 μm^2	53	0.75	0. 028125
	Sasamal, Singh [22]	0.05 μm^2	40	0.5	0.0125
	Bahar, Waheed [24] (1)	0.06 μm^2	51	0.5	0.015
	Bahar, Waheed [24] (2)	0.09 μm^2	96	0.75	0.050625
	Riyaz and Sharma [29]	0.02 μm^2	27	0.25	0.005

5. Conclusions and Future Work

QCA technology is one of the unique types of nanotechnologies that have replaced CMOS due to its better speed and area capabilities. This research proposed a new and optimal structure for a 3 × 3 reversible circuit. The 3 × 3 reversible circuit generates the Q, R, and P signals after the 0.25 clock cycle. The results were acquired using QCADesigner-E. In QCA, our proposed reversible structure for the 3 × 3 reversible circuit was made up of 21 cells that take up only 0.046 μm^2. The coplanar QCA method was used in the described reversible circuit's construction. As a result, our modern schematizations revealed significant advancements in QCA area, intricacy, and clock postponement in terms of the obtainable layouts completed using distinct clock designs. The proposed circuits outperformed other circuits in terms of area, cell count, latency, and quantum cost. The energy dissipation in circuits has also been calculated; the proposed reversible 3 × 3 circuit dissipates average energy of 1.36 (eV) and 1.49 (eV) overall. The proposed reversible circuits could be used as a future primary block in complex circuits. It can also be used as a stunning building block for larger units in the future to create a reversible circuit. We can use this design to create a 1:n reversible circuit and 4-bit, 8-bit, and 16-bit parity generators in the future. Furthermore, the proposed circuit can organize more complex and high-performance fault-tolerant nano-scale circuits in the future.

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