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A High-Gain Multiphase Interleaved Differential Capacitor Clamped Boost Converter

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Abstract: A step-up for a non-isolated interleaved differential capacitor clamped boost (IDCCB) DC–DC converter is proposed in this manuscript. Because of its ability to produce high voltage gains, it is used in high-power applications. This converter's modelling and control design are applicable to any number of phases. A six-phase interleaved differential capacitor clamped boost prototype is tested in this work, with an input voltage of 60 V, an output voltage of 360 V, and a nominal output power of 2.2 kW. The components of the converter are placed and controlled in such a way that the output voltage is the sum of the two capacitor voltages and the input voltage, which is two times higher than the supply voltage when compared to a conventional interleaved differential dual-boost converter. This converter reduces the stress on the capacitor with reference to the conventional interleaved differential boost converter for the same conversion gain. This prototype is considered and the developed approach is applied, after which the experimental results are obtained. This converter has potential for application in areas such as renewable energy conversion and electric vehicles.

Keywords: capacitor clamped converter; high-gain converter; DC–DC power converter

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1. Introduction

New challenges in energy conversion technology are being faced due to the increased use of renewable energy sources. One such challenge is that several types of devices that store or produce electrical energy, such as ultra-capacitors, solar panels, batteries, and fuel cells, are manufactured using low-voltage cells, which must be series-connected to attain reasonable voltages [1–3]. In such cases, the complexity of the system is increased due to the series connection of a large number of cells, which reduces the performance due to the differences among the cells, such as fabrication variations and other various working conditions. Moreover, the notable variations in the output voltages of this kind of electrical energy source depend on factors such as the state of charge, the output current, and the solar radiation [4].

Using comparatively high and stable voltages in typical applications such as in electrical motor drives, power infusion into the grid is essential at times. For this, a step-up converter is used to increase the voltage of the source based on the requirements of the application and to produce a stable output voltage, even if variations exist in the voltages of the source [5–8]. For instance, let us contemplate the electronic circuits in a Toyota Prius.

The battery pack is developed at 206.1 V and the peak value of the DC link inverter is 500 V, as shown in Figure 1. Here, the conventional buck–boost type bidirectional DC–DC converter can be utilised to amplify and modulate the DC link. These BDCs are broadly classified as isolated (transformer-based) converters and non-isolated (transformerless) converters. Conventional isolated converters are utilised to meet the high gain needs of EVs, providing flexibility in the design of EVs by allowing for lower operating voltages at the battery side. Step-up isolated converters such as flyback, push–pull, current-fed half-bridge, and current-fed full-bridge topologies are chosen for this purpose, along with a sufficient transformer turn ratio. However, this approach suffers from huge voltage spikes caused by the transformer's leakage inductance, resulting in power loss in the switch. Thus, non-isolated BDCs [9–25] are chosen over isolated BDCs due to their various advantages, such as their higher efficiency, greater reliability, and lower component count, which leads to a smaller size and lower overall cost [5,6]. In general, a high duty cycle is used to achieve high gain in transformerless converters. However, the growing costs reverse the recovery losses and decrease efficiency. Furthermore, the reliability of the switches is harmed as a result of the high voltage stress caused by the high duty ratio. To address these concerns, other converter topologies have been proposed in the literature, including coupled inductors in typical boost topologies [11–14], cascading converters [15] and interleaved topologies [9,10,16,17] to alleviate voltage spikes. Coupled inductor (CI)-based topologies have received the most attention as they can achieve high conversion gains due to their compactness and high power density in both charging and discharging modes [18–22]. However, there are several issues with CI–BDC converters, such as energy leakage from the connected inductor, which causes voltage stress during the turn-off process, in addition to the complexity of the circuit design. On the other hand, the cascading of converters increases the component count, enlarges the size, and decreases the efficiency [23–26]. Hence, to address the abovementioned issues, the interleaving concept is adopted in this manuscript to derive new types of converters, as this approach can also alleviate the drawbacks of both isolated and non-isolated BDCs, such as the voltage stress, high voltage diversity factor with large duty cycles, and high costs.

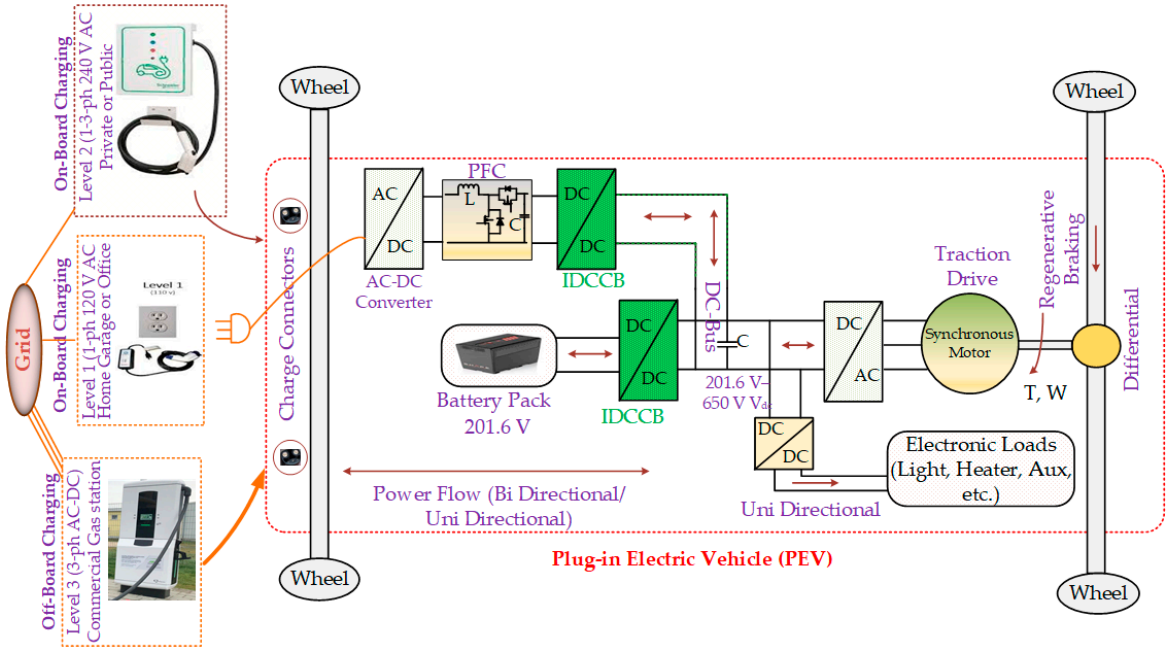

Figure 1. Architecture of a plug-in electric vehicle.

With the aim of achieving higher voltage gain than with a conventional boost converter, the alternative topology (interleaved double dual-boost (IDDB) converter [16,17]) is proposed and discussed in this paper. The phase interleaving feature enables the usage

of the converter for high-power applications, which is why this topology is chosen over others with high-gain properties [9–25]. This converter has applications in areas such as renewable energy conversion, microgrids, and electric vehicles [26–28]. The components of the converter are placed and controlled in such a way that the output voltage is the sum of the two capacitor voltages and the input voltage, which is two times higher than the supply voltage when compared to the conventional interleaved differential dual-boost converter. This converter reduces the stress on the capacitor with reference to the conventional interleaved differential boost converter for the same conversion gain. In this topology, one can step the voltage down to a lower level than the output voltage so as to utilise the smaller values of the components (switches and capacitors). The multiphase IDCCB's linearised dynamic model and the parameter dispersion problem are being presented in this paper. The results show that this model is distinct from the conventional interleaved boost model. To better estimate the system behaviour, the reduced-order model is used.

2. Modelling of the Two-Phase Converter

2.1. Topology

Figure 2 shows the dual-phase IDCCB. Here, V_{in} is the input voltage and R is the load resistor. Both the phases of this converter consist of an inductor and two semiconductor switches. Phase 1 is composed of inductor L_1, and devices S_1, D_1 and S_2, D_2. Here, phase 1 and capacitor C_1 are together named as "module 1", and likewise phase 2 and capacitor C_2 are together named as "module 2". The inductor (ESR) equivalent series resistance and the ESR of the switches are represented by the resistors r_{L1} and r_{L2}, respectively. Bidirectional power flow is required in systems where energy storage systems such as the batteries and ultra-capacitors are involved, which is facilitated by this converter, with which all the switches are individually implemented using a transistor with an anti-parallel diode. The terminal load (i.e., output voltage), V_0, is given by:

$$V_0 = V_1 + V_2 - V_{in} \tag{1}$$

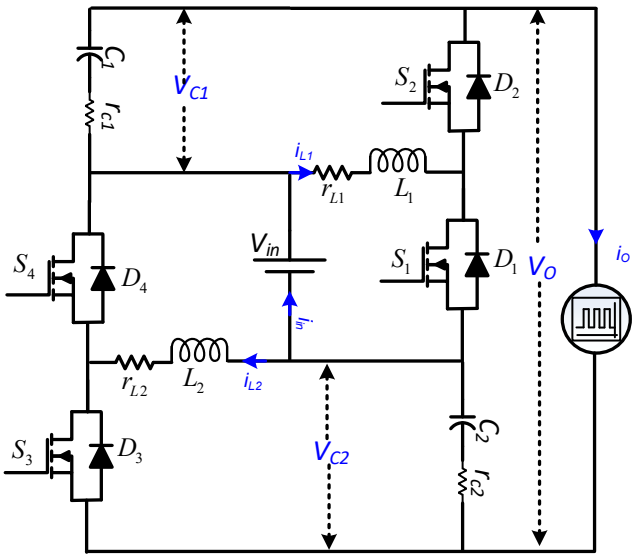

Figure 2. Interleaved differential capacitor clamped boost converter.

By neglecting the losses in the converter, $r_{L1} = r_{L2} = 0$. Let us propose a hypothesis that states that with the continuous conduction mode (CCM) operation of the phases with equivalent duty (δ), the converter's static gain is given as:

$$\frac{V_0}{V_{in}} = \frac{1+\delta}{1-\delta} \tag{2}$$

The current supplied by the source V_{in} (i.e., converter's input current) is given as

$$i_{in} = i_1 + i_2 - i_0 \tag{3}$$

Here, $i_0 = V_0/R$, which is the converter's output current.

2.2. Reduced-Order Mathematical Model of IDCCB

Figure 3 shows the two-phase interleaved differential capacitor clamped boost converter with ideal switching devices. Here, the duty ratio δ_i of the switch is S_i. This explanation shows that the duty ratio relates to lower side switch S_1 conduction. For switch S_2, this relates to the conduction of the upper side device.

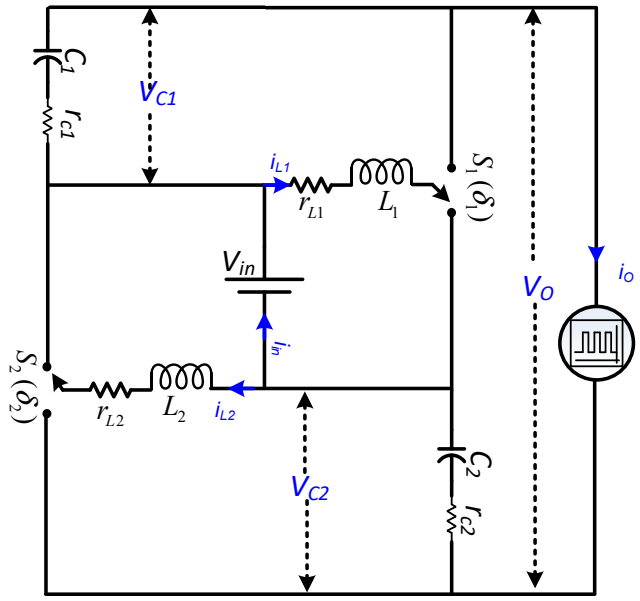

Figure 3. Interleaved capacitor clamped boost converter.

The converter's state space model is given as:

$$\dot{x} = Ax + Bu \tag{4}$$

With consideration of the dual-phase IDDBC, the system is of the fourth order. State vector x_2 is given as in Equation (5).

$$x_{2\_ph} = \begin{bmatrix} I_1 & V_1 & I_2 & V_2 \end{bmatrix}' \tag{5}$$

Note: The mean variable values are represented by the capital letters.
The system, which has single input, is defined as:

$$u = [V_{in}] \tag{6}$$

By applying the state space averaging technique [2], apart from using expression $\overline{\delta}_i = (1 - \delta_i)$, the average system matrix is given by:

$$A_{2\_ph} = \begin{bmatrix} -\frac{(r_{L1}+r_{on})}{L_1} - \overline{\delta}_1(r_x r_{c1}) & -\overline{\delta}_1 r_x & 0 & 0 \\ -\overline{\delta}_1 \frac{r_x}{R} & -\overline{\delta}_1 r_x & 0 & -\overline{\delta}_1 \frac{r_x}{R} \\ 0 & 0 & -\frac{(r_{L2}+r_{on})}{L_2} - \overline{\delta}_2(r_x r_{c2}) & -\overline{\delta}_2 r_x \\ 0 & -\overline{\delta}_2 \frac{r_x}{R} & -\overline{\delta}_2 r_x & -\overline{\delta}_2 \frac{r_x}{R} \end{bmatrix} \tag{7}$$

Here, $r_x = \frac{R}{R+r_{c1}+r_{c2}}$.

The input matrix is:

$$B_{2\_ph} = \begin{bmatrix} \frac{1}{L_1} & \frac{r_x}{RC_1} & \frac{1}{L_2} & \frac{r_x}{RC_2} \end{bmatrix} \tag{8}$$

Now, let us consider that there is perfect symmetry among the phases:

$$L_1 = L_2 = L \tag{9}$$

$$r_{L1} = r_{L2} = r_L \tag{10}$$

and

$$C_1 = C_2 = C \tag{11}$$

The viability of the approximations in (9)–(11) is studied in Section 5. Additionally, the same voltage reference is utilised for the voltage of the two load-side capacitors, which results in:

$$V_1 = V_2 = V \tag{12}$$

With the consideration of the condition in (12), the system matrix is given as:

$$A_{2\_ph} = \begin{bmatrix} -\frac{(r_L+r_{on})}{L} - \overline{\delta}_1(r_x r_c) & -\overline{\delta}_1 r_x & 0 & 0 \\ -\overline{\delta}_1 \frac{r_x}{R} & -\overline{\delta}_1 r_x & 0 & -\overline{\delta}_1 \frac{r_x}{R} \\ 0 & 0 & -\frac{(r_L+r_{on})}{L} - \overline{\delta}_2(r_x r_c) & -\overline{\delta}_2 r_x \\ 0 & -\overline{\delta}_2 \frac{r_x}{R} & -\overline{\delta}_2 r_x & -\overline{\delta}_2 \frac{r_x}{R} \end{bmatrix} \tag{13}$$

Here, $r_x = \frac{R}{R+2r_c}$.

In order to meet the aim of effective control design for the proposed converter, the overall system can be decomposed into two independent second-order systems for the two modules. The following state vector is present in the first module:

$$x'_{2\_ph} = \begin{bmatrix} I & V \end{bmatrix}' \tag{14}$$

The reduced-order state and input matrices can be written as:

$$A_{2\_ph} = \begin{pmatrix} -\frac{(r_L+r_{on})}{L} - \overline{\delta}_1\left(\frac{Rr_c}{R+2r_c}\right) & -\overline{\delta}_1 \frac{R}{R+2r_c} \\ -\overline{\delta}_1 \frac{R}{R+2r_c} & -\overline{\delta}_1 \frac{1}{R+2r_c} \end{pmatrix} B_{2\_ph} = \begin{bmatrix} \frac{1}{L} \\ \frac{1}{(2r_c+R)C} \end{bmatrix} \tag{15}$$

The dynamic mathematic model per phase current and the corresponding module voltage are represented by this reduced-order system, with a hypothesis that states that the other module and phase act supplementary. The equivalent duty ratio is represented by δ, which is the same for both phases.

In this model, one has to be worried about the voltages in the capacitors C_1 and C_2 but not with the output voltage directly. However, the load voltage of this configuration depends on the module voltages and source voltage, using (1). The variation in input voltages changes the load voltage, which is secured with adjustments of the capacitor voltage, which in turn requires measurement of the input voltage. An imbalance of the voltages (V_1 and V_2) is created when one tries to control the output voltage (directly), causing the converter symmetry to break.

3. Modelling of the *N*-Phase Converter

This topology is not only used for two phases, but can also be used for more than two phases. However, here we use an even number of phases to maintain the symmetry of the converter. Let us spread the modelling of the dual-phase converter to the generalised *N*-phase converter in this section.

"Module 1" comprises the capacitor C_1 and the grouping of phases that are linked to it (capacitor C_1). Similarly, "module 2" comprises the capacitor C_2 and the grouping of phases that are linked to it (capacitor C_2). Figure 4 shows the six-phase IDCCB converter as a paradigm of the converter, which has a large number of phases. Both Equations (1)

and (2) are independent of the number of phases. Therefore, the source current can be calculated as:

$$i_{in} = i_1 + i_2 + \ldots + i_N - i_o \tag{16}$$

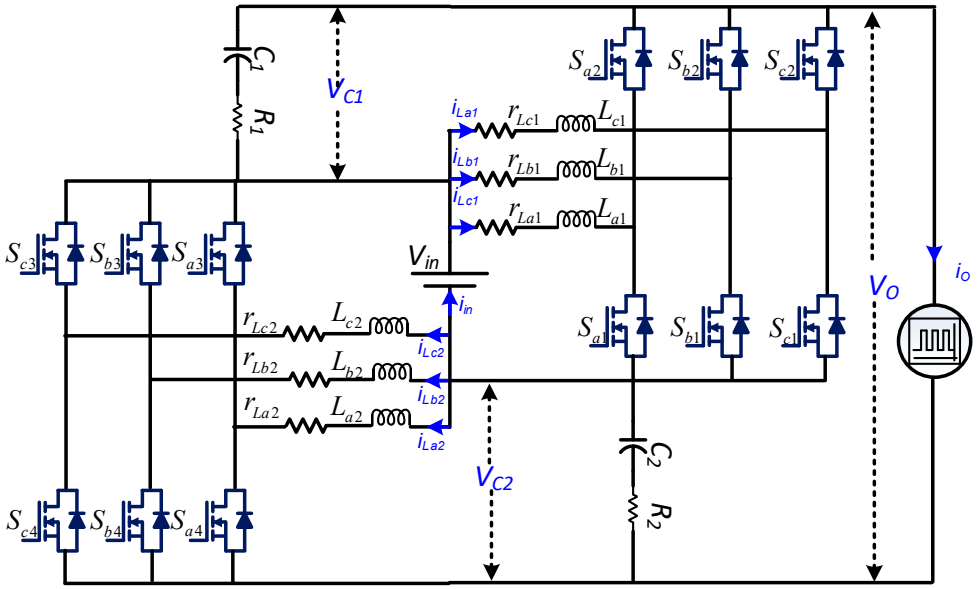

Figure 4. Multiphase IMPCCB.

Here, there are N states for currents in the inductor and 2 states for voltages across the capacitor; hence, the N-phase IDCCB has $N + 2$ state variables.

For both halves of the N inductors of module 1, the differential equation of the current is:

$$\frac{d}{dt} I_k = \frac{1}{L_k}(-(r_{Lk} + r_{on}) I_k - (i_{c1} r_{c1} + V_1)\bar{\delta}_k + \delta_k V_{in}) \tag{17}$$

where $k = 1, \ldots, N/2$.

In both halves of N inductors of module 2, the differential expression of the current is:

$$\frac{d}{dt} I_k = \frac{1}{L_k}(-(r_{Lk} + r_{on}) I_k - (i_{c2} r_{c2} + V_2)\bar{\delta}_k + \delta_k V_{in}) \tag{18}$$

For $k = N/2 + 1, \ldots .., N$.

In C_1, the differential expression of the capacitor voltage is:

$$\frac{d}{dt} V_1 = \frac{1}{C_1}\left[\left(\sum_{k=1}^{N/2} I_k \bar{\delta}_k\right) + \frac{-i_{c1} r_{c1} - i_{c2} r_{c2} - V_1 - V_2 + V_{in}}{R}\right] \tag{19}$$

In C_2, the differential expression of the voltage is:

$$\frac{d}{dt} V_2 = \frac{1}{C_2}\left[\left(\sum_{k=\frac{N}{2}+1}^{N} I_k \bar{\delta}_k\right) + \frac{-i_{c1} r_{c1} - i_{c2} r_{c2} - V_1 - V_2 + V_{in}}{R}\right] \tag{20}$$

Here, to reduce the order of the system, we need to explore the symmetry of the system identically to the process for the dual-phase IDCCB converter model. Let us assume that:

$$L_1 = L_2 = \cdots = L_N = L \tag{21}$$

$$r_{L1} = r_{L2} = \cdots = r_{LN} = r_L \tag{22}$$

and:

$$C_1 = C_2 = C \tag{23}$$

The viability of the approximations in (21)–(23) is studied in Section 5. The same voltage reference is used for V_1 and V_2. Additionally, the controller, alongside the converter symmetry, will lead to the expression:

$$V_1 = V_2 = V \tag{24}$$

Additionally, the current in every phase is the same, which can be shown by using the same reference currents for every module:

$$I_1 = I_2 = \cdots = I_N = I \tag{25}$$

For all the phases, the duty ratio is equivalent:

$$\delta_1 = \delta_2 = \cdots = \delta_N = \delta \tag{26}$$

Expressions (17) and (18) can be combined as:

$$\frac{d}{dt}I = \frac{1}{L}(-(r_L + r_{on})I - (i_c r_c + V)\bar{\delta} + V_{in}) \tag{27}$$

Equations (19) and (20) are written as:

$$\frac{d}{dt}V = \frac{1}{C}\left[\frac{N\bar{\delta}I}{2} + \frac{-2(V + i_c r_c) + V_{in}}{R}\right] \tag{28}$$

The state vector in the state-space representation is:

$$x = \begin{bmatrix} I & V \end{bmatrix}' \tag{29}$$

The state matrix and corresponding input matrices can be obtained as:

$$A = \begin{pmatrix} -\frac{(r_L+r_{on})}{L} - \bar{\delta}_1\left(\frac{Rr_c}{R+2r_c}\right)\frac{N}{2} & -\bar{\delta}_1\frac{R}{R+2r_c} \\ -\bar{\delta}_1\frac{R}{R+2r_c}\frac{N}{2} & -\bar{\delta}_1\frac{1}{R+2r_c}\frac{N}{2} \end{pmatrix} B = \begin{bmatrix} \frac{1}{L} \\ \frac{1}{(2r_c+R)C} \end{bmatrix} \tag{30}$$

It is quite fascinating to compare the results obtained with those of the conventional N-phase IDDB converter [3]. With consideration of similar assumptions for the symmetry between phases, (31) gives the N-phase interleaved boost converter reduced-order model, with the state variables being selected as the output voltage and the inductor current in one phase:

$$A_{ib} = \begin{pmatrix} \frac{-(r_{on}+r_L)}{L} & \frac{-\bar{\delta}}{L} \\ \frac{N\bar{\delta}}{C} & \frac{-1}{(r_C+R)C} \end{pmatrix} B_{ib} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{31}$$

The interleaved double dual-boost and conventional interleaved boost models of reduced order differ mainly in the presence of a term in matrix B that depends on load, which arises from the specific relation between the source and load and which also explains the existence of coefficient 2 (element a_{22}) of matrix $\boldsymbol{A}$, while element a_{21} is generated by dividing phases among two modules.

Small-Signal State-Space Model

The set of possible equilibrium operating points for the converter is:

$$X_{eq} = -A^{-1}BU \tag{32}$$

The collection of equilibrium operating points, using (30), can be obtained as:

$$X_{eq} = \begin{bmatrix} I_{eq} \\ V_{eq} \end{bmatrix} = \begin{bmatrix} \frac{2+2\delta}{4r_L+NR(1-\delta)^2} \\ \frac{2R+NR(1-\delta)}{4r_L+NR(1-\delta)^2} \end{bmatrix} \tag{33}$$

From the expressions in (1) and (33), the relationship between the load voltage and source voltage is written as in (34).

Note that resistive losses are considered in (34); hence, this equation is more accurate than the relation in (2).

$$\frac{V_0}{V_{in}} = \frac{NR(1-\delta^2)}{4r_L + NR(1-\delta)^2} \tag{34}$$

By using the state-space averaging technique [2] and with consideration of the small-signal approximation, the corresponding linear system closer to the equilibrium operating point can be written as:

$$\dot{x} = A\widetilde{x} + [(A_1 - A_2)X + (B_1 - B_2)U]\widetilde{\delta} \tag{35}$$

where:

$$A_1 = \begin{pmatrix} \frac{-R}{L} & 0 \\ 0 & \frac{-2}{R_0C} \end{pmatrix} A_2 = \begin{pmatrix} \frac{-R}{L} & \frac{-1}{L} \\ \frac{N}{2C} & \frac{-2}{R_0C} \end{pmatrix} \tag{36}$$

and:

$$B_1 = B_2 = B = \begin{bmatrix} \frac{1}{L} & \frac{1}{R_0C} \end{bmatrix}' \tag{37}$$

By using (37), (35) can be simplified further to:

$$\dot{x} = A\widetilde{x} + [(A_1 - A_2)X]\widetilde{\delta} \tag{38}$$

Around the operating point, the linearised system's transfer functions are obtained as:

$$H(s) = (sI - A)^{-1}(A_1 - A_2)X_{eq} \tag{39}$$

Expression (39) can be improvised to:

$$\begin{bmatrix} G_{id}(s) \\ G_{vd}(s) \end{bmatrix} = \begin{bmatrix} \frac{(2R_oCV_{eq})s+[4V_{eq}+NR_o(1-\delta)I_{eq}}{2R_oLCs^2+(2RR_oC+4L)s+4R+NR_o(1-\delta)^2} \\ \frac{-NR_oLI_{eq}s-NI_{eq}RR_o+NR_o(1-\delta)V_{eq}}{2R_oLCs^2+(4RR_oC+4L)s+4R+NR_o(1-\delta)^2} \end{bmatrix} \tag{40}$$

where $G_{id}(s) = I(s)/\Delta(s)$ and $G_{vd}(s) = V(s)/\Delta(s)$.

The transfer function $G_{vi}(s) = V(s)/I(s)$ between the voltage and current is obtained from (40):

$$G_{vi}(s) = \frac{V(s)}{I(s)} = \frac{-NR_oLI_{eq}s - NI_{eq}RR_o + NR_o(1-\delta)I_{eq}}{2R_oCV_{eq}s + 4V_{eq} + NR_o(1-\delta)^2I_{eq}} \tag{41}$$

4. Capacitor Voltage Profile

The major goal of this study is to reduce the peak voltage across the capacitor, which can be computed for the IDDB using the formula below:

$$V_{C1} = V_{C2} = \frac{D}{1-D}V_{in} \tag{42}$$

The output voltage in the IDCCB is:

$$V_o = V_{C1} + V_{C2} + V_{in} = \frac{1+D}{1-D}V_{in} \tag{43}$$

In contrast, in the typical scenario [16], capacitor voltages can be calculated:

$$V_{C1\_IDDB} = V_{C2\_IDDB} = \frac{1}{1-D} V_{in} \tag{44}$$

The output voltage in the IDDB is:

$$V_{o\_IDDB} = V_{C1\_IDDB} + V_{C2\_IDDB} - V_{in} = \frac{1+D}{1-D} V_{in} \tag{45}$$

From Equations (43) and (45), it can be understood that the output voltages in the conventional case differ between the sum of the capacitor voltages and input voltage, whereas for the IDCCB this equals the sum of the capacitor voltages and input voltage. Hence, for the same output voltage, the capacitor voltages in the IDCCB are lower than in the conventional IDDB. Figure 5a displays the capacitor voltage profiles in the traditional and proposed cases, while Figure 5b depicts the reduction in voltage stress on the capacitor.

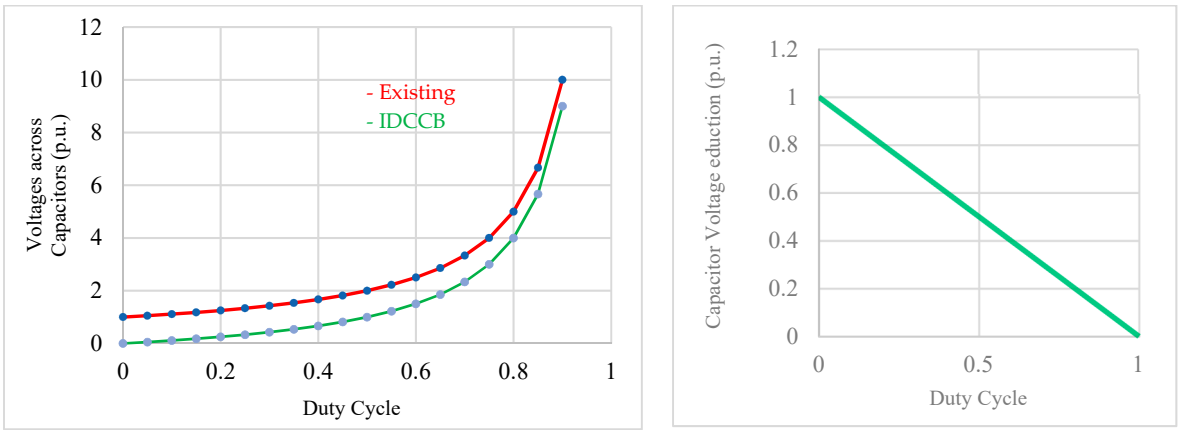

Figure 5. Capacitor voltage profiles (**a**) p.u. capacitor voltages [16] and (**b**) Reduced p.u. stresses on capacitors in existing and proposed IDCCB (the base value is the input voltage).

5. Control Design

Here, an IDCCB converter, which is shown in Figure 2, is considered to exhibit the model's application for the control scheme. The parameters of the converter are presented below in Table 1.

Table 1. Parameters of the proposed converter.

Parameter Name	CCB Module
Input voltage, V_{in}	48 V
Output voltage, V_o	224 V
Duty ratio	0.7857
Load power	1000 W
Output current, A	2.5 A
Load resistance, Ω	89.6 Ω
Inductor current, A	11.666 A
Output voltage ripple, %	≤0.5
Switching frequency, kHz	20
Inductor	0.5 mH
Filter capacitors	4.4 μF/500 V

For practical purposes, high duty ratio values are not suitable due to the large current and low efficiency. Thus, the limit of the duty ratio 0.85. A nominal equilibrium point that belongs to the interval represented by (33) is chosen to obtain the small-signal converter

model, as presented in Table 2. The open-loop transfer function bode plots of input currents and output voltage with respect to the duty ratio and line voltage are plotted in Figure 5, and from this it can be seen that the proposed converter can offer better performance at its input compared to the existing boost-based differential converter for both line and control changes.

Table 2. Equilibrium points of the proposed converter's module.

Parameter	Proposed
Duty ratio (D)	0.7857
Inductor equilibrium current (A)	11.66 A
Capacitor equilibrium voltage (V)	224 V

By utilising the current mode control [4], the control loops are designed using the control-to-current transfer function, as obtained in (40), while the voltage-to-current transfer function is obtained with (41).

The internal current controller loop decides the value of the duty ratio. The outer voltage controller loop generates the average value of the current reference. The control diagrams of the per phase module and per phase current are depicted in Figure 6.

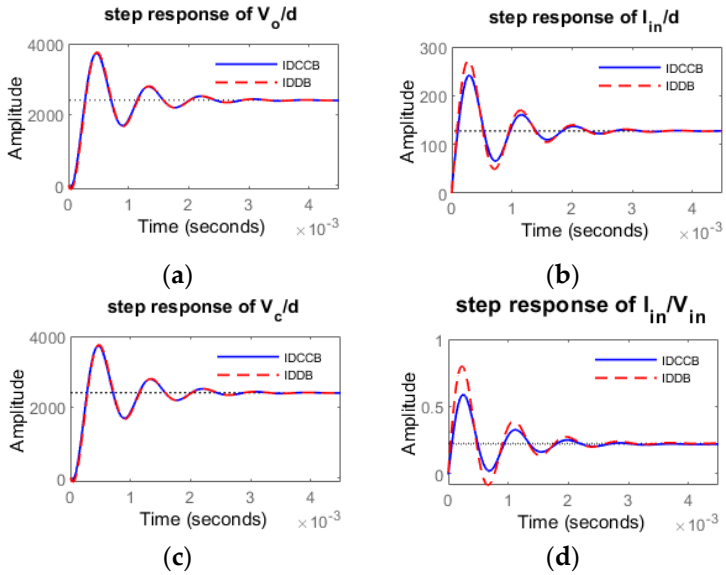

Figure 6. Set of probable equilibrium points: (**a**) output voltage-to-duty ratio (V_o/d); (**b**) input current-to-duty ratio (I_{in}/d); (**c**) capacitor voltage-to-duty ratio (V_c/d); (**d**) input current-to-input voltage (I_{in}/V_{in}) transfer functions of the IDDB and IDCCB.

From Tables 1 and 2, one can evaluate the current-to-duty ratio transfer function of (40), which results in the transfer function being presented in (42):

$$G_{id}(s) = \frac{I_{in}(s)}{d(s)} = \frac{7.995 \times 10^5 s + 7.164 \times 10^7}{s^2 + 597.8s + 1.921 \times 10^6} \tag{46}$$

The inner current loop controller and outer voltage loop controller are represented as the PI controller, as shown in Figure 7. This controller can be written as:

$$G_{pi}(s) = \left(k_p + \frac{k_i}{s}\right)\left(\frac{\omega_p}{s+\omega_p}\right) = \frac{k_i}{s}\left(\frac{s+\omega_z}{\omega_z}\right)\left(\frac{\omega_p}{s+\omega_p}\right) \tag{47}$$

where k_p = proportional gain; k_i = integral gain; ω_p = pole angular frequency; $\omega_z = k_i/k_p$ = zero angular frequency.

Figure 7. Per module and per phase model of the control loop.

The cut-off frequency of the closed-loop block f_{ci} = 1 kHz $\approx f_{sw}/10$ and the phase margin $PM_i = 60^\circ$ are chosen to compute the current controller parameters. The k factor method [5] stipulates that the inner current controller ($G_i(s)$) be considered, which results in the following parameters: k_{ic} = 14.02 rad/s, ω_{zc} = 885.7 rad/s, ω_{pc} = 59,479 rad/s.

By utilising (41), the transfer function between the output voltage and input current is estimated and is shown in (48). In designing the voltage controller, this transfer function is used.

$$G_{vi}(s) = \frac{V_o(s)}{I_{in}(s)} = \frac{-0.3097s^2 + 6195s + 3.635 \times 10^6}{s^2 + 1333s + 4.393 \times 10^5} \tag{48}$$

To derive the cut-off frequency of the inner current control loop to achieve the unity gain and zero phase, the cut-off frequency of the outer voltage control loop should be chosen, as it is much smaller than the current control loop cut-off frequency.

The closed voltage control loop cut-off frequency and phase margin are f_{cv} = 100 Hz and $PM_v = 80^\circ$, respectively.

From the k factor method [5], the voltage controller ($G_v(s)$) is designed and the parameters obtained are: k_{iv} = 40.9 rad/s, ω_{zv} = 117.7 rad/s, ω_{pv} = rad/s.

The digital current mode control is employed to achieve control loops based on [6]. The mean current per phase is obtained by sampling the signal using a current sensor that is synced with the centre of the width-modulated pulse.

The voltage reference employed for both capacitors is the same in order to ensure identical mean voltage conditions in the capacitors (24), as well as similar average current conditions in the phases of the same module (25). Figure 8 illustrates that the current reference for the three phases of the same module is the same. Two voltage controllers (one per module) and six current controllers (one per phase) are used. For this proposed IDCCB, the dual-loop control strategy is implemented to generate the gate signals to control the devices. The outer voltage loops respond to minimise the errors in module voltages by providing appropriate reference currents. These reference currents will be used in three inner current loops of each module. This loop minimises errors in inductor currents by providing appropriate gate signals. The PWM signals of the microcontroller are represented by the PWM blocks.

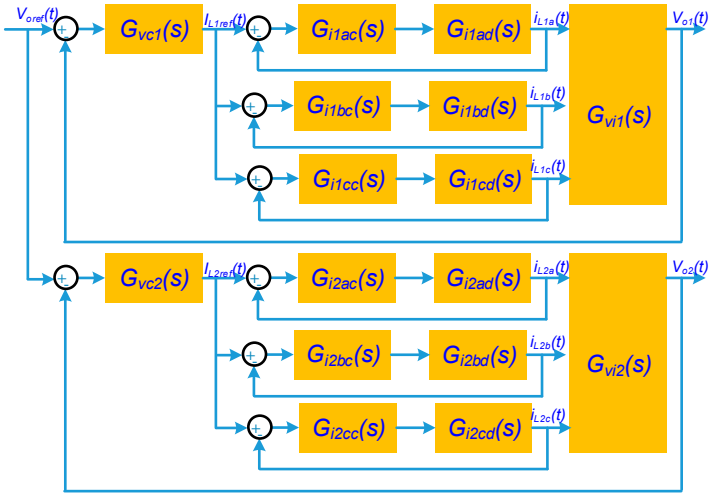

Figure 8. Control diagram of the implemented controller.

6. Parameter Variation Effects

According to Equations (21)–(23), the symmetry condition of the converter is used to reduce the order of the system and to simplify the analysis. In practice, however, there are certain unavoidable component tolerances. By considering the variations in the components, the full model system model is considered to show the viability of the adopted simplifications.

The phase-wise control-to-current transfer functions are computed using MATLAB. The values of the components $\{L_1, \ldots\ldots, L_6\}$, $\{R_1, \ldots\ldots, R_6\}$ and $\{C_1, C_2\}$ are randomly obtained using uniform distribution in the band within $\pm 20\%$ tolerance w.r.t the nominal values in Table 1. This method is performed ten times to generate a total of 60 control-to-current transfer functions. The ensuing loop gains ($T(s) = G_{id}(s) * G_{ic}(s)$) with the designed controller for the nominal component values are shown. Figure 9 depicts the corresponding bode plots. The crossover frequency is designed to be 1 kHz, although the actual values fluctuate between 869 and 1232 Hz (based on the parameters that are randomly generated). The limiting values of the phase margin are 59.37° and 60.45°, both of which are close to the desired limit of 60°.

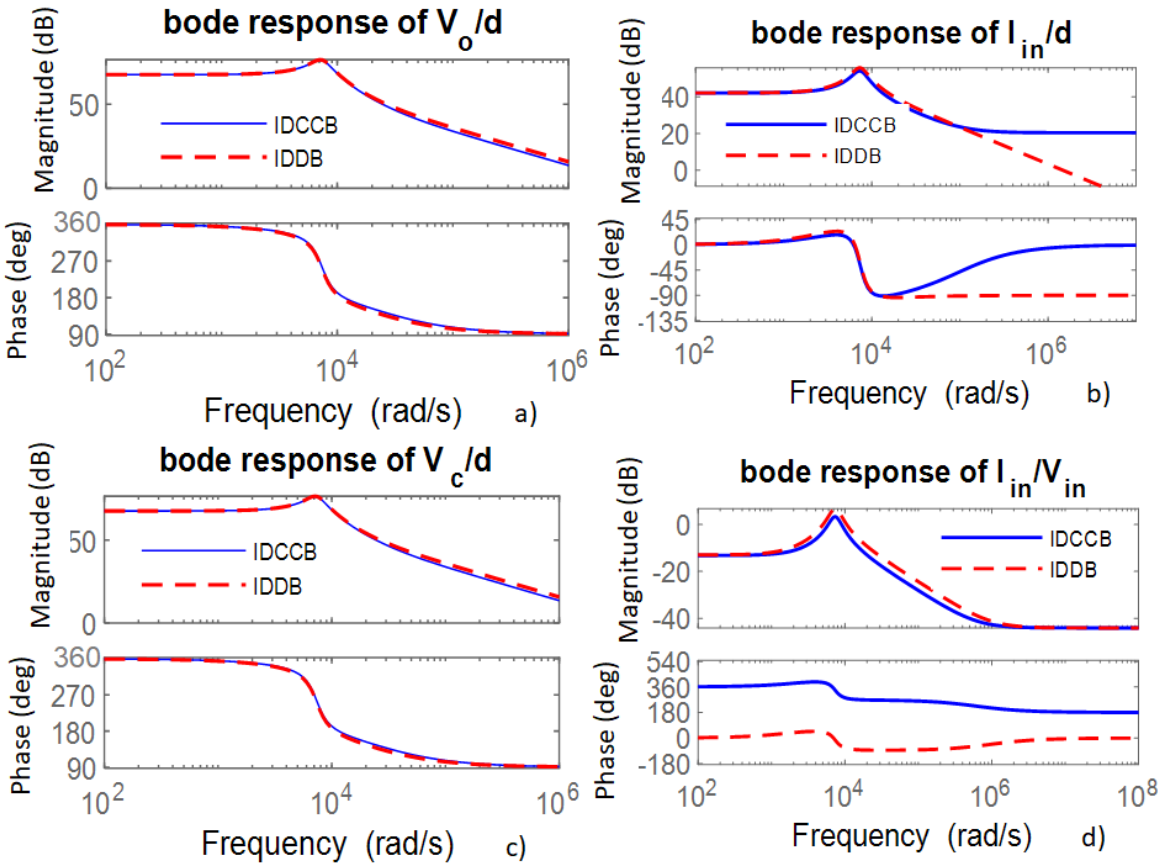

Figure 9. Bode plots: (**a**) output voltage-to-duty ratio (V_o/d); (**b**) input current-to-duty ratio (I_{in}/d); (**c**) capacitor voltage-to-duty ratio (V_c/d); (**d**) input current-to-input voltage (I_{in}/V_{in}) transfer functions for the IDCCB.

The symmetry hypothesis agrees with this analysis, because for the design under consideration here, changes in the parameter values never generate sizeable deviations in the efficiency or closed-loop stability, which is intended for the perfect scenario. A similar method is used for the voltage control loop. The limits of the crossover frequency are 96.7 Hz to 149.4 Hz, with a design value of 120 Hz. The phase margins are 52.6° to 66.3°, while the gain margins are 26.1 dB to 31.3 dB.

7. Experimental Results

Figure 10 shows the six-phase IDCCB experimental setup of the proposed converter used to validate the functionality. For minimisation of the electromagnetic interference, the DSP controller is placed inside a metallic box. The signals from current and voltage sensors are captured using a signal conditioning board and relayed onto the microcontroller.

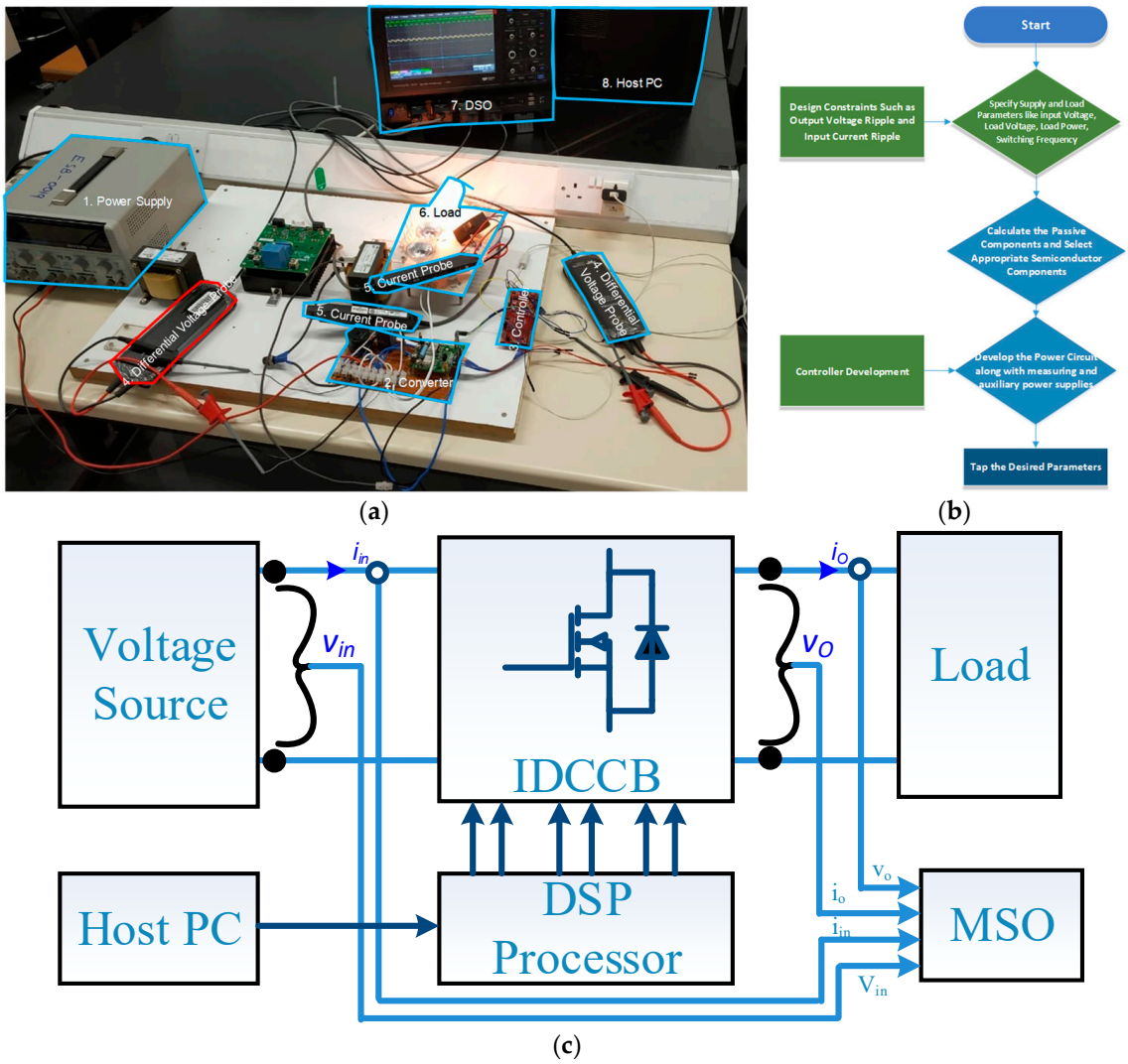

Figure 10. (**a**) Experimental setup: (1) power supply; (2) IDCCB converter; (3) DSP controller; (4) voltage probes; (5) current probes; (7) digital storage oscilloscope; (8) host PC. (**b**) Design guidelines flowchart for the IDCCB and (**c**) block diagram of the hardware setup.

A BlackHawk USB2000 was used to program the DSP controller. The power circuits consisting of the semiconductor switching devices, sensors, and capacitors, and inductors are situated on the power circuit board.

The control procedures were implemented using a Texas Instruments TMS320F28335 DSP controller. The power switches were IRAM20UP60A devices from International Rectifier. The per-phase converter's switching frequency was set to 11.1 kHz (T = 90 s). The converter's nominal operating point was v_i = 60 V, v_o = 360 V, P_o = 2200 W.

The waveforms were obtained with a WaveSurfer 3024z oscilloscope and plotted using MATLAB. Figure 11 depicts the waveforms of the six phase currents captured from the hardware prototype. The currents of all six phases had approximately the same mean value due to the controller action. The peak-to-peak values were variable, as were the slopes of the phase currents, because of the inductor changes. Due to the proper phase displacement,

the ripple was notably decreased in the input current of each module, which can be seen in Figure 12. This leads to ripple content reduction input current, which can be witnessed from Figure 13a, Current supplied to load can be seen from Figure 13b. From this figure, it can be understood that converter is offering smooth dc current to load. The six phases of the converter were dislodged by 60° and the three phases of each module were dislodged by 120°. In the voltages of each module, a similar effect of ripple cancelation was observed, which are summed by Equation (1) for the generation of the output voltage, as shown in Figure 14.

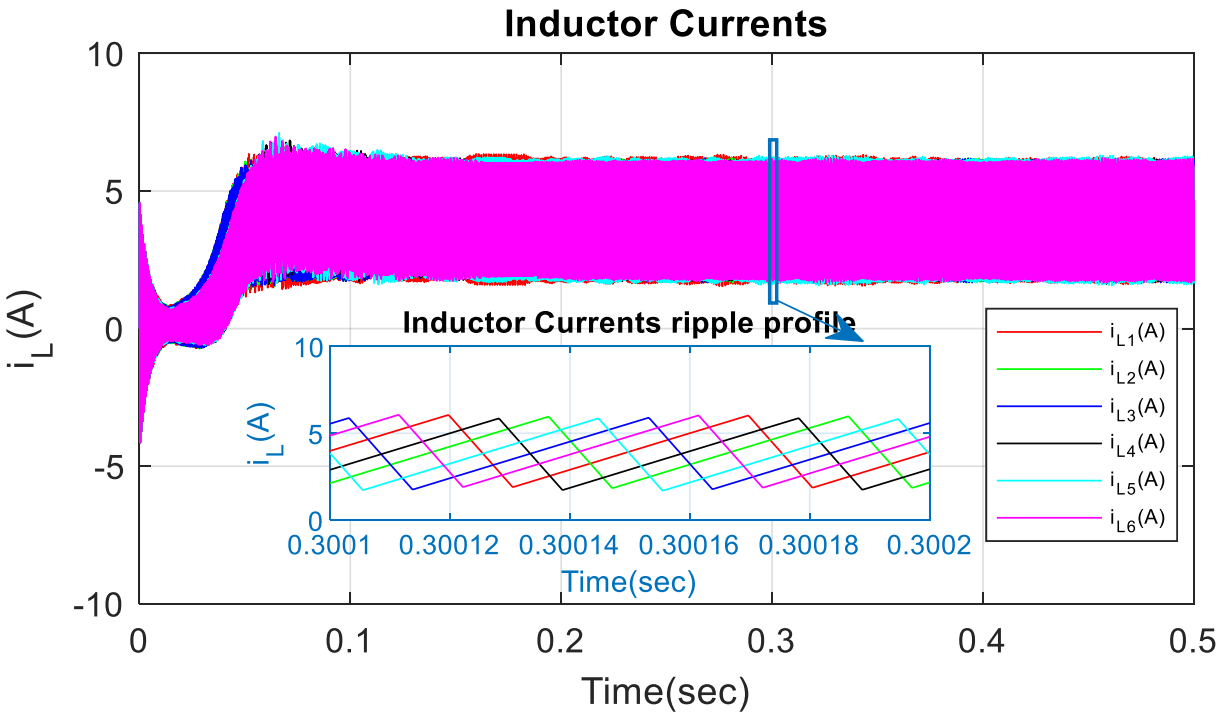

Figure 11. Experimental waveforms of the inductor currents in six phases.

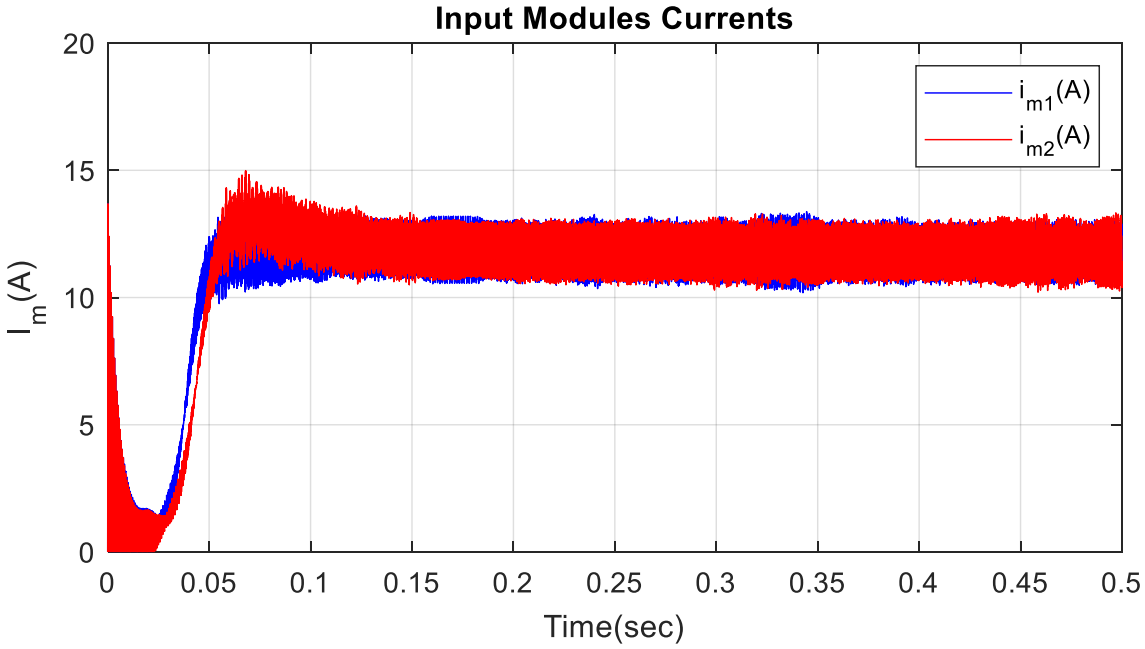

Figure 12. Experimental waveforms of the module input currents in the converter.

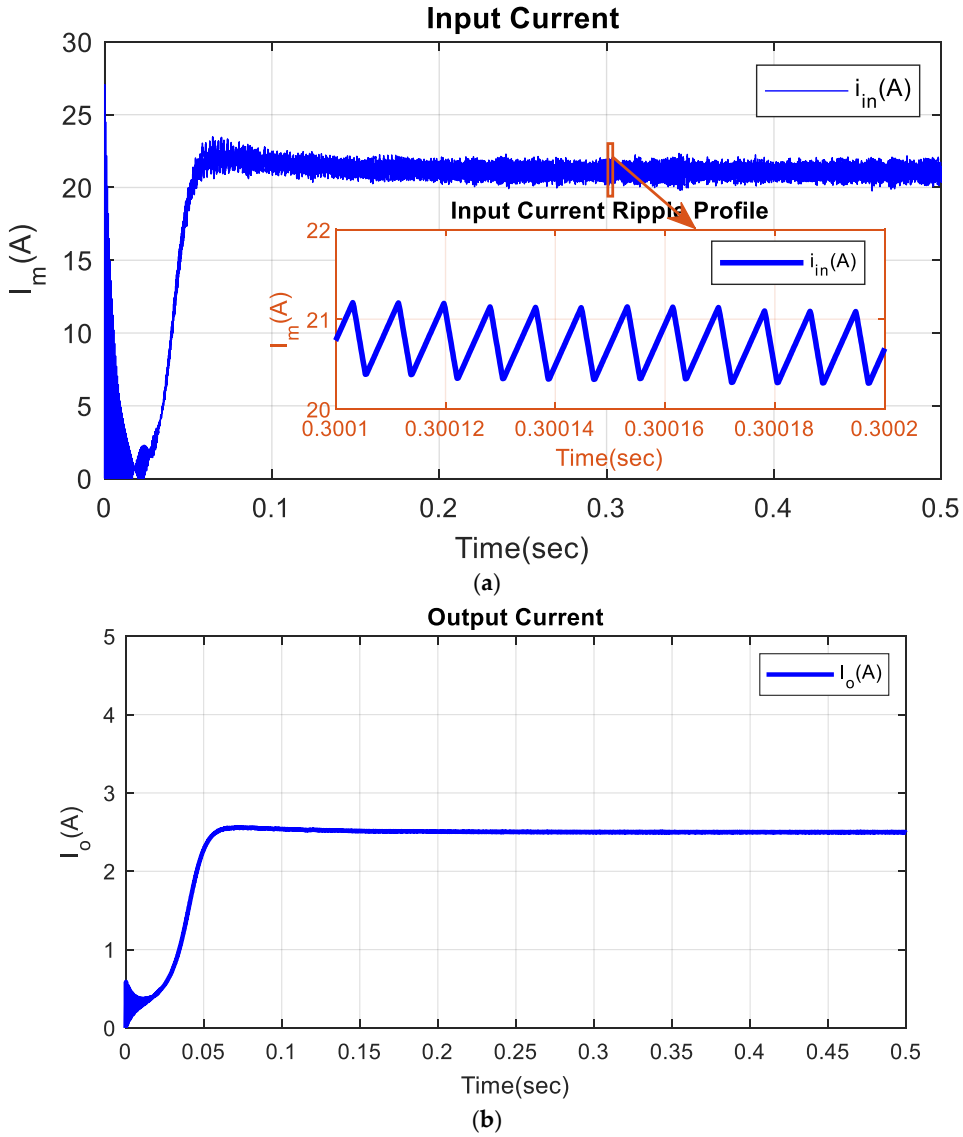

Figure 13. (**a**) Input and (**b**) output currents in the converter.

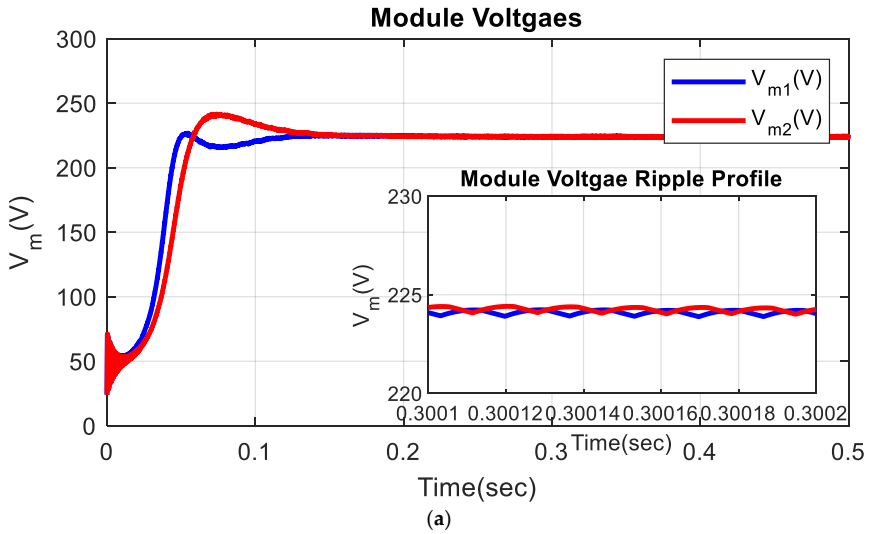

Figure 14. *Cont.*

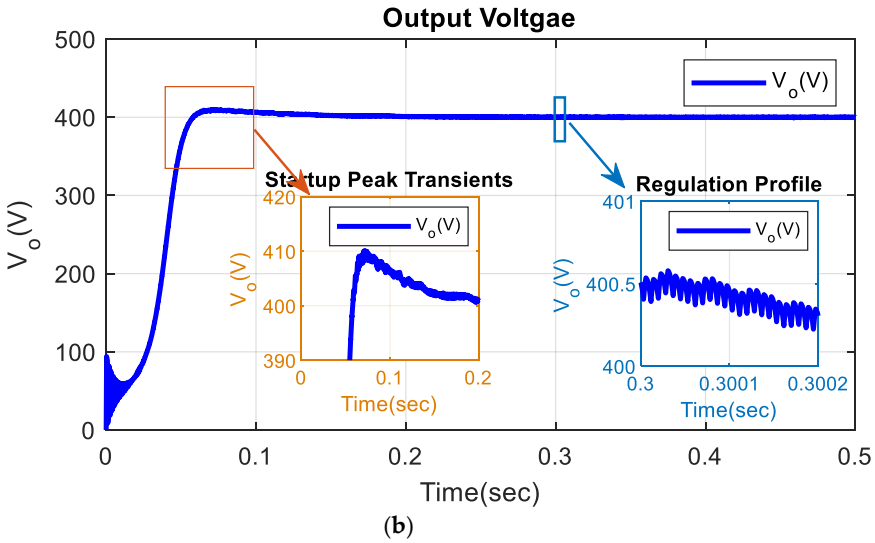

Figure 14. Measurements of the module and output voltages in the converter.

The converter's efficiency for input voltages ranged from 40 V to 100 V in 20 V steps. The output power varied from 200 W to 3.6 kW in 200 W intervals (note that the higher input voltage allowed the converter to operate at higher output power). The converter's efficiency was measured to be 92.8 percent at the nominal operating point.

A positive step change in load was introduced in the converter, with the load varying from 500 W to 1000 W, the result of which is shown in Figure 15. Figure 16 shows the reverse step load shift, with the load changing from 1000 W to 500 W.

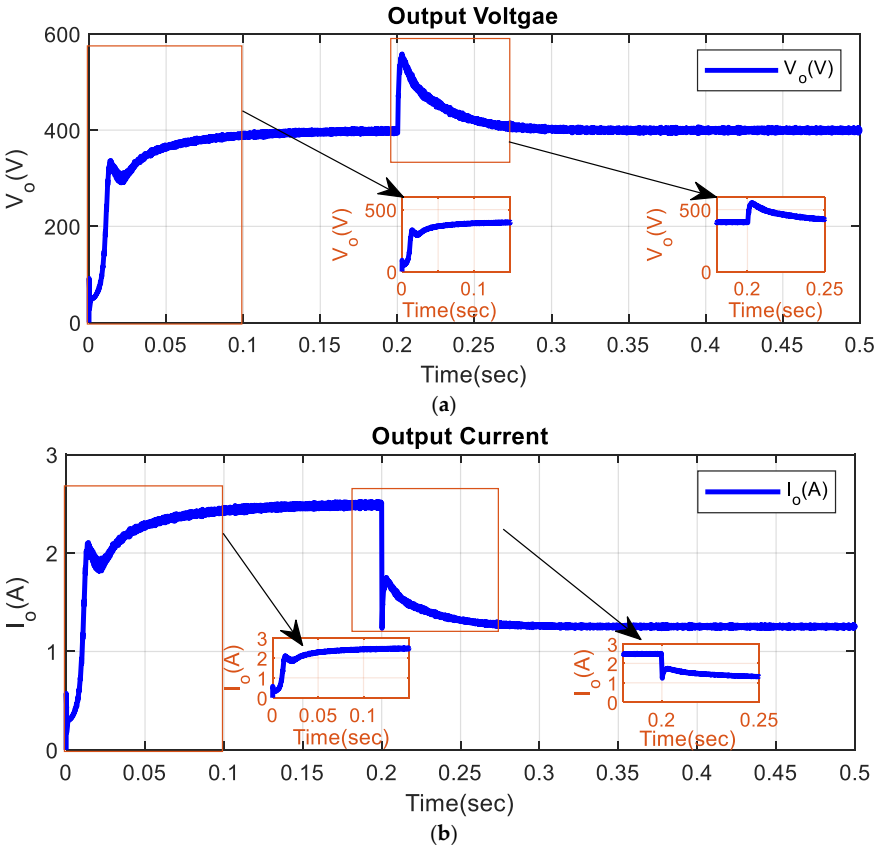

Figure 15. Load parameters during load change from 1000 W to 500 W.

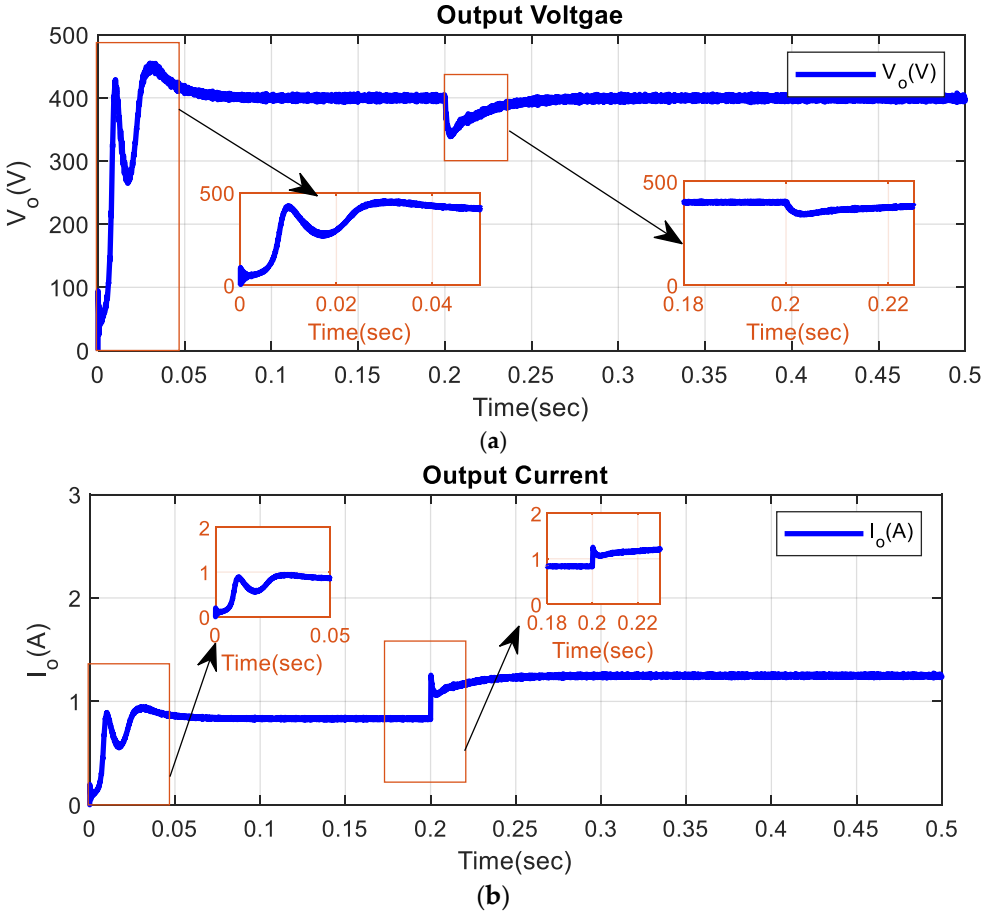

Figure 16. Load parameters during load change from 500 W to 1000 W.

The undervoltage was precisely 4% for the positive load change, as shown in Figure 15. The settling time at 95% of the mean value was precisely obtained as 20 ms. Meanwhile, the overvoltage was precisely 8.5% for the negative load change, as shown in Figure 16, and the settling time was precisely 25 ms.

8. Conclusions

This work has described the modelling of a generalised *N*-phase IDCCB, as well as the development of a small-signal model for an IDCCB circuit. The controller design and implementation processes were presented for a six-phase IDCCB, and experimental verification was carried out to confirm the design. The symmetry of the converter and the control action were used to simplify the model, and the viability of the simplifying assumptions was examined so as to reduce the complexity of the model. Altering the placement of components in the converter along with the adopted control schemes resulted in high gains and the sharing of input currents, making this topology suitable for high-power applications. The analysis of the IDCCB proved that the output voltage for this converter is equal to the sum of the two capacitor voltages and the input voltage, which is two times higher than the supply voltage when compared to the conventional interleaved differential dual boost converter. This converter reduces stress on the capacitor compared to the conventional interleaved differential boost converter for the same conversion gain. Additionally, a dynamic analysis of the converter was presented and the results of the load changes proved that the converter is able to offer better dynamic performance.

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