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A Multi-Band LNA Covering 17–38 GHz in 45 nm CMOS SOI

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Abstract: This paper presents a multi-band low-noise amplifier (LNA) in the 45-nm CMOS silicon-on-insulator (SOI) process. The LNA consists of three stages, with the differential cascode amplifier as the core structure. The first stage is mainly responsible for input matching to ensure favourable noise characteristics and bandwidth, while the subsequent stages increase the gain. Moreover, the LNA utilizes baluns for input/output and interstage impedance matching. Switch capacitances are added to switch the three operating bands of the LNA, which cover 17–38 GHz overall. Measurement results show that the proposed LNA achieves a gain (S21) of 23.0 dB and a noise figure (NF) of 4.0 dB.

Keywords: balun; cascode; low-noise amplifier (LNA); multi-band; switch capacitance

1. Introduction

The vigorous progress of wireless transmission presents a growing demand for high data rates, driving the quest for more spectrum-efficient systems and high-frequency broadband applications, such as 5G communication, broadband satellite communication, and millimeter-wave (MMW) automotive radars [1]. Designs for transceivers, as wireless communication systems' front ends, have emerged endlessly. Transceivers covering broadband, suitable for multiple providers and applications, can significantly reduce the cost of research and manufacturing. Thus, the wideband technique has become popular [2]. Low-noise amplifiers (LNA) play an irreplaceable role in determining the noise characteristics, bandwidth, linearity, and sensitivity of the receiver. Figure 1 shows the functional orientation of an LNA in a multi-band receiver.

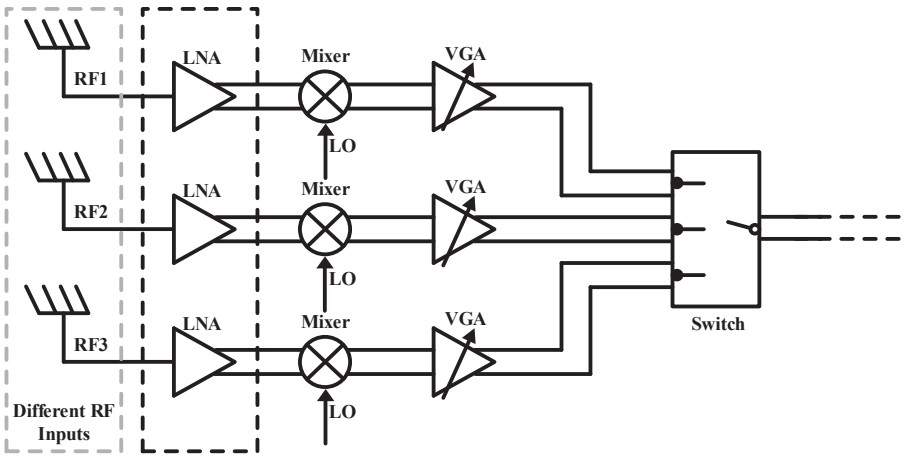

Figure 1. LNA in a receiver system.

The common source (CS) amplifier is utilized for wideband LNA in designs [3–5]. However, advanced techniques are often needed to improve the poor input matching for CS-LNA. Source degeneration inductors were used in [3], and a bandwidth enhancement

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technique was adopted in [4] to obtain broadband. In other designs [6–12], wideband LNA was implemented based on the common gate (CG) amplifier, which can provide preferable wideband input matching. Nevertheless, CG-LNA is disturbed by high power consumption. To work out the situation above, a gm-boosting technique was proposed in [11]. The current-reuse technique was also a candidate in [10]. Beyond that, in [10], the low gain was another drawback that made additional stages necessary. In comparison with CS and CG structures, the cascode LNA possesses advantageous high gain, broadband matching, and high reverse isolation, as seen in various works [1,2,13–24]. In this paper, a wideband LNA is proposed in multi-band mode based on the cascode structure. The differential form is adopted to facilitate system-on-chip integration due to its high resistance to the power supply and common-mode noise.

The reminder of the manuscript is organized as follows: Section 2 introduces the structure of the LNA and the condition of input/output and interstage matching, Section 3 gives the measurement results of the LNA, and Section 4 concludes the work of this paper.

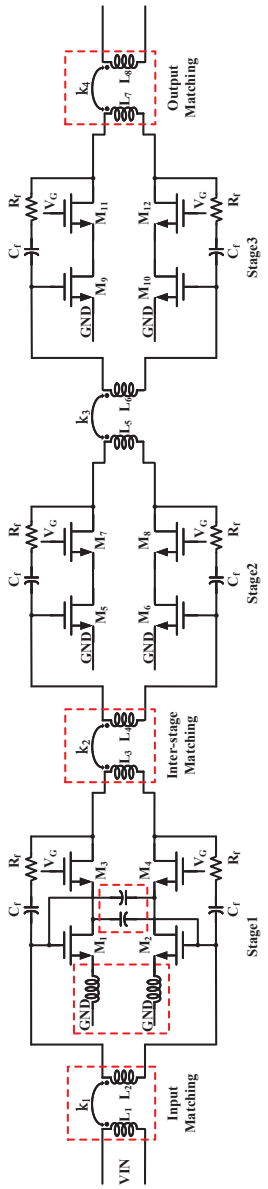
2. Circuit Design

The schematic of the proposed LNA is shown in Figure 2. To obtain a high gain, the LNA consists of three stages, of which their basic structures are semblable, referring to the differential cascode amplifier. Regarding a multi-stage LNA, the input/output and interstage impedance matching are of importance. For this work, baluns are utilized to realize favorable matching. The first stage in the LNA is of the essence, as it has a great impact on NF, bandwidth, and gain. Compared with the subsequent stages, the first stage has source degeneration inductors and cross-coupling capacitors. The input and output ports of the LNA are matched to 50 Ω.

2.1. The Structure and Performance of the LNA

As shown in Figure 3, due to the influence of parasitic capacitances C_{GS} and C_{GD}, the input port of the traditional differential cascode amplifier can be equivalent to a parallel RC network in terms of impedance matching. The equivalent shunt resistance converted from the impedance seen from the input port is on the order of kilo-ohms. The inductor in balun will be enormous when making a resistance of kilo-ohms be matched to 50 Ω, resulting in the vast majority of the chip area. As a solution to the problem above, a series RC feedback link is introduced between the input and output port of the circuit, as shown in Figure 4a. Considering the Miller effect, the feedback link can be equivalent to the impedance R_{miller} at the input port, which is shown in Equation (1). R_f is the feedback resistance, and $|A_v|$ is the open-loop gain of the circuit. The connecting of the equivalent network of the input port and the R_{miller} in parallel reduces the real part of the impedance seen from the input port.

$$R_{miller} = \frac{R_f}{1 + |A_v|} \tag{1}$$



M_1-M_{12}	64 μm/40 nm	L_3	553 pm
k_1	0.6 V/(cm·Oe)	L_4	207 pm
k_2	0.57 V/(cm·Oe)	L_5	553 pm
k_3	0.57 V/(cm·Oe)	L_6	207 pm
k_4	0.57 V/(cm·Oe)	L_7	802 pm
L_1	221 pm	L_8	331 pm
L_2	600 pm	V_{DD}	1.2 V

Figure 2. The schematic of the proposed LNA.

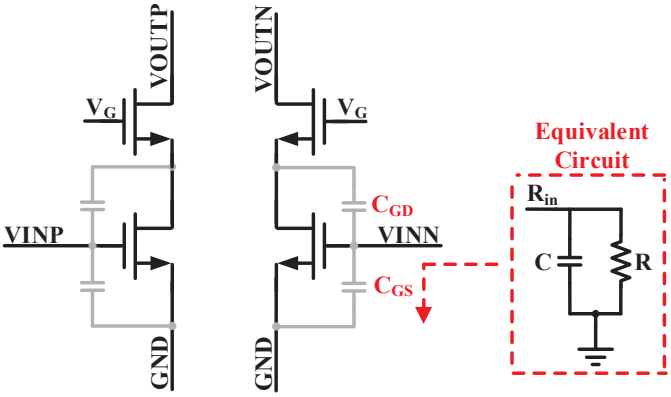


Figure 3. The traditional differential amplifier and the input equivalent circuit.

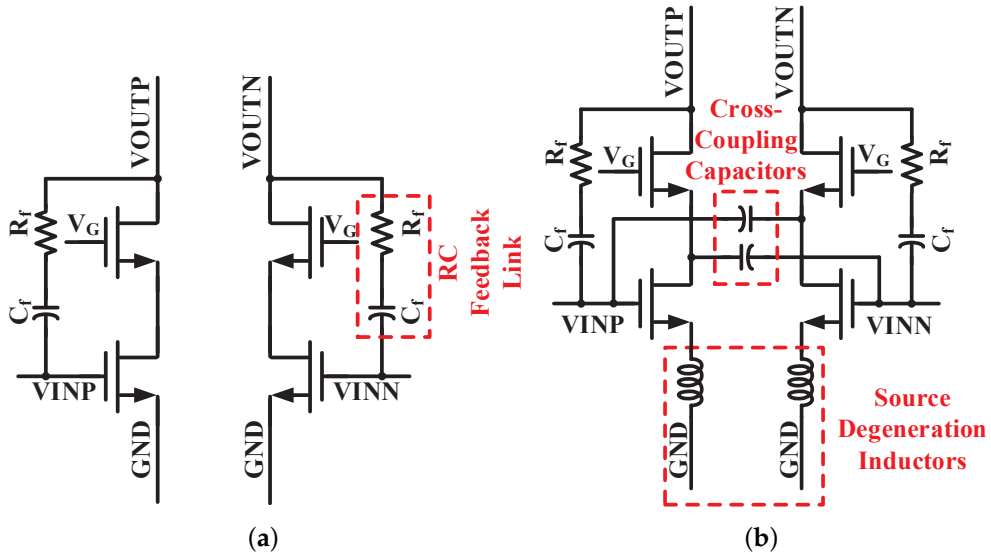


Figure 4. (**a**) Adding feedback links based on the traditional differential cascode amplifier; (**b**) adding additional cross-coupling capacitors and source degeneration inductors.

To further satisfy the 50 Ω impedance matching of the input port, the source degeneration inductors are added to the first stage to reduce the input port impedance and optimize the noise characteristics, shown in Figure 4b. Simultaneously, cross-coupling capacitors are added, which can eliminate parasitic effects and provide a gm-boost. Figure 5 shows the S21 and NF simulation results of the first stage with and without cross-coupling capacitors. The simulations of gain, input return loss (S11), noise figure, and input impedance are performed by Cadence Virtuoso Spectre RF using S-parameter analysis.

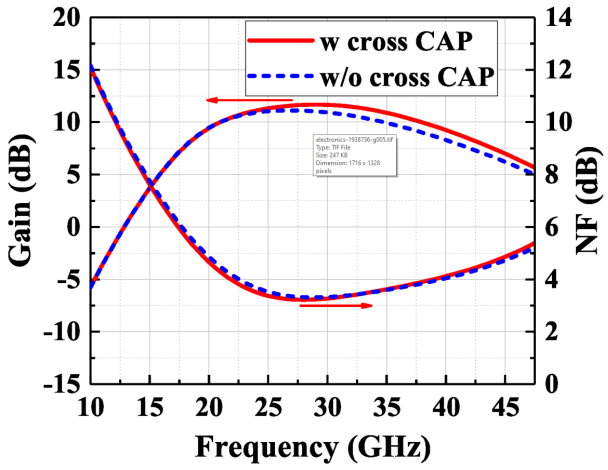


Figure 5. The gain and NF simulation results of the LNA with and without cross-coupling capacitors.

Comprehensively considering the power consumption, input impedance, and gain of the proposed LNA, the transistors (M_1–M_{12}) are designed as 16 fingers with a total channel width of 64 μm. On the premise that the transistors have the same size, Figure 6 shows the simulation results of the impedance of the traditional differential cascode amplifier and the structures of the proposed LNA, which undergoes an equivalent transformation from series to parallel. The black line corresponds to the traditional cascode amplifier. The blue line and the red line correspond to the circuits; only the feedback link is added in one, and in the other, both the feedback link and degeneration inductor are added. Both them are based on the traditional cascode amplifier.

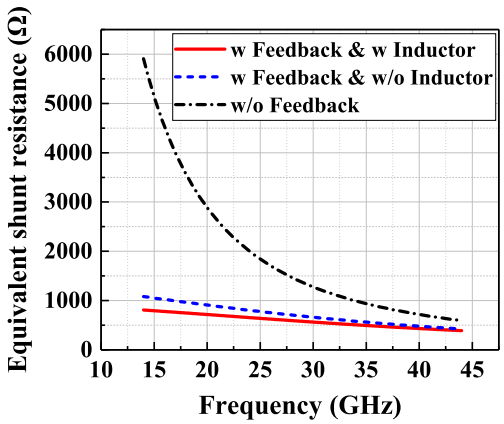


Figure 6. The impedance of the traditional differential cascode amplifier and the structures of the proposed LNA.

The first stage of the LNA sacrifices gain for admirable input matching and low NF. Thus, two additional stages are appended to boost the gain. Apart from the high gain, the LNA has three operating bands, controlled by a 2-bit signal. The gain simulation results of stepwise circuits in three bands are shown in Figure 7.

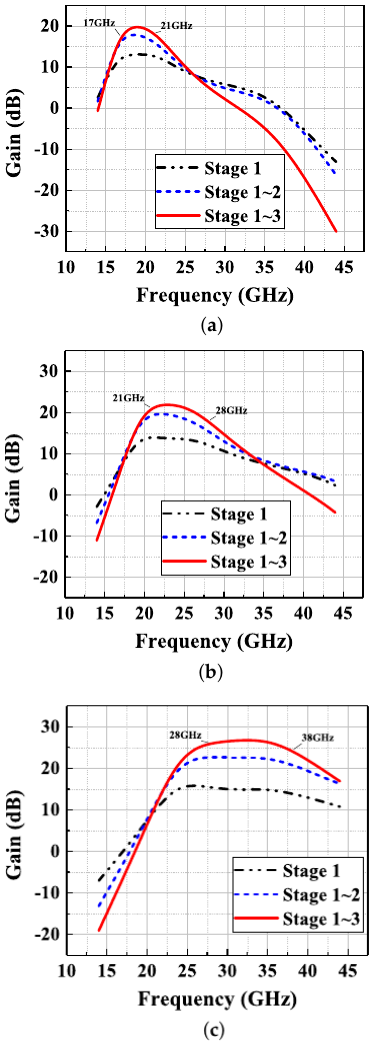


Figure 7. The gain of all stages simulated in (**a**) 17–21 GHz, (**b**) 21–28 GHz and (**c**) 28–38 GHz.

2.2. Magnetically Coupled Resonator(MCR) Matching Network

In order to obtain a broad bandwidth, the MCR matching network is adopted for impedance matching [25]. Taking input port matching as an example, the resistance seen through the balun is converted to 50 Ω. Figure 8 shows the input port matching network and the equivalent network on both sides of the balun. As shown in Figure 8b, the prerequisite conditions for the matching network are as follows: R_1 of the tank1 is 50 Ω, and R_2 and C_2 of the tank2 can be obtained by converting the accessible simulation data. On this basis, the value of L_1, L_2 and C_1 can be determined as long as the resonant frequencies of the networks are definite. To enhance the bandwidth, the resonant frequencies of RLC networks on both sides are set as different frequencies f_1 and f_2; thus, the S21 image of the balun can produce two peaks, as shown in Figure 9. Figure 10 shows the gain and S11 simulation results of the first stage with different magnetic coupling coefficients k in the range of 28–38 GHz. As the coefficient increases, the bandwidth of the LNA is extended. However, k is restricted in balun. The same approach is applied to the output and interstage matching.

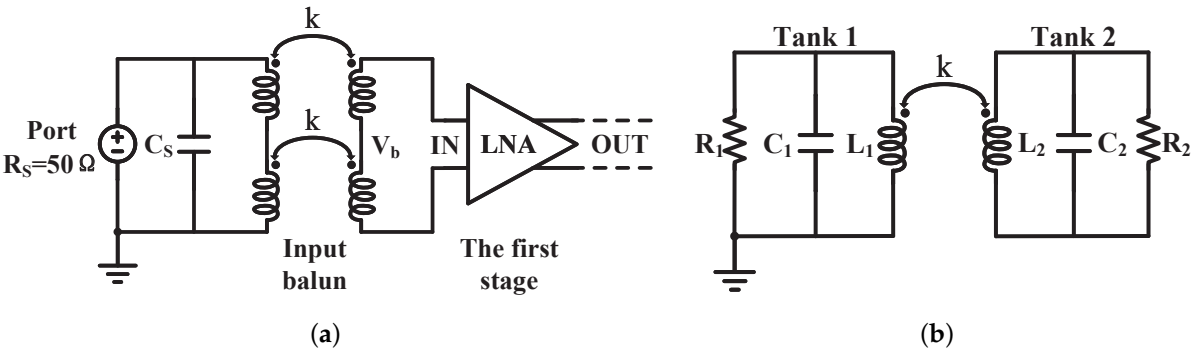


Figure 8. (**a**) The input port matching network and (**b**) the equivalent circuit of the balun.

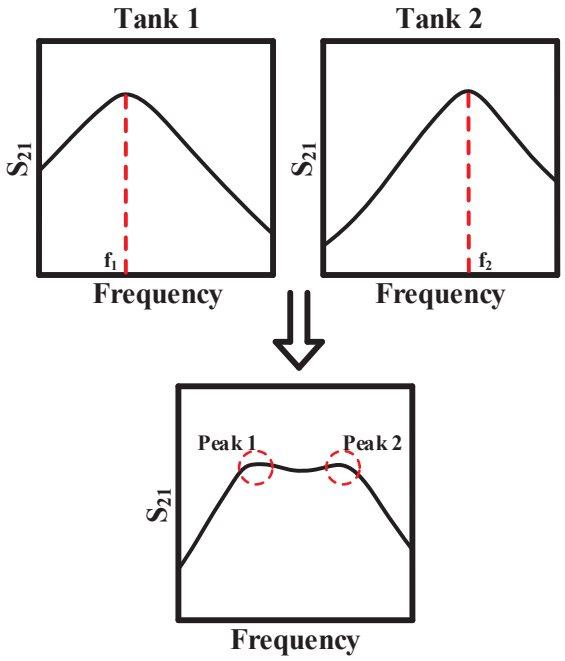


Figure 9. Wideband technology.

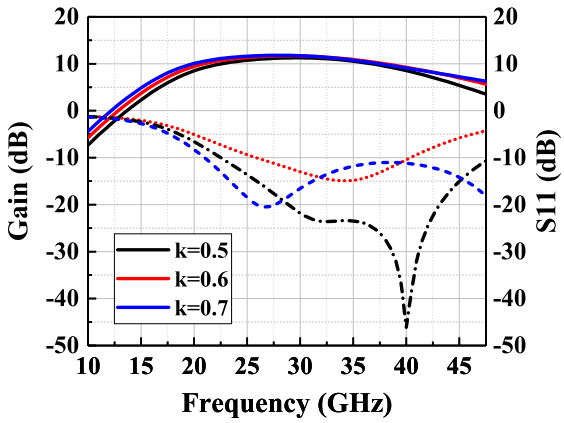


Figure 10. Gain and S11 simulation results of LNA with different magnetic coupling coefficients.

Due to the compromise between the bandwidth and the gain, the LNA is designed with three operating bands. Switch capacitances are introduced, which can conduct the switching of three operating bands with a 2-bit control signal. There is a trade-off for the switching transistor design. A switching transistor with a large size has preferable conduction characteristics, but this worsens the matching situation due to the large parasitic capacitance. Conversely, a switching transistor with a small size has less impact on matching but brings additional power consumption due to its low equivalent shunt resistance.

Figure 11 shows the switch capacitances designed in the LNA, which are inserted at the input and output port of all stages in parallel. Figure 12 shows the S11 simulation results of the LNA with the switch capacitors in different states. With the switch of the LNA input port on, the capacitor is connected in parallel at the input port, and the resonant frequency decreases.

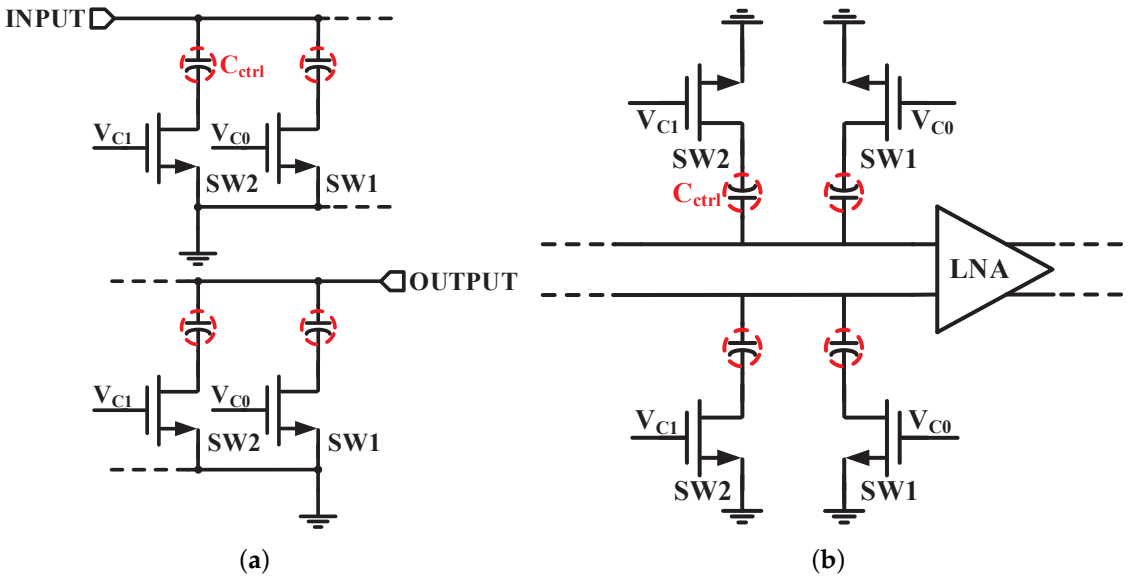


Figure 11. The switch capacitances in LNA (**a**) for input/output port and (**b**) for interstage coupling.

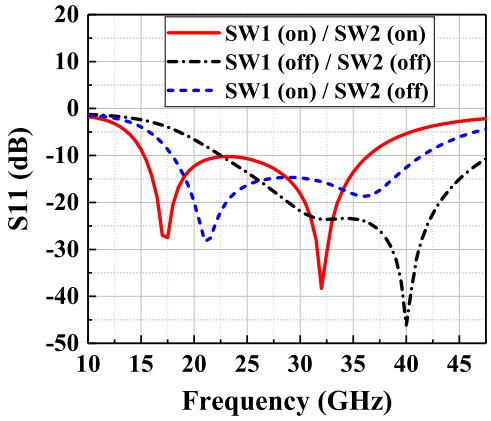


Figure 12. S11 of LNA with switch capacitors in different states.

The change in resonant frequency is associated with a change in capacitance. The switch capacitance is in the high-impedance state when the transistor turns off, while it is correspondingly capacitive when the transistor turns on. In the case of the latter, C_{ctrl} is connected in parallel with the parasitic capacitance of the transistor at the input port, which increases the capacitance of the input port. On the premise that balun's matching inductance remains unchanged, according to $\omega = 1/\sqrt{LC}$, the resonant frequency will move to a low frequency. Utilizing this principle, the resonant frequencies of both sides in balun extend to low frequencies simultaneously. Thus, the LNA can realize the migration of the operating frequency band.

3. Measurement Results

The LNA is designed and implemented in the 45-nm CMOS SOI process. Figure 13 shows the die micrograph of the LNA, occupying a chip area of $0.94 \times 0.34\,\mathrm{mm}^2$. The power consumption is 59 mW from 1-V supply. The chip is tested under the probe station in the measurement process. The input and output of the LNA are directly connected to the test instrument through GSG RF pads on the chip using Cascade RF probes. The block diagram of the measurement setup is shown in Figure 14. An Agilent E3646A DC source provides a power supply of 1 V. An Agilent N5245A Vector Network Analyzer (VNA) is used to measure the S-parameters, gain, and NF. The connection cables and probes are calibrated before measurement to ensure the accuracy.

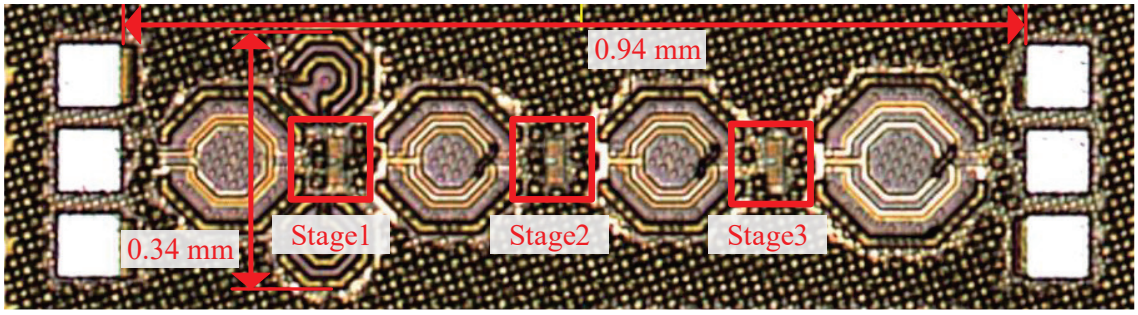


Figure 13. The die micrograph.

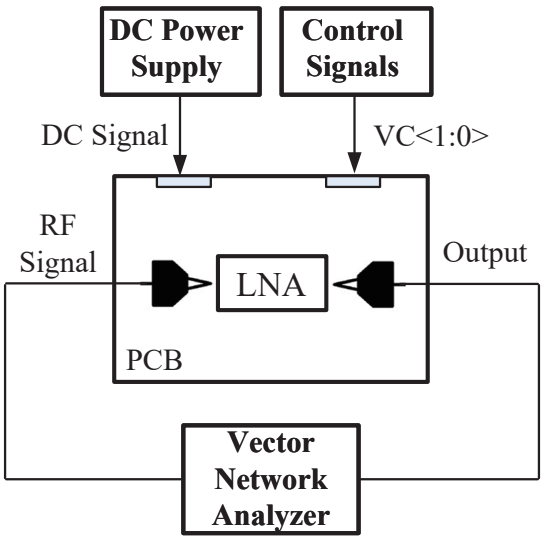
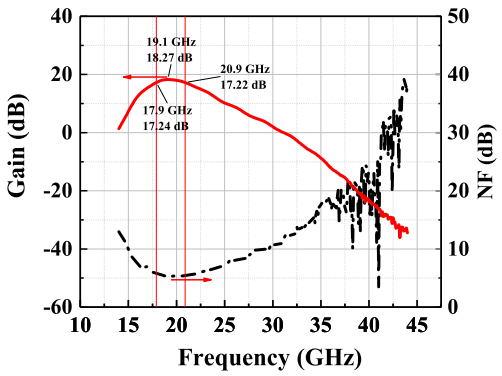
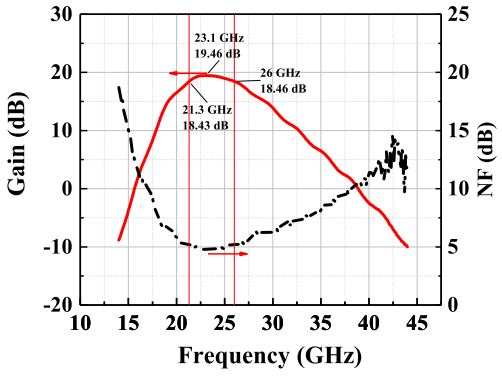


Figure 14. The measurement setup.

Figure 15 shows the measurement results of the S21 and NF in 17–21 GHz, 21–28 GHz and 28–38 GHz. The maximum gain in each band is 18.3 dB, 19.5 dB and 23.0 dB, while the minimum NF is 5.2 dB, 4.7 dB and 4.0 dB, respectively. The measured 1-dB gain bandwidth is 3 GHz, 4.7 GHz and 5.4 GHz, respectively, in each operating band. Table 1 summarizes the maximum gain, and the minimum NF.



(**a**)



(**b**)

Figure 15. *Cont.*

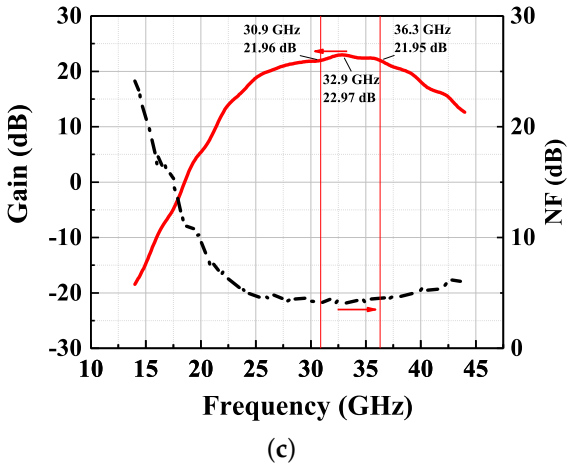


Figure 15. The measured gain, and NF at (**a**) 17–21 GHz, (**b**) 21–28 GHz and (**c**) 28–38 GHz.

Table 1. The performance summary.

Frequency Band (GHz)	Maximum Gain (dB)	Minimum NF (dB)
17–21	18.3	5.2
21–28	19.5	4.7
28–38	23.0	4.0

Figure 16 shows the synthesis of gain and NF measurement results in three bands exhibiting that the LNA can provide high gain and low NF across the full frequency band. A figure of merit (FOM) for evaluating the performance of a broadband LNA is defined as Equation (2).

$$FOM[\frac{GHz}{mW}] = \frac{S_{21}[mag] * BW[GHz]}{(NF-1)[mag] * P_{DC}[mW]} \quad (2)$$

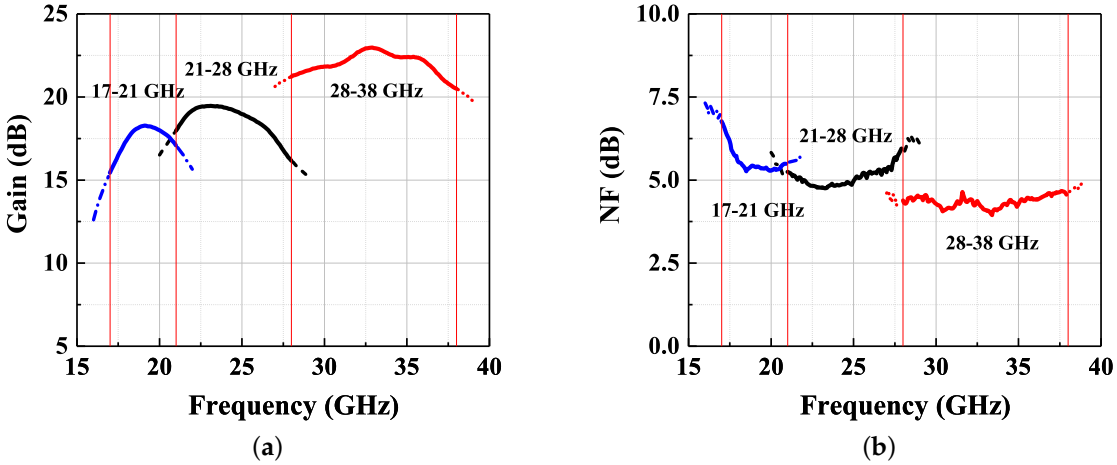


Figure 16. The synthesis of (**a**) gain and (**b**) NF measurement results in three bands.

Table 2 compares the performance of this design with the state-of-the-art wideband LNAs. The LNA in [9], which can operate under two supply voltages, has a low power consumption but low gain and a narrow band. The works [16,17,23,24] also adopted the cascode structure. However, [16,23] used low gain, [17] had narrow bands and [24] had an inferior NF. It is evident that this work achieves the best FOM of 4.9 GHz/mW. The

proposed LNA obtains high gain, low NF, and high FOM with a wide operating band covering 17–38 GHz.

Table 2. The summarized performance of the proposed LNA.

Reference	Process	Architecture	Supply Voltage (V)	Bandwidth (GHz)	Gain (dB)	NF (dB)	FOM (GHz/mW)	Area (mm^2)
[9] [a]	0.13-µm CMOS	CG	0.6 1.2	17.3-29.3 17.3–29.3	15.4 18	5.5–7 4.7–6.2	- -	0.192 [b]
[17]	65-nm CMOS	Cascode	-	30–34.5	20.8	3.71	1.4	0.39
[16]	45-nm CMOS SOI	Cascode	1	24–30	11.2	3.2	0.7	-
[23]	65-nm CMOS	Cascode	-	15.8–30.3	10.2	3.3–5.7	3.3	0.18
[24]	0.18-µm BiCMOS	Cascode	1.8	22–32.5	18.6	4.5–5.5	-	0.46 [b]
This work	45-nm CMOS SOI	Cascode	1	17–21 21–28 28–38	18.3 19.5 23.0	5.2 4.7 4.0	4.9	0.42 [b]

[a] Two supply voltages; [b] w/o pads.

4. Conclusions

In this work, a multi-band LNA is designed and implemented in a 45-nm CMOS SOI process, which is composed of the differential cascode amplifier, RC feedback link, and source degeneration inductor. The LNA consists of three stages in order to achieve high gain, broadband, and low NF, and adopts baluns for the input/output and interstage impedance matching. Meanwhile, by adding switch capacitances, the proposed LNA realizes the switching of three operating bands, 17–21 GHz, 21–28 GHz, and 28–38 GHz. Measurement results show that the maximum gain is 23.0 dB, and the minimum NF is 4.0 dB, while occupying a chip area of $0.94 \times 0.34\ mm^2$. This work has a certain reference value for multi-band LNA design.

Author Contributions: Conceptualization, F.H., X.L. (Xuzhi Liu) and Z.L.; data curation, Q.Q. and Z.L.; formal analysis, F.H., X.L. (Xuzhi Liu) and C.W.; funding acquisition, X.L. (Xiao Li) and X.L. (Xiaoran Li); investigation, F.H., X.L. (Xuzhi Liu), C.W. and X.L. (Xiaoran Li); methodology, X.L. (Xuzhi Liu) and Q.Q.; project administration, X.L. (Xiao Li), X.L. (Xiaoran Li) and Z.L.; supervision, Q.Q., X.L. (Xiaoran Li) and Z.L.; validation, X.L. (Xuzhi Liu) and Z.L.; visualization, F.H., C.W. and X.L. (Xiaoran Li); writing—original draft, C.W.; writing—review and editing, F.H. and X.L. (Xiaoran Li). All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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