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A Novel Non-Isolated Step-Up DC/AC Inverter with Less Switches

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Abstract: In order to solve the problem of leakage current and step-up voltage capability associated with the single-phase single-stage non-isolated inverter, a new topology is proposed in this paper. The proposal has the advantages of less switch components, high step-up voltage capability and no leakage current. The three operation modes are discussed and the modulation strategy is designed. Finally, the prototype of the proposed new single-phase single-stage non-isolated inverter is established. The TMS320F28335 DSP and Xilinx XC6SLX9 FPGA are used to provide the system with digital control. The experimental results show that the proposed inverter achieved the boosted ability as well as the sinusoidal output voltage, whose total harmonic distortion is well below 5%, which meets the IEEE Std. 519-2014.

Keywords: single-phase inverter; single-stage inverter; circuit topology; modulation

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1. Introduction

Renewable energy installation is increasing rapidly, and the world added nearly 290 gigawatts of renewable power capacity in 2021. The IEA's Renewables Market Report forecasts that the planet's renewable electricity capacity will jump to more than 4800 GW by the year 2026. As one of the most prevalent renewable energy sources (Figure 1), solar energy is undoubtedly a powerful engine that can drive the planet past "carbon peak" and towards "carbon neutrality".

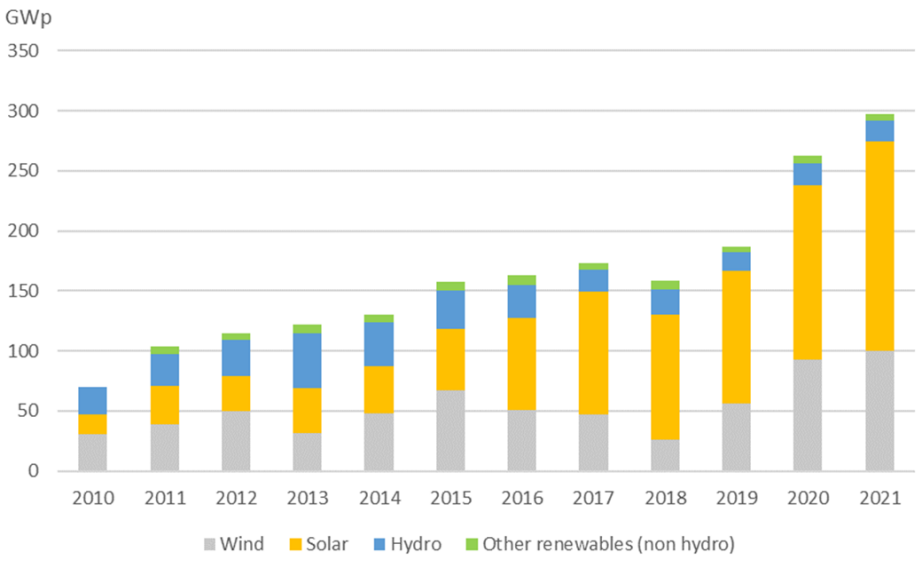


Figure 1. Evaluation of renewable energy annual installation.

Traditional photovoltaic inverters are divided into two types: isolated and non-isolated [1,2]. Isolated grid-connected inverters are divided into power frequency transformer isolation mode and high-frequency transformer isolation mode. At the beginning of the development of photovoltaic grid-connected inverters, power frequency transformer isolation mode was mostly used, but these inverters have obvious disadvantages, including size, weight and cost.

In recent years, grid-connected inverters with high-frequency transformer isolation modes have developed rapidly, and non-isolated grid-connected inverters have gradually been accepted for their high efficiency and simple control. Therefore, non-isolated inverters have not been the focus of development [3,4]. Many novel inverter topologies have appeared in recent years, such as Heric, H5, H6, etc. [5–16]. This type of topology changes the common mode characteristics of the circuit by adding switches, which reduces the leakage current of the system to a certain extent. However, since the parasitic capacitance voltage is still affected by the low frequency grid voltage, the resultant ground leakage current cannot be fundamentally eliminated. In addition, these non-isolated inverters are all step-down in structure. Due to the low voltage level generated by the photovoltaic array, it is necessary to add a front-stage DC/DC boost circuit [17], resulting in a complicated system control scheme that needs to coordinate pre-stage and post-stage power control. Besides, additional switching devices in the front-end circuit of the system increase the system cost.

The objective of this paper is to propose a novel step-up inverter. The rest of the paper is organized as follows: Section 2 presents the theoretical analysis and design the proposed inverter, as well as its modulation strategy, Section 3 provides the experimental test results of the proposed inverter, and the conclusion is drawn in Section 4.

2. Analysis and Design of New Type Inverter

Figure 2 shows the single-phase monopole inverter topology proposed in this paper, which includes: input source V_{in}, inductor L_3, capacitor C_3, switching device S_1, inductor L_1, L_2, capacitor C_1, C_2 and switching device S_2, S_3. This topology has the advantages of boost ability and double-end common ground. The circuit principle is analyzed as follows:

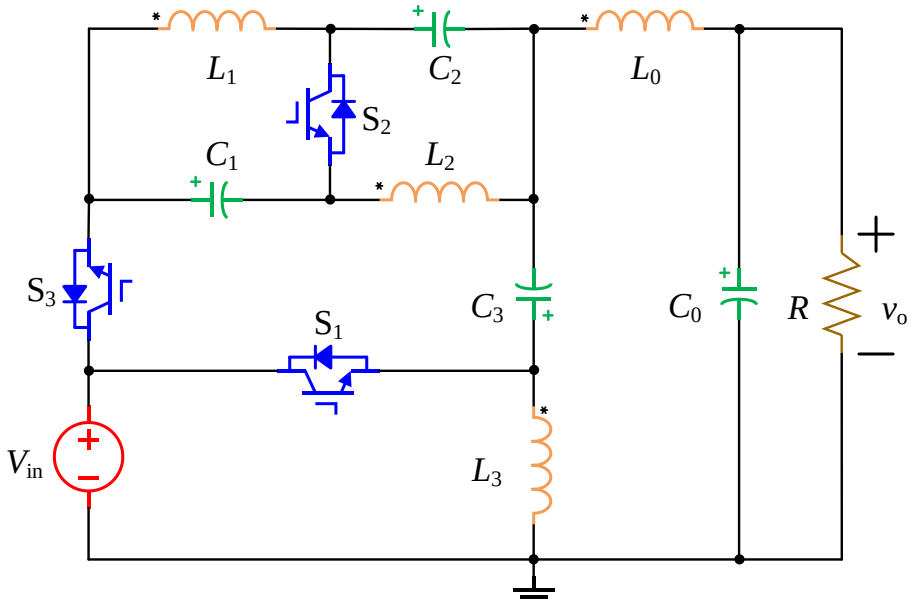


Figure 2. Proposed inverter.

The working state 1 is shown in Figure 3a. The switches S_1 and S_3 are turned on and S_2 is off. The input source charges the inductor L_3 and capacitor C_3 through the switch

S_1, and charges the inductor L_1, L_2 and capacitors C_1 and C_2 through S_3. According to Kirchhoff's law, the variables of working state 1 are expressed as follows:

$$\begin{cases} V_{L0} = V_{in} - V_{C3} - V_o \\ V_{L1} = V_{C3} - V_{C2} \\ V_{L2} = V_{C3} - V_{C1} \\ V_{L3} = V_{in} \end{cases} \tag{1}$$

$$\begin{cases} i_{C1} = i_{L2} \\ i_{C2} = i_{L1} \\ i_{C3} = i_{L0} - i_{L1} - i_{L2} \\ i_{Co} = i_{L0} - i_o \end{cases} \tag{2}$$

Working state 2 is shown in Figure 3b. At this time, the switches S_1 and S_2 are turned on and S_3 is off. The inductor L_3 is charged, while the capacitor C_3 is in the discharge state. The inductor L_1 and inductor L_2 are in the charging state, but the capacitance C_1 and C_2 are in the discharge state. According to Kirchhoff's law, the expressions of the variables of working state 2 are as follows:

$$\begin{cases} V_{L0} = V_{in} - V_{C3} - V_o \\ V_{L1} = V_{C1} \\ V_{L2} = V_{C2} \\ V_{L3} = V_{in} \end{cases} \tag{3}$$

$$\begin{cases} i_{C1} = -i_{L1} \\ i_{C2} = -i_{L2} \\ i_{C3} = i_{L0} \\ i_{C0} = i_{L0} - i_o \end{cases} \tag{4}$$

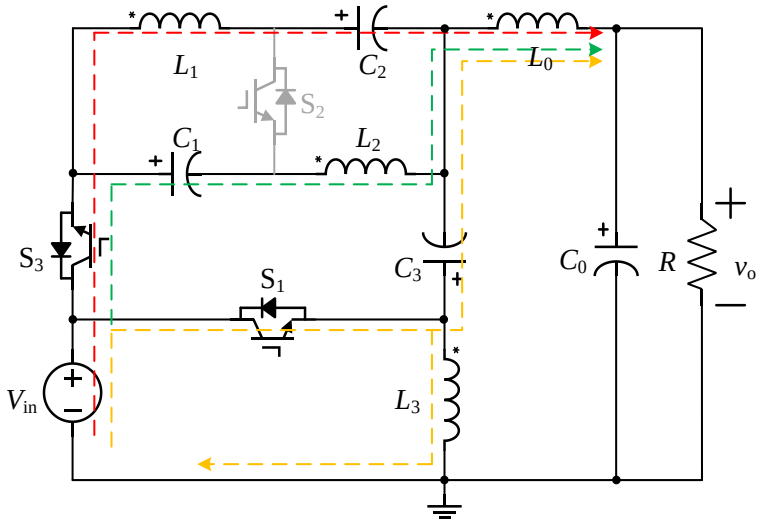
The working state 3 is shown in Figure 3c. The switches S_2 and S_3 are turned on, and S_1 is off. The capacitor C_1, C_2 and C_3 are in the discharge state. According to Kirchhoff's law, the expressions of the variables of working state 3 are as follows:

$$\begin{cases} V_{L0} = V_{in} - V_{C1} - V_{C2} - V_o \\ V_{L1} = V_{C1} \\ V_{L2} = V_{C2} \\ V_{L3} = V_{in} + V_{C3} - V_{C1} - V_{C2} \end{cases} \tag{5}$$

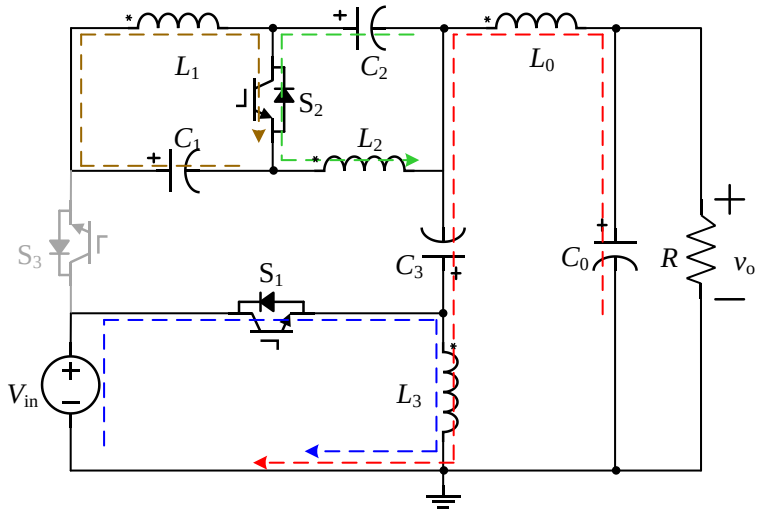
$$\begin{cases} i_{C1} = i_{L3} + i_{L0} - i_{L1} \\ i_{C2} = i_{L3} + i_{L0} - i_{L2} \\ i_{C3} = -i_{L3} \\ i_{Co} = i_{L0} - i_o \end{cases} \tag{6}$$

According to the above analysis, the corresponding relationship between input voltage V_{in} and the four capacitor voltages, output current i_o, and four inductor currents can be obtained. If the duty cycle of S_1 and S_2 is D_1 and D_2 respectively, the duty cycle of S_3 can be expressed as $2 - D_1 - D_2$. If the time of a working cycle is T_s, the running time from working state 1 to working state 3 is $(1 - D_2)T_s$, $(D_1 + D_2 - 1)T_s$ and $(1 - D_1)T_s$ respectively. Based on the volt-second principle, the corresponding relationship between inductor voltage and capacitor current is constructed as follows:

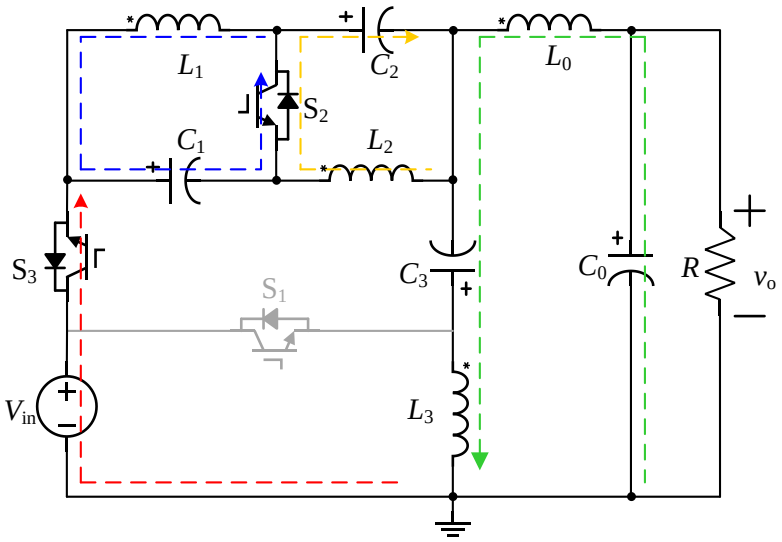
$$\begin{cases} \frac{V_o}{V_{in}} = \frac{V_{C0}}{V_{in}} = \frac{2D_2-1}{1-D_1} \\ \frac{V_{C1}}{V_{in}} = \frac{V_{C2}}{V_{in}} = \frac{1-D_2}{1-D_1} \\ \frac{i_{L0}}{i_o} = \frac{i_{L1}}{i_o} = \frac{i_{L2}}{i_o} = 1 \\ \frac{i_{L3}}{i_o} = \frac{D_1+2D_2-2}{1-D_1} \end{cases} \tag{7}$$



(**a**) working state 1



(**b**) working state 2



(**c**) working state 3

Figure 3. Operation modes of proposed inverter.

According to (7), the output voltage V_o is influenced by variables D_1 and D_2, and the maximum output range is mainly determined by the value of D_1. Hence, D_1 is set to an appropriate value to ensure that the output voltage can reach the expected range and that D_2 changes as sinusoid to produce a sinusoidal output voltage. For ease of analysis, define

$$\begin{cases} v_o = AV_{\text{in}} \sin \omega t \\ k = \frac{1}{1-D_1} - 2 \quad (D_1 > 0.5) \end{cases} \tag{8}$$

Among them, the peak gain A is equal to $V_{\text{omax}}/V_{\text{in}}$. V_{omax} is the maximum output voltage, and k is the maximum boost ratio. D_1 can be expressed as:

$$D_1 = \frac{k+1}{k+2} \tag{9}$$

By substituting (9) into (7), the new inverter voltage gain g can be obtained:

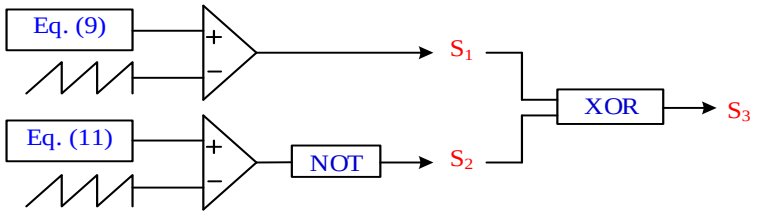
$$g = \frac{v_{\text{o}}}{V_{\text{in}}} = (k+2)(2D_2 - 1) \tag{10}$$

When D_1 is constant and (8) is substituted into (10), then D_2 can be expressed as:

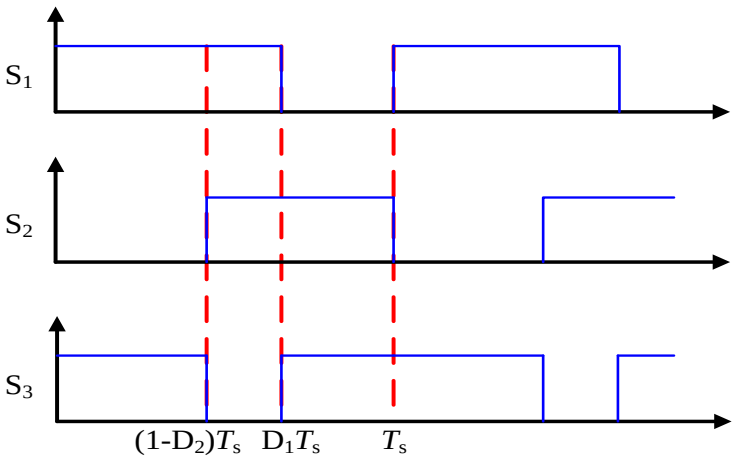
$$D_2 = \frac{1}{2} + \frac{A}{2(k+2)} \sin \omega t \tag{11}$$

According to (11) and (7), the duty cycle D_2 is changed by modulating A to control the output voltage v_{o} of the inverter.

The new topology modulation process is shown in Figure 4: First, D_1 is determined according to (9), and then D_1 and the carrier signal are input to the comparator at the same time to get the driving signal of switch S_1. D_2 is determined according to (11), then D_2 and the carrier signal are input to the comparator at the same time. After that, the driving signal of the switch S_2 is obtained through the NOT gate. Finally, the driving signal of S_3 is obtained by passing the driving signal of S_1 and S_2 through the XOR gate.



(**a**) modulation principle



(**b**) switching logic

Figure 4. Modulation strategy of proposed inverter.

3. Experimental Result

In order to verify the feasibility of the proposed method, a low power experimental platform of the new inverter was built. This system adopted digital control, in which DSP (TMS320F28335) is used to control the output voltage of the inverter, and FPGA (XilinxXC6SLX9) is used to generate three switch driving signals. The experimental parameters of the system are listed in Table 1.

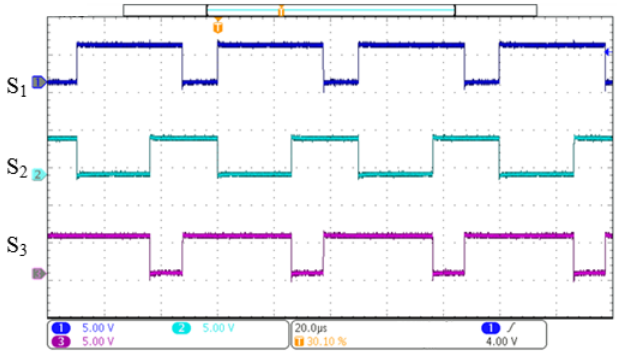
Table 1. Experimental parameters.

Parameters	Value
Input voltage	35 V
Inductor L_1	1.2 mH
Inductor L_2	1.2 mH
Inductor L_3	0.5 mH
Capacitor C_1	4.7 μF
Capacitor C_2	4.7 μF
Not-polarized capacitor C_3	4.7 μF
Switching frequency f_s	20 kHz
Inductor L_0	1 mH
Not-polarized capacitor C_0	9.4 μF
Load resistance	3.3 Ω
Output voltage	50 V
Output frequency	50 Hz

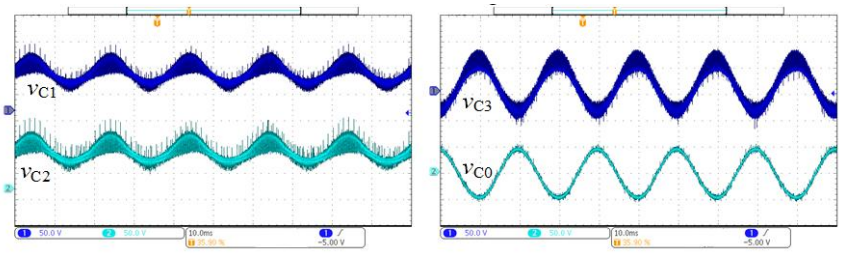
Figure 5a shows the experimental waveform of the switch drive signal, which is the driving logic signal of the switches S_1, S_2 and S_3 respectively from top to bottom. It can be seen that only two switches of S_1, S_2 and S_3 are turned on at the same time, which is in accordance with the theoretical analysis and design of Figure 4. Figure 5b demonstrates the experimental voltage waveforms of the capacitors C_1, C_2, C_3, and the output filter capacitor C_0 in the inverter topology. Due to the circuit impedance network being symmetrical, the voltage waveforms of capacitors C_1 and C_2 are the same. On the other hand, the C_3 and C_0 voltages are raised, which validates the boost ability of the circuit. It should be noted that spikes occur on vc1, vc2, vc3. The main reason behind it is the high-frequency interference from the measurement due to the high-frequency switching operation in the circuit.

Figure 5c shows the voltage and current waveforms of the impedance network inductors L_1, L_2, the boost inductor L_3, and the output filter inductor L_0 in the topology. According to the inductor voltage and current waveform, it can be seen that when the forward voltage is added at both ends of the inductor, the inductor is in the charging state, and the inductor current rises, which is consistent with the theoretical analysis. Figure 5d shows the output voltage v_o and current i_o waveform of the inverter. It can be seen that the proposed inverter can achieve sine wave output and boost ability at the same time. The total harmonic distortion of the output voltage is well below 5%, which meets the IEEE Std 519-2014. Therefore, the effectiveness of the proposed scheme is validated.

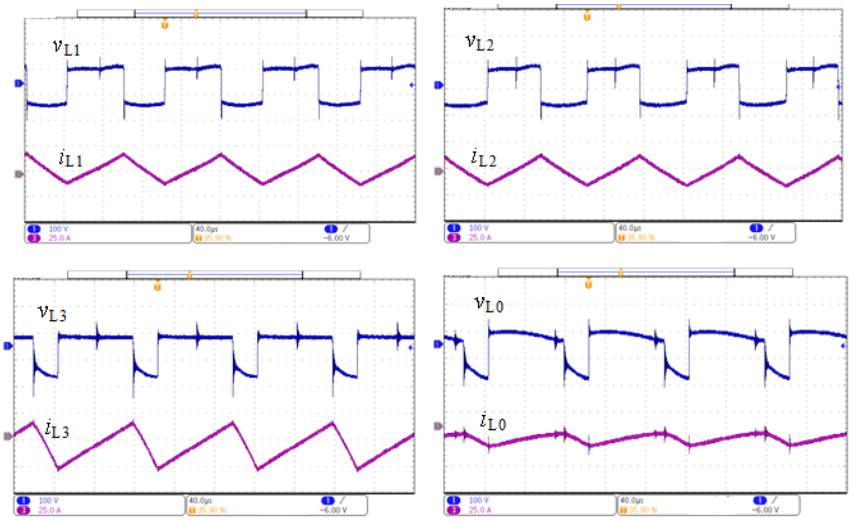
Table 2 shows the comparison analysis. The traditional inverters, such as H5, CH5 H6, and H8, have more switches, heat sinks and complicated isolated gating driver circuits. This all results in higher costs. On the other hand, the numbers of inductors and capacitors are more for the proposed inverters, however, they do not need the complicated isolated gating driver circuits and heat sinks. Also, with the high-frequency operation of the switches, the capacitor and inductors can be optimally reduced. Finally, the proposed inverter has the advantages of both boost capability and dual-grounded features, while others do not. Therefore, the proposed inverter is promising.



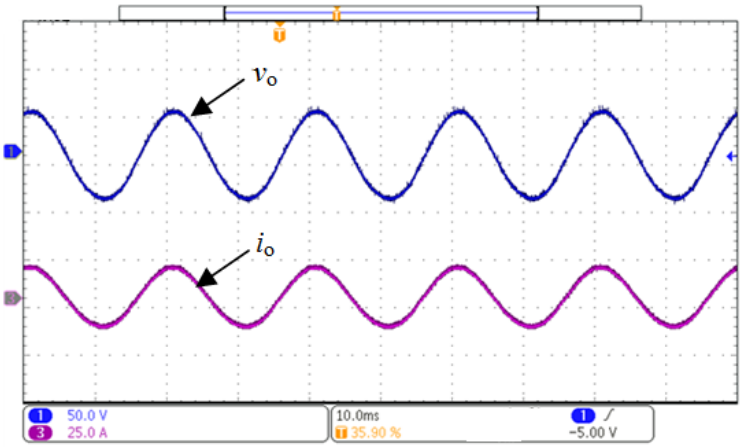
(**a**) switch logic signal



(**b**) the experimental voltage waveforms of the capacitors



(**c**) the voltage and current waveforms of inductors



(**d**) the output voltage and current waveform

Figure 5. Experimental results.

Table 2. Comparison analysis.

	H5 [7]	CH5 [8]	H6 [9]	H8 [10]	Proposal
Switch	5	5	6	8	3
Inductor	2	2	2	2	4
Capacitor	1	1	1	1	4
Boost capability	✗	✓	✗	✗	✓
Dual-grounded	✗	✗	✗	✗	✓

4. Conclusions

This paper has presented a novel topology and modulation strategy of a step-up inverter. The theoretical analysis was presented to verify the boost ability regarding the output voltage by controlling the duty cycle of the proposed circuit. The experimental results show that the proposed scheme has the advantages of less switching devices, boost ability and dual-grounded features. Also, the designed modulation strategy is simple to implement with the sinusoidal output voltage. Our future research is towards the extension of the proposed scheme to the three-phase non-isolated step-up inverter systems.

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Conflicts of Interest: The authors declare no conflict of interest.

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