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The Design of a Low Noise and Low Power Current Readout Circuit for Sub-pA Current Detection Based on Charge Distribution Model

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Abstract: In this article, we proposed an analytical model based on charge distribution for switched-capacitor trans-impedance amplifiers (SCTIAs). The changes in the load state of the amplifier under different operating conditions and the influence of the gain of the operational amplifier (Opamp) on the trans-impedance gain are analyzed to improve the design theory of switched-capacitor trans-impedance amplifiers. According to the conclusion drawn from the analysis, the trans-impedance amplifier (TIA) has been designed by adopting "correlated double sampling technology" and "cross-connection technology" to optimize input-referred noise current, power consumption, and trans-impedance gain. As a result, the trans-impedance gain reaches up to 206 dB, while the bandwidth is 3 kHz. The current readout system achieves an input-referred noise current floor of 2.96 $fA/\sqrt{Hz}$ at 1 kHz, and the power consumption of the system is 0.643 mW. The circuit has been simulated with the technology of 0.18 μm, and the layout area is 1000 μm × 500 μm.

Keywords: switched-capacitor; current readout circuit; trans-impedance amplifier; charge distribution; high gain; low noise; low power

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1. Introduction

With the development of science and technology, access to information has become more significant than before, and people are required to observe and detect various weak signals. Weak signal detection has a wide range of applications in many fields, such as chemistry, medicine, and food safety. In the measurement process, most methods convert the physical quantity into an electrical signal through the corresponding sensor for easy observation and analysis. The weak signal detection technology has also promoted the development of medical equipment and industrial production [1–4]. It is apparent that the development of weak signal detection technology prompts people to explore the laws of nature and develop high technology.

Sensors are applied to convert physical quantities into current signals that sometimes are too tiny to be detected by Analog to Digital Converter (ADC) directly. It is necessary to employ a trans-impedance amplifier (TIA) to convert and amplify the current signal for ADC [5]. The inserted buffer between the TIA and ADC ensures that the sampled signal is sufficiently accurate. Since the rapid development of digital signal processing, it is a reasonable choice to transmit the output of the ADC into processors like Microprogrammed Control Unit (MCU) or Digital Signal Processor (DSP) for further signal processing.

The general architecture of a weak current signal detection system is shown in Figure 1 [6].

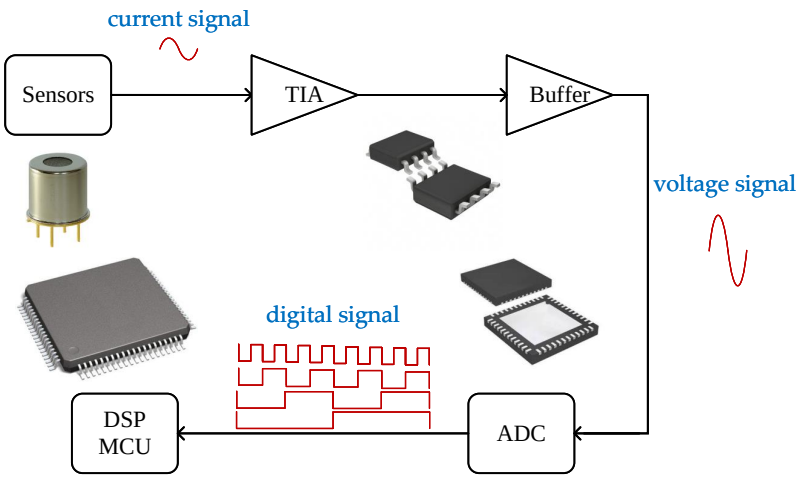


Figure 1. The architecture of the weak current signal detection system.

TIAs applied to detect the current signal produced by an input device, such as current type sensors, convert it into a voltage signal for further signal processing, and play more and more vital roles in weak current signal detection.

A classical structure of TIA adopting a simple resistor R_f between the input and output of an operational amplifier (Opamp) is unsuited for low noise and high gain application. The feedback resistor determines the current-to-voltage conversion factor (R_f) and the input-referred noise current ($4\,kT/R_f$) of the TIA, where k represents boltzmann constant and T stands for absolute temperature [7,8]. The requirement of high-value resistors (at the order of $G\Omega$) is difficult to be integrated for increasing trans-impedance gain (R_f) and decreasing input-referred noise current ($4\,kT/R_f$) [9]. Moreover, the resistor is limited by the gain-bandwidth product (GBW) of the Opamp as $R_f \leq GBW/(2\pi C_{in} BW^2)$ for stability [10].

Due to the difficulties of realizing resistive high-gain, low-noise TIAs, most state-of-the-art TIAs utilize pseudo-resistors and capacitors as the feedback elements [11–17].

Chuah and Holburn presented a resistive feedback TIA, utilizing a single PR as feedback element, which is operated in the linear region and tunable by an adjustable gate potential [15]. Therefore, the performance is very sensitive to process and temperature variations [16]. To mitigate the problems, Djekic proposed the use of a modified PR with enhanced linearity and robustness as resistive feedback element. However, the circuit needed to be manufactured in SOI CMOS process to greatly reduce parasitic capacitances [17].

A feedback capacitor replaces the resistor in the above structure as the feedback element. Since capacitors are regarded as elements with no noise, there are fewer noise sources in capacitive feedback type TIAs [18]. However, there is a fatal drawback in the topology of capacitive feedback TIA. The trans-impedance gain can be expressed as $1/(sC_f)$. Even a very tiny leakage current, generated by the sensors and regarded as direct current, will lead the Opamp to saturate [19].

Ferrari has proposed a topology of integrator-differentiator with dc feedback to avoid a direct current charge to the feedback capacitor. Since the structure of the dc feedback path has much negative feedback, stability is a challenge [9]. Another solution to solve the saturation of the Opamp is connecting a reset network between the input and output of the Opamp. The scheme has been proposed in [20], but the article ignored the effect of capacitative load during the process of current amplifying, and the load state, which is diverse in different working states of the TIA, was neglected as well.

It is necessary to analyze the transient behavior considering the charge distribution caused by the load capacitors and conclude the load states in different operating conditions

to optimize the trans-impedance gain and power consumption. As a supplement, the bandwidth (BW) of the switched-capacitor trans-impedance amplifier (SCTIA) and the influence of the Opamp on the trans-impedance gain are also analyzed to improve the previous work.

This paper is organized as follows. Section 2 gives a brief introduction to the SCTIA and analyzes the principle of correlated double sampling (CDS). In Section 3, an analytical model based on charge distribution is proposed, which gives a new viewpoint on the principle of SCTIAs. Section 4 shows the results and corresponding analysis, and Section 5 draws the conclusion.

2. Analysis and Design

2.1. The Architecture Design

Figure 2 shows the architecture of the current detection system. It consists of a TIA adopting switched-capacitors, CDS, digital circuit controlling switches, and a low noise buffer employed to improve the drive capability.

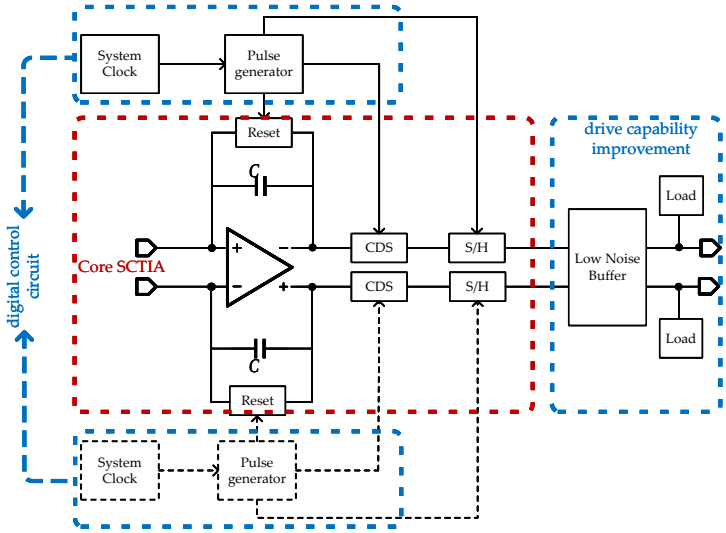


Figure 2. The schematic of the weak current detection system.

2.2. The Introduction to SCTIA

As present in Figure 3, the TIA contains a fully differential operational amplifier, several capacitors used for different functions, some switches, and a logic circuit used to control the switches and not displayed in the circuit diagram. All switches turn on (off) at high (low) voltage.

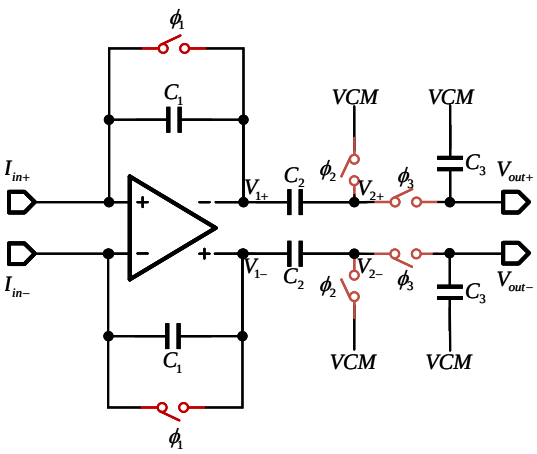


Figure 3. The schematic of the switched-capacitor trans-impedance amplifier (SCTIA).

The timing phase generated to control the switches should be appropriate to make the circuit work properly. This paper employs the timing phases as shown in Figure 4.

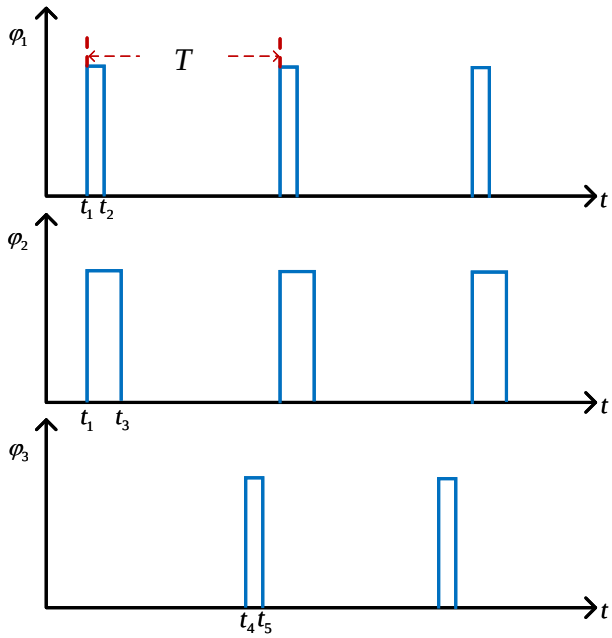


Figure 4. The diagram of timing phase.

As shown in Figure 4, there are three phases named φ_1, φ_2, and φ_3, which control the switches named ϕ_1, ϕ_2, and ϕ_3 in Figure 5, respectively. The working period is marked as T in Figure 4.

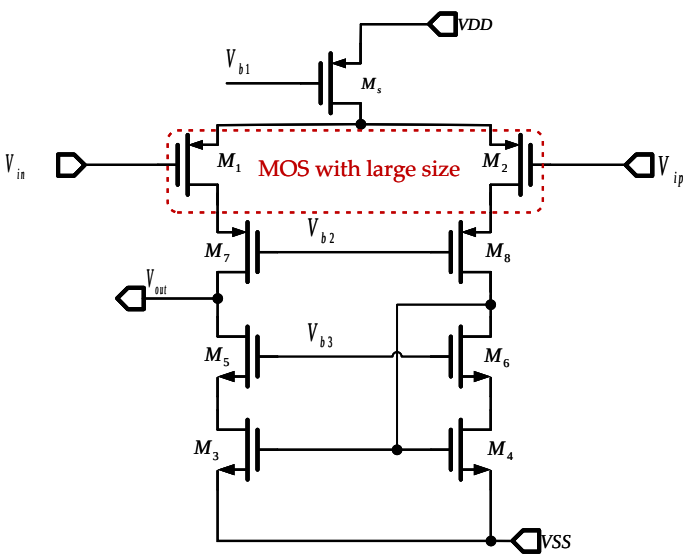
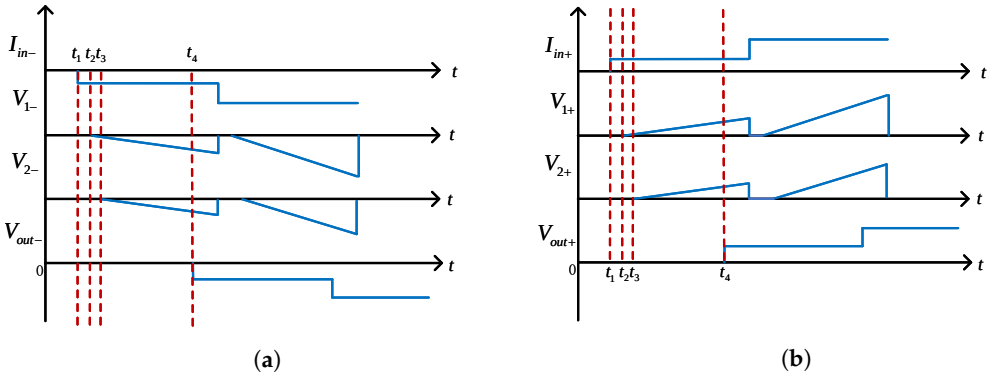


Figure 5. The schematic of telescopic cascade amplifier.

When ϕ_1 is on, the voltages of C_1 and C_2 are reset to zero so that there is no charge on C_1 and C_2. When ϕ_1 goes off at t_2, the input current begins to charge C_1, v_{1+}, and v_{1-} starts to rise (fall) or fall (rise) until the next period comes. After ϕ_2 is off at t_3, v_{2+}, and v_{2-} follow the change of v_{1+} and v_{1-}, respectively. Sample and hold circuit, consisting of a CMOS switch ϕ_3 and a sample capacitor C_3, is used to sample v_2 at the end of t_5 and hold the value until the next time when ϕ_3 is on. The brief waveforms of the node voltage of the TIA are shown in Figure 6 [20].



(**a**) (**b**)

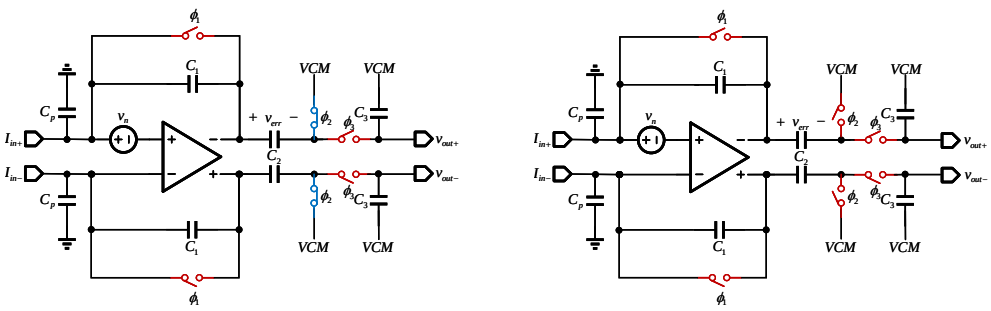
Figure 6. The brief waveform of the trans-impedance amplifier (TIA). (**a**) The waveforms depict the voltage of V_{1-},V_{2-},V_{out-} when the input current is displayed as I_{in-}. (**b**) The waveforms depict the voltage of V_{1+},V_{2+},V_{out+} when the input current is displayed as I_{in+}.

2.3. Correlated Double Sampling

The input-referred noise current is required to be small enough to make the TIA have the capability of detecting weak current signals.

Compared with the topology of resistive feedback, there is no resistor used in the structure of SCTIA, and then we can conclude the noise sources in the circuit. The noise sources of the TIAs are flicker noise, thermal noise of the operational amplifier, noise from the clock phase, and the shot noise caused by the leakage currents of the Electro-Static Discharge (ESD) protection diodes at the input of TIA, which is on the order of fA during regular operation. Since the transistors of switches work in the deep linear region, the clock noise is greatly reduced. Consequently, the noise from the Opamp usually dominates other noise sources. CDS is a technique commonly applied to reduce the noise of operational amplifiers, especially utilized for flicker noise and offset cancellation [20].

Signify the sum of the offset and low-frequency noise, principally flicker noise, as shown in Figure 7. To simplify the analysis, assume that v_n exists only at the positive port of the amplifier.



(**a**) (**b**)

Figure 7. The principle of correlated double sampling (CDS). (**a**) The switch state of the first stage of CDS; (**b**) The switch state of the second stage of CDS.

At the time of t_3 as shown in Figure 8, $v_n(t_3)$, denotes the voltage of v_n at t_3, is amplified by the operational amplifier and the amplification coefficient depends on the ratio of parasitic capacitance C_p and feedback capacitance C_1 and stored in C_2 as a voltage v_{err} across C_2.

It is effortless to get the expression of v_{err} as shown in the following.

$$v_{err}(t_3) = 1 + \frac{C_p}{C_1} v_n(t_3). \tag{1}$$

When all switches are off, charges stored in C_2 will not be variational for one end of C_2 connected to high resistance, like a floating state. Obviously, v_{1+}, at t_5 , can be expressed as

$$v_{1+} = v_{err}(t_5) + v_{si}(t_5). \tag{2}$$

$v_{si}(t_5)$ denotes the signal when noise is going to be omitted. Compared with a clock signal, the frequency of v_n is much smaller, for that v_n is mainly comprised of offset and flicker noise of the Opamp. Then it is reasonable to regard v_n as a constant in a single period so that the effect of offset and flicker noise at the output can be canceled through the above technology [21].

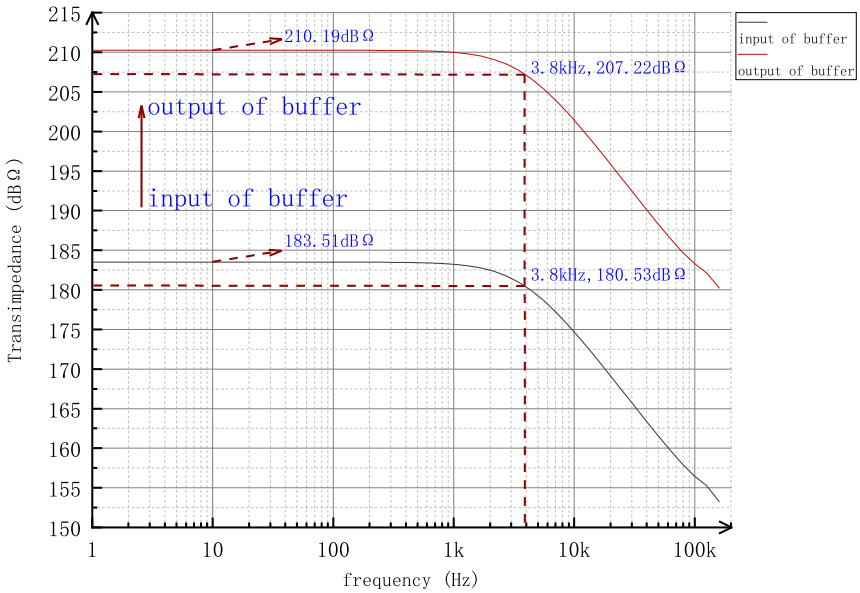


Figure 8. The comparison result of the frequency response of the input and the output of the buffer.

3. Detailed Analysis

3.1. The Charge Distribution Model

In the previous sections, we have introduced the working principle of TIA briefly. An analysis in detail of the circuit is needed to be carried out to guide the actual design. We can derive the equations which describe the working process according to the following analysis based on charge distribution.

When ϕ_1 is on, the input and the output of the Opamp are connected directly, and then the charge on the feedback capacitor C_1 and capacitor C_2 is zeroed. Compared with the branch of the capacitor, the output of the Opamp shows lower impedance, so the input current flows into the output stage of the Opamp through the feedback switch directly, then v_{1+} and v_{1-} are expressed below.

$$v_{1+} = 0, \tag{3}$$

$$v_{2+} = 0. \tag{4}$$

To simplify the analysis, the differential terminals v_{1-} and v_{2-} are omitted. The same goes for the following analysis. Since the sampling switch is not closed, v_{out+} remains unchanged as a value as the previous period v_{out+} was.

When ϕ_1 is off and ϕ_2 is still on, the input current will charge C_1. At the moment switch ϕ_1 is off, feedback capacitor C_1, which was originally shorted, is connected to the circuit, and then the load state of the operational amplifier will change. The voltage of the input and output of the amplifier will not mutate for both the charge stored in C_1 and C_2 at the moment before and after the switch ϕ_1 is off is zero.

An Opamp has the character of a virtual short circuit and virtual open circuit for its high gain and high input impedance. As a result, the input current flow from the input node to the output node of the amplifier through the feedback capacitor will not make the voltage of the input node of the amplifier change. According to the relationship between voltage and current of the capacitors, the voltage of C_1 can be expressed as

$$u_{c_1}(t) = \frac{1}{C_1}\int_{t_2}^{t} i_{in}(t)dt + u_{c_1}(t_2). \tag{5}$$

where $t_2 \leqslant t \leqslant t_3$,$u_{c_1}(t_2) = 0$.

Compared with the period of the clock, the period of the input current is longer. As a result, it is reasonable to regard the input current $i_{in}(t)$ as a constant I_{in}, so that the above expression can be simplified as

$$u_{c_1(t)} = \frac{t - t_2}{C_1} I_{in}. \tag{6}$$

That $t_2 \leqslant t \leqslant t_3$ is assumed. The voltage of the output of the Opamp varies linearly concerning the input current over time. Since the voltage of the output of the amplifier has changed, and another port of capacitor C_2 is connected to VCM, current will flow through capacitor C_2, whose value depends on the rate of change of the output voltage of the Opamp. According to the expression of $u_{c_1}(t)$, the current which flows through capacitor C_2 can be calculated below.

$$i_{C_1} = C_2\frac{du_2}{dt} = C_2\frac{I_{in}}{C_1}. \tag{7}$$

According to Kirchhoff's Current Law (KCL), the output current of the Opamp is required to be larger than the sum of current flowing through the capacitor C_1 and capacitor C_2.

When ϕ_1, ϕ_2, ϕ_3 all are off, the port of capacitor C_2 connected to switch ϕ_3 is considered to be in a high resistance state, as a consequence, there is no current flow through capacitor C_2, so that the voltage of the two ports of C_2 do not change, v_2 is going to change as v_1 changes.

The expression of v_{1+} and v_{2+} can be derived as follows when $t_3 \leqslant t \leqslant t_4$.

$$v_{1+} = \frac{1}{C_1}\int_{t_2}^{t} i_{in+}(t)dt + u_{c_1}(t_2), \tag{8}$$

$$v_{2+} = \frac{1}{C_1}\int_{t_3}^{t} i_{in+}(t)dt. \tag{9}$$

Assuming that the output voltage of the TIA is $V(nT - T)$ at the end of the last cycle, as a result, charges stored in capacitor C_3 at t_{4-} can be expressed as

$$Q_{C_{31}} = V(nT - T)C_3. \tag{10}$$

During the phase when ϕ_1 is off, and ϕ_2 is on, charges stored in C_2 at t_{4-} can be derived as

$$Q_{C_{21}} = i_{in}(t_3 - t_2)C_3. \tag{11}$$

That t_{4-} denotes the moment before ϕ_3 is on.

The voltage of a capacitor does not change dramatically since C_1 is connected across the input and output of the Opamp, which means that the voltage at the node where the C_1 is connected to the input of the Opamp remains zero.

Suppose that the final stable output at the end of the period is $V(nT)$, and $V(nT) > V(nT - T)$. According to the analysis above, we can derive v_2 as

$$v_2 = \frac{I_{in}}{C_1}(t_4 - t_3). \tag{12}$$

The charging process when the switch ϕ_3 is on is analyzed separately to simplify the analysis. As a result, the voltage across C_1 is regarded as constant during the process of charge redistribution between C_2 and C_2.

Given the assumption of $V(nT) > V(nT - T)$, the charge will be transferred from capacitor C_2 to capacitor C_3 when the redistribution of charge happens. In other words, v_1 will drop sharply, and then v_1 will drop sharply as well. The voltage of the input of the Opamp connected to capacitor C_1 changes in the same way as v_1. Through the adjustment of the feedback of the Opamp, the input voltage of the amplifier will change to zero, and the output voltage of the amplifier will return to $I_{in}/C_1(t_4 - t_2)$, during the above process, the charge is transferred.

Before and after the transfer of charge, the amount of charge is conserved, so the charges stored in capacitor C_2 and C_3 have the relationship as follows.

$$(V(nT) - \frac{i_{in}(t_4 - t_2)}{C_1})C_2 + V(nT)C_3 = (V(nT - T))C_3 + \frac{i_{in}(t_3 - t_2)}{C_1}C_2, \tag{13}$$

$$V(nT) = V(nT - T)\frac{C_3}{C_2 + C_3} + \frac{C_2}{C_1(C_2 + C_3)}i_{in}(t_4 + t_3 - 2t_2). \tag{14}$$

For the assumption of $V(nT) > V(nT - T)$, we can define $V_{nT-T} = \alpha V_{nT}$, where $0 < \alpha < 1$, so that the trans-impedance gain of the TIA can be derived as

$$\frac{V(nT)}{i_{in}} = \frac{C_2}{[C_2 + (1 - \alpha)C_3]C_1}(t_4 + t_3 - 2t_2). \tag{15}$$

3.2. Equivalent Load Capacitance

In order to optimize the power consumption, it is necessary to know the load state of the Opamp at each phase. Figure 9 is the different working states of the TIA. In separate circuit states, capacitors connected to the output of the Opamp are dissimilar. According to the method concluded in [22], the equivalent load capacitances of the Opamp at different phases are expressed below.

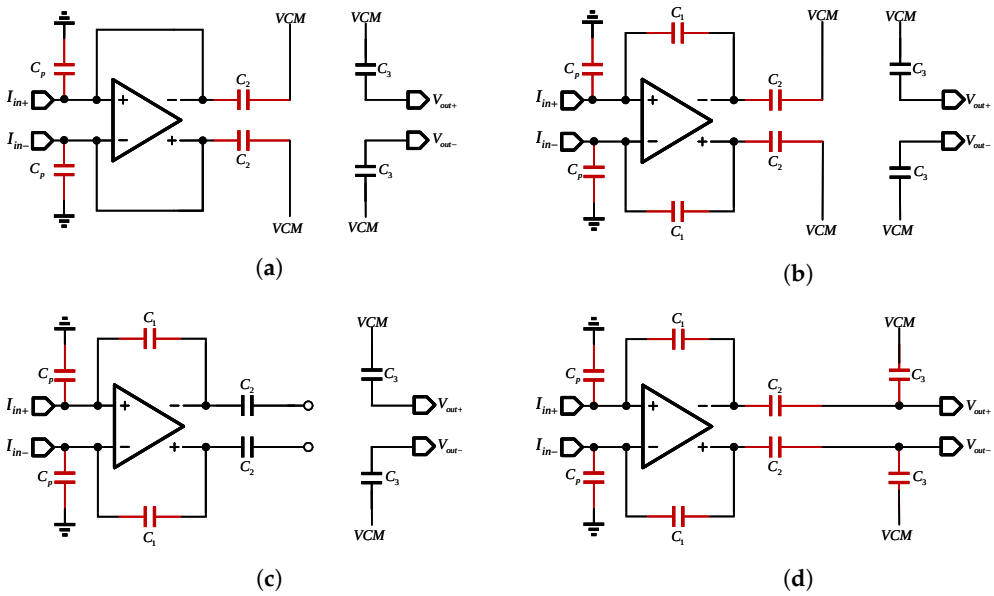


Figure 9. The different working states of the TIA. (**a**) The working state when $t_1 < t < t_2$; (**b**) The working state when $t_2 < t < t_3$; (**c**) The working state when $t_3 < t < t_4$; (**d**) The working state when $t_4 < t < t_5$.

$$C_{eqa} = C_p + C_2, \tag{16}$$

$$C_{eqb} = C_p + C_2(1 + C_p/C_1), \tag{17}$$

$$C_{eqc} = C_p, \tag{18}$$

$$C_{eqd} = C_p + (C_2//C_3)(1 + C_p/C_1). \tag{19}$$

According to the equations above, it is clear that when ϕ_2 is on and ϕ_1 is off, the load capacitance of the Opamp is the largest.

3.3. Analysis of Bandwidth

Different from the analysis in conventional circuit structures, it is hard to analyze the bandwidth in SCTIAs accurately, but the factors affecting the bandwidth can be obtained through qualitative analysis.

Because of switch capacitors, there is a hypothesis about the trans-impedance gain—that the input current is regarded as a constant in a complete working period in the above analysis. To satisfy the assumptions, the bandwidth of the TIA is far less than the frequency of a complete working cycle.

As a consequence, we can improve the bandwidth of the TIA through the method of increasing the frequency of the system clock, which will decrease the charging time of capacitor C_1 in a single cycle, the trans-impedance gain will decline. In addition, the time when switch ϕ_1 is closed becomes shorter, and the power consumption of the Opamp is required to be higher to meet the quick setting up under the condition of unit feedback. Therefore, the system clock should be reasonable according to the trade-off of power, bandwidth, and trans-impedance gain.

In addition to a constraint on bandwidth from the system clock, the pole generated by the equivalent resistance and the input capacitor also has an impact on the bandwidth. Since the frequency of this pole is relatively high, it is generally not taken into account when the requirement of bandwidth is low.

3.4. Analysis of Leakage Current

In the sub-pA current detection circuit, the leakage current needs to be concerned. In CMOS technology, it is considered that leakage of PN junction and leakage of MOS operating in the sub-threshold region are the primary leakage current in the circuit [23].

The leakage current of the PN junction is caused by the drift of minority carriers at the edge of the depletion region and the recombination of electron–hole pairs in the depletion region. Generally, the leakage current of PN junction in 0.18 µm CMOS technology is in the order of $aA/\mu m^2$, which is a low leakage current level in the CMOS circuit [24,25].

The leakage current of MOS operating in the sub-threshold region is generated by the channel between source and drain when the gate-source voltage is less than the threshold voltage, which is mainly determined by the diffusion of carriers [26].

Some secondary effects of MOS, such as DIBL (Drain Induced Barrier Lowering), body effect, and threshold voltage roll-off, will affect the threshold of MOS and then influence the sub-threshold leakage current of MOS [27]. DIBL often occurs in small size devices because of the decrease in channel length, increasing the voltage at the drain. The source and drain depletion zone will close together. As a result, the number of electrons injected into the channel from the source will increase, resulting in an increase in leakage current. It is obvious that we can increase the length of the MOS to reduce the effect of DIBL on leakage current. Body effect is caused by different potentials of bulk and source, and it will change the threshold voltage of the MOS. It is a good method to take advantage of the body effect to increase the threshold voltage of the MOS and then decrease leakage current [28]. Threshold voltage roll-off is caused by short channel length as DIBL. The typical sub-threshold leakage current of MOS is several decades fA of orders [29].

3.5. Effects of the Operational Amplifier on TIA

It is obvious to be seen from the above analysis that we can converse current signal to voltage signal because of the charging of the feedback capacitor C_1. It is necessary to

analyze the transient process when considering the influences of the Opamp, for the reason that the amplifier is the core element in the TIA.

The following equations hold at both the input and output of the Opamp.

$$I_{in}(t) = I_1(t) + I_2(t), \tag{20}$$

$$-V_{in}(t)A = V_{out}(t), \tag{21}$$

$$V_{out}(t) - V_{in}(t) = \frac{1}{C_1} I_2(t)(t-0), \tag{22}$$

$$V_{in}(t) = -\frac{I_1(t)t}{C_p}. \tag{23}$$

where $I_{in}(t)$ is the input current, $I_1(t)$ is the current flowing through the parasitic capacitor C_p, $I_2(t)$ is the current flowing through the feedback capacitor C_2, $V_{in(t)}$ is the voltage at the input of the Opamp, and $V_{out}(t)$ is the voltage at the output of the Opamp, all are shown in Figure 10. According to above equations, the relationship between $V_{out}(t)$ and $I_{in}(t)$ can be derived as follows.

$$\frac{V_{out}(t)}{I_{in}(t)} = \frac{t}{C_1} \frac{1}{1 + 1/A + C_p/(AC_1)}. \tag{24}$$

The gain of the Opamp A is required to be large enough to avoid the influence of the parasitic capacitor on trans-impedance gain.

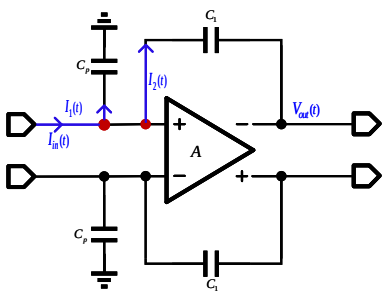


Figure 10. Schematic of the resistive feedback TIA describing the noise performance

Compared with telescopic cascade and two-stage amplifier, folded cascade amplifier has a better trade-off in power consumption and output swing. In this design, we adopt the structure of folded cascade amplifier, and the diagram is shown in Figure 11. Compared with NMOS, PMOS has lower flicker noise because the probability of capturing and releasing carriers is much smaller. Therefore, it is reasonable to choose PMOS as the input MOS of the amplifier.

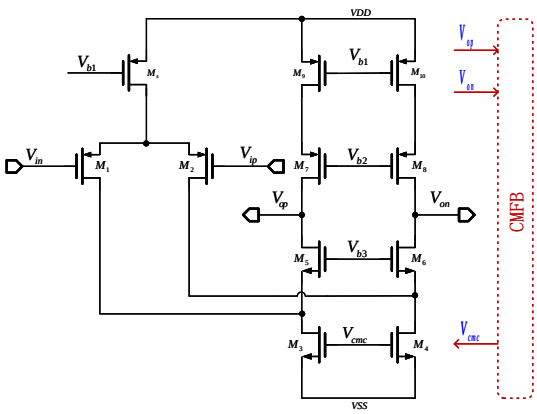


Figure 11. The schematic of fully differential folded-cascade amplifier (CMFB is not displayed).

3.6. Buffer Design

The TIA has a poor ability to drive load since its output is capacitive. Therefore, the TIA needs to be connected to an appropriate buffer to drive a load. In this paper, cross-connection technology is adopted to design a fully differential buffer with high input impedance and low output impedance based on telescopic operational amplifiers. The structure of the buffer is shown in Figure 12.

The relationship between the output and the input of the buffer can be derived as follows [30].

$$\frac{V_{out}}{V_{in}} = 2 \times (\frac{R_1}{R_2} - \frac{R_1}{R_3}). \tag{25}$$

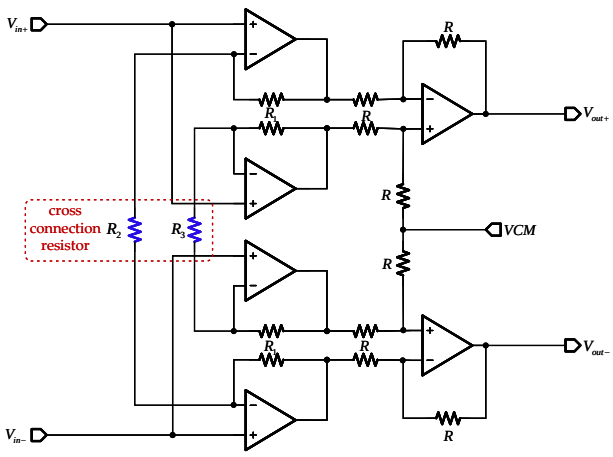


Figure 12. The schematic of the low noise buffer.

To reduce the overall power consumption, Opamps adopting a telescopic cascade structure, as shown in Figure 5, are applied to build the low noise buffer. For the reason that there are sampling capacitors at the output of the core TIA, the signal at the output will change due to the effect of clock feedthrough and charge injection of switches if low noise technology like chopper or auto-zero is adopted to reduce input-referred noise voltage of buffer. As a result, it is necessary to increase the size of the input MOS of the buffer to achieve the requirement of low noise, as described in Figure 5.

4. Result and Analysis

The frequency response and noise performance of the TIA have been simulated. We can obtain the periodic operating point of the TIA through "Periodic Steady State" (PSS) analysis. After PSS is completed, "Periodic Alternating Current" (PAC) analysis computes the frequency response of the TIA, and "Periodic Noise" (PNOISE) analysis is run to find out its noise behavior.

That shown in Figures 13 and 14 are the results representing the gain of the input and output nodes of the buffer.

Low-frequency trans-impedance gains as high as 206 dB with a 3 kHz–3 dB bandwidth at the output node of the buffer and 183 dB with a 3 kHz bandwidth at the input node of the buffer have been simulated in the worst case from the result. This shows that the gain of the in-band signal is very high, and the designed current readout circuit has a good ability to amplify the tiny current.

The curves of the frequency response are shown in Figure 8 under the condition of 27 °C and "typical–typical" (tt) process corner to facilitate the comparison of the input and output gains of the buffer. The gain is observed to increase from 183.51 dBΩ to 210.19 dBΩ, indicating that the buffer could improve the ability to drive loads and enhance the gain of the trans-impedance amplifier.

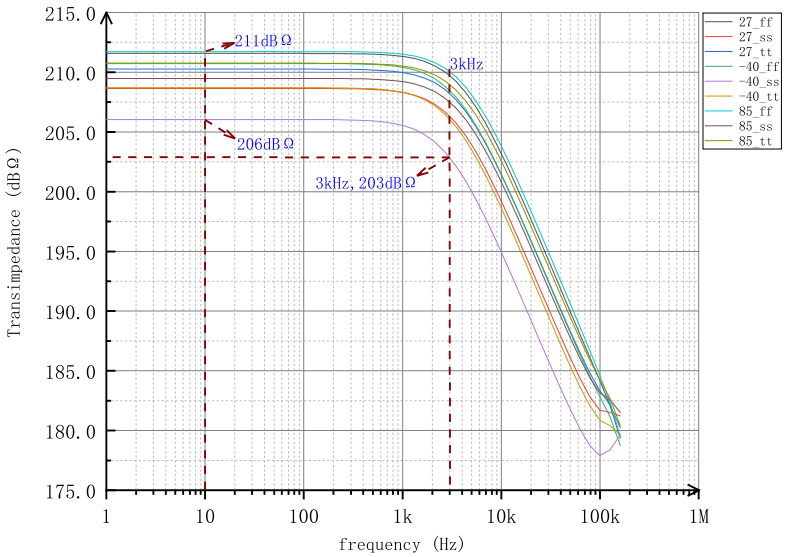


Figure 13. Frequency response of the complete system.

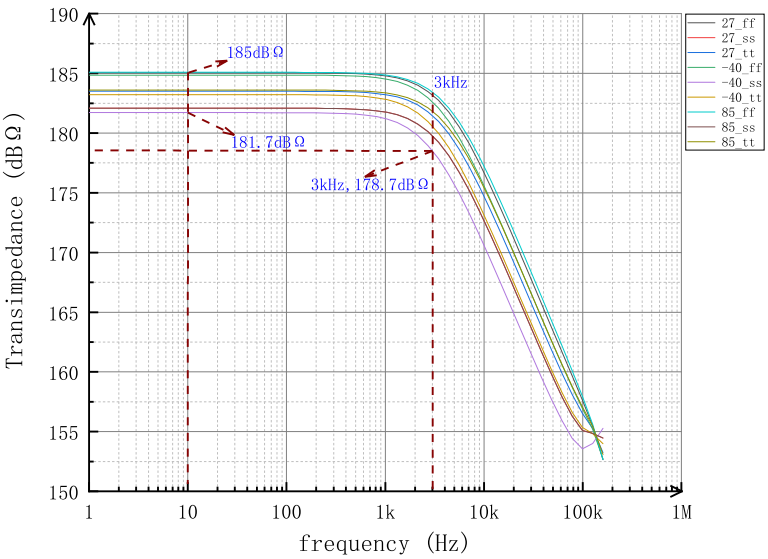


Figure 14. Frequency response of the input node of the buffer.

Figure 15 displays the input-referred noise voltage of the buffer. In this paper, the low-frequency input-referred noise voltage of the buffer is decreased through the increasing size of the input *MOS*. As shown in the result, input-referred noise voltage of 33.143 nV$\sqrt{Hz}$ at 1 kHz has been achieved regardless of process and temperature variation.

That shown in Figure 16 is the performance of the input-referred noise current of the TIA. A low input-referred noise current of 2.69 $fA/\sqrt{Hz}$ is achieved. Its noise performance ensures that the current readout circuit can amplify the weak current in the band effectively without introducing too much noise.

That shown in Figure 17 is the layout of the complete system, and all sub-circuits have been marked on the layout.

A comparison result of the performance of the published circuits in recent years is shown in Table 1.

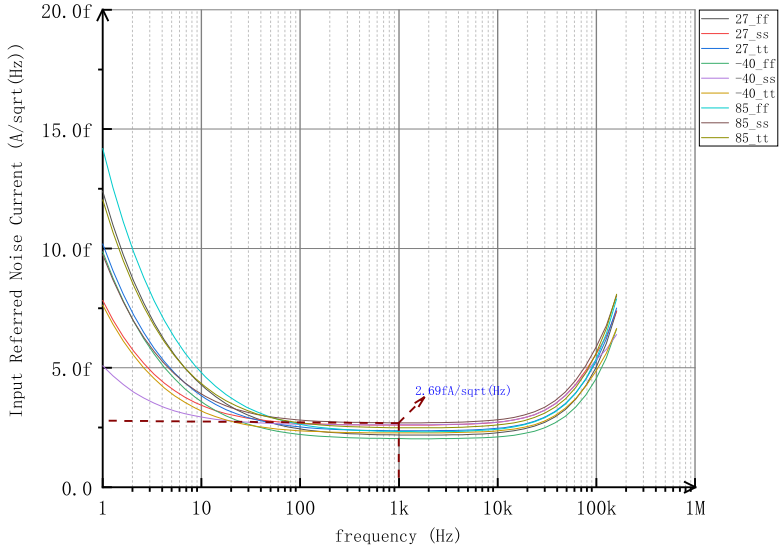


Figure 15. Noise performance of the TIA.

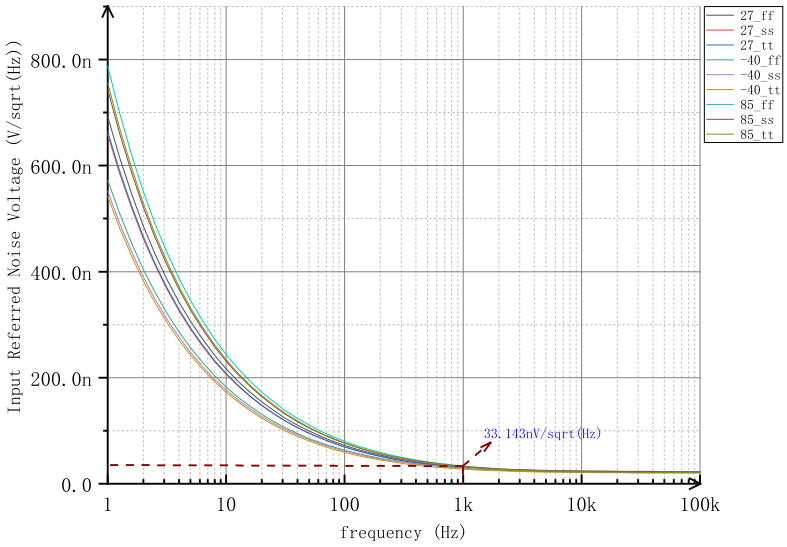


Figure 16. Noise performance of the low noise buffer.

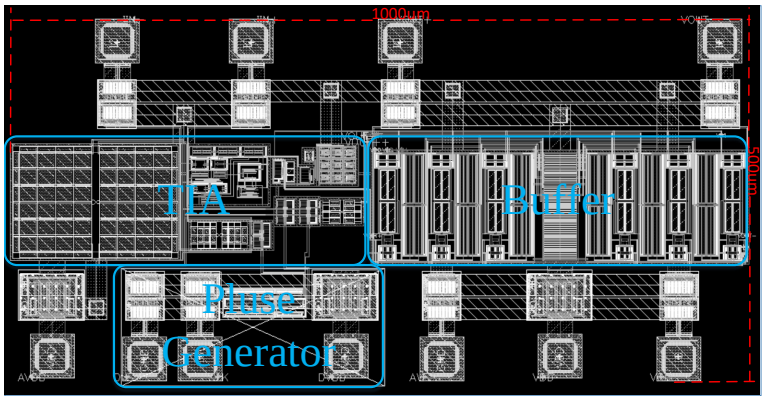


Figure 17. The layout of the TIA with buffer.

Table 1. The comparison result of the performance of circuits. CT represents continuous type, DT represents discrete type.

	This Work	IEEE J. Solid State Circuits [11]	ISCAS [31]	Sensors [20]	CoDIT [32]	IEEE J. Solid State Circuits [33]	Electronics [34]	IEEE J. Solid State Circuits [35]
Bandwidth/MHz	3×10^{-3}	4	1	4×10^{-2}	**10**	1×10^{-3}	0.555	2
Input referred noise/$fA\sqrt{Hz}$	**2.69**	4	27	25	500	–	390	140
DC gain/dBΩ	**206**	153	148.9	158	104.1	148	124	120
Power/mW	0.643	45	2.71	3.2	0.71	0.4	**0.0361**	9.5
Technology	0.18	0.35	0.18	0.35	0.18	0.6	0.18	0.18
Circuit Type	DT	CT	CT	DT	CT	DT	CT	CT
Result	Simulated	Measured	Simulated	Measured	Simulated	Measured	Simulated	Measured

From the comparison result, it is apparent that CT-TIAs (Continuous type trans-impedance amplifiers) [11,13,31,35] reach the MHz bandwidth, while DT-TIAs (Discrete type trans-impedance amplifiers) [20,33], including the design in this paper, are limited in bandwidth by system clock as analyzed in Section 3.3.

According to the conclusion drawn from the charge distribution model and equivalent load capacitance, the trans-impedance gain and power consumption of the design have been optimized.

This work has advantages in the performance of gain and power consumption compared with the previous work displayed in Table 1, so it is suitable for low-noise and low-power application scenarios with the relaxed bandwidth requirement, such as the current process in ECG, EGG, NIRS, and DNA analysis [36–38].

5. Conclusions

Building on previous work, in order to analyze the factors affecting the trans-impedance gain of SCTIAs accurately, the analytical model of charge distribution proposed improves the analysis theory of SCTIAs. Grounded on the proposed model, combined with the analysis of load states and effects on the trans-impedance gain of the Opamp, the designed circuit achieves a trans-impedance gain as high as 206 dB with 3 kHz bandwidth and 0.643 mW power consumption. Its input-referred noise current is as low as $2.69 fA/\sqrt{Hz}$ at 1 kHz. The simulation results show that the model is referential on low power and high gain TIAs. The detailed analysis process helps technical personnel, engineers, and researchers specializing in TIAs to design high-performance current readout circuits.

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Abbreviations

The following abbreviations are used in this manuscript:

ADC	Analog to Digital Converter
MCU	Micro Control Unit
DSP	Digital Signal Processor
TIA	Transimpedance amplifier
SCTIA	Switched-capacitor transimpedance amplifier
Opamp	Operational amplifier

GBW	Gain-Bandwidth product
CDS	Correlated double sampling
ESD	Electro-Static Discharge
KCL	Kirchhoff's Current Law
CT-TIAs	Continuous type trans-impedance amplifiers
DT-TIAs	Discrete type trans-impedance amplifiers
PSS	Periodic Steady State
PAC	Periodic Alternating Current
PNOISE	Periodic Noise

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