electronics

MDPI

Article

Design of Capacitor-Less High Reliability LDO Regulator with LVTSCR Based ESD Protection Circuit Using Current Driving Buffer Structure

Sang-Wook Kwon and Yong-Seo Koo *

Department of Electronics and Electrical Engineering, Dankook University, Yongin-si 16890, Korea; kso804@naver.com

* Correspondence: yskoo@dankook.ac.kr

Abstract: The peak voltage depending on the load current can be affected by the external capacitors installed in the output stage of the LDO regulator. However, the capacitor-less LDO regulator proposed in this study was applied a current driving buffer structure between the output stage of the error amplifier and the path transistor. Therefore, the proposed LDO regulator maintained a stable output voltage regardless of the load current by controlling an effective overshoot/undershoot voltage. In addition, the proposed LDO regulator has a built-in LVTSCR based on the ESD protection circuit. As most IC circuits are malfunctioned and destroyed by the ESD phenomenon, the reliability was verified through the built-in ESD protection circuit of the proposed LDO regulator. The proposed LDO regulator with the current driving buffer structure can effectively control the peak voltage. As a result of the measurement, the undershoot voltage of 22 mV and the overshoot voltage of 19 mV were maintained when the load current of 250 mA was provided under the conditions of 3.3 V to 4.5 V and the output power voltage of 3 V. The proposed ESD protection circuit is also guaranteed to function at temperatures as high as 500 K.

Keywords: capacitor-less LDO; ESD protection; load transient response; current buffer structure; SCR based ESD protection; LDO regulator; high reliability LDO regulator

Citation: Kwon, S.-W.; Koo, Y.-S. Design of Capacitor-Less High Reliability LDO Regulator with LVTSCR Based ESD Protection Circuit Using Current Driving Buffer Structure. *Electronics* **2022**, *11*, 1781. https://doi.org/10.3390/electronics11111781

Academic Editor: Alina Caddemi

Received: 13 May 2022
Accepted: 1 June 2022
Published: 3 June 2022

1. Introduction

The reliability and stable voltage supply in integrated circuits are indispensable. Reliability must be guaranteed to operate normally due to the external environment and Electrostatic Discharge (ESD) phenomenon along the high integration of the semiconductor process. If the destruction of IC occurs because of the ESD situation, the stable operation of IC may not be guaranteed. Therefore, the output voltage must be provided a constant voltage regardless of the load voltage or current. As the weight of mobile devices is decreasing day by day, the size of the battery is getting smaller, but the power consumption of the battery tends to increase continuously. In particular, it is impossible for mobile devices to operate normally without a supply of stable power. Therefore, the power in a battery with a limited capacity must be continuously managed by a power management integrated circuit (PMIC). The Low Drop-Out (LDO) regulators are an indispensable component for IC management [1–7]. In addition, the LDO regulator with low noise and stable voltage drive is an important factor to consider in the circuit design. The voltage and the load current of a LDO regulator must be controlled to provide the output voltage required in the various blocks, as shown in Figure 1. However, the load current required by the system may be rapidly increased or decreased by the non-uniform input. Therefore, it is essential for the LDO regulator to provide a stable peak voltage regardless of the load current. The peak voltage formed steadily by the LDO regulator can affect the adjacent systems. Therefore, the LDO regulators must always provide a constant output voltage regardless of load current [8–10]. Also, the conventional LDO regulators used to achieve

this purpose have large external capacitors. Of course, the presence of an external capacitor affects the stability of the LDO regulator due to the output voltage varying with the load current. However, the LDO regulator, which has replaced the function of the external capacitor with a chip, has great advantages in the view of economy and space utilization. In order to take advantage of them, studies are being actively conducted to effectively implement the function of the LDO regulator without an external capacitor. This study was carried out to propose a current-driven buffer structure that can effectively control the peak voltage generated by mobile devices without an external capacitor. Conventional LDO regulators typically control the momentary changes in the load current into the single feedback. However, the proposed LDO regulator has added the feedback loop to effectively control the peak voltage in response to the load current. In other words, the LDO regulator can be effectively controlled at the output node by additionally supplying or discharging the current through the feedback loop according to the instantaneous change in the load current. Namely, the LDO regulator with an additional feedback loop can control the load current by the gate node of the pass transistor. Therefore, the proposed LDO regulator was designed to supply and discharge the current through an additional feedback path with the current driving buffer structure [11–17]. IC circuits of miniaturized and highly integrated semiconductor devices cannot be operated normally by the electrostatic discharge (ESD). The ESD is released by direct contact with a machine or human body and causes damage and malfunction through the external pins. Therefore, it is essential to consider the ESD protection circuit. Diodes are widely applied because they have a very simple structure and are easier to implement than other ESD protection circuits. However, recently, it has been determined that SCR with a current driving capability superior to the diode is suitable as an ESD protection circuit of an internal IC because of the high integration of semiconductors and the fineness of the process. The reason why diodes are not mainly used as an ESD protection circuit is that the turn-on voltage of the diode is very sensitive to temperature, and thus is vulnerable to temperature. In addition, the diode with a certain area has poor current driving capability. In order to solve these problems, the proposed ESD protection circuit is embedded in the proposed LDO regulator to ensure high reliability due to the high integration of semi-conductors and process refinement. The ESD protection circuit proposed in this paper is a Low Voltage Trigger Silicon-Controlled Rectifier (LVTSCR) ESD protection circuit that has improved the conventional Silicon-Controlled Rectifier (SCR) structure. The LVTSCR ESD protection structure has improved electrical properties to effectively prevent ESD surge at a low voltage. The proposed LDO regulator has built in an LVTSCR-based ESD protection circuit to secure the high reliability of the IC circuit [18–24]. The proposed LDO regulator using the current driving buffer structure was secured reliably by applying ESD surge to POWER CLAMP and I/O CLAMP, and then the output voltage was verified.

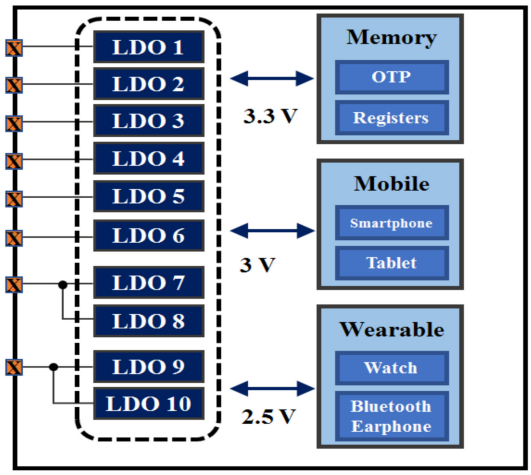

Figure 1. PMIC (Power Management Integrated Circuit) block.

2. The Proposed LDO Regulator with ESD Protection Structure

2.1. Current Driving Buffer Structure

Figure 2 shows a proposed LDO regulator with a current driving buffer structure. The proposed LDO regulator has a current driving buffer structure to provide additional feedback paths depending on the load current. The output node of the LDO regulator must always supply a stable voltage regardless of the load current. As shown in Figure 3, the current driving buffer structure has the function of increasing the voltage of the output node while decreasing the voltage of the pass gate node for an undershoot state in which the output voltage drops. Thereby, the output voltage reduced by the load current can be increased. Therefore, an additional current discharge path may be formed at the gate terminal of the pass transistor. In addition, the proposed LDO regulator provides additional current to the output nodes through MOSFET detection. The result is a current path that can effectively supply and discharge the additional current in an undershoot condition. The current driving buffer structure has a function of increasing the gate node voltage of the pass transistor while decreasing the rising voltage due to the load current for an overshoot condition in which the output voltage increases as shown in Figure 4. Thereby, the rising voltage due to the load can be reduced. Therefore, an additional current supply path was formed at the gate terminal of the pass transistor. In addition, the proposed LDO regulator discharges the additional current to the output nodes through the MOSFET detection. The capacitor-less LDO regulator without an external capacitor is essentially exposed to peak voltage occurred by the change in load current. The overshoot and undershoot conditions occur due to the instantaneous change of the load current. Since the presence of an external capacitor can control the output voltage by the load current applied to the LDO regulator, a system must be configured to provide additional current to operate reliably in the load current range of the capacitor-less LDO regulator. The capacitor was noticeable when the output voltage changed with the load current. As a result, the proposed LDO regulator was designed as a system to replace the capacitor by providing an additional current path in the given load current range. As a result, the proposed LDO regulator obtained a current path capable of effectively supplying and discharging additional current and maintaining a stable voltage under overshoot and undershoot conditions. And also, it can be confirmed that the proposed LDO regulator also formed additional feedback paths at the output node and at the gate nodes of the pass transistors in response to changes in the output voltage.

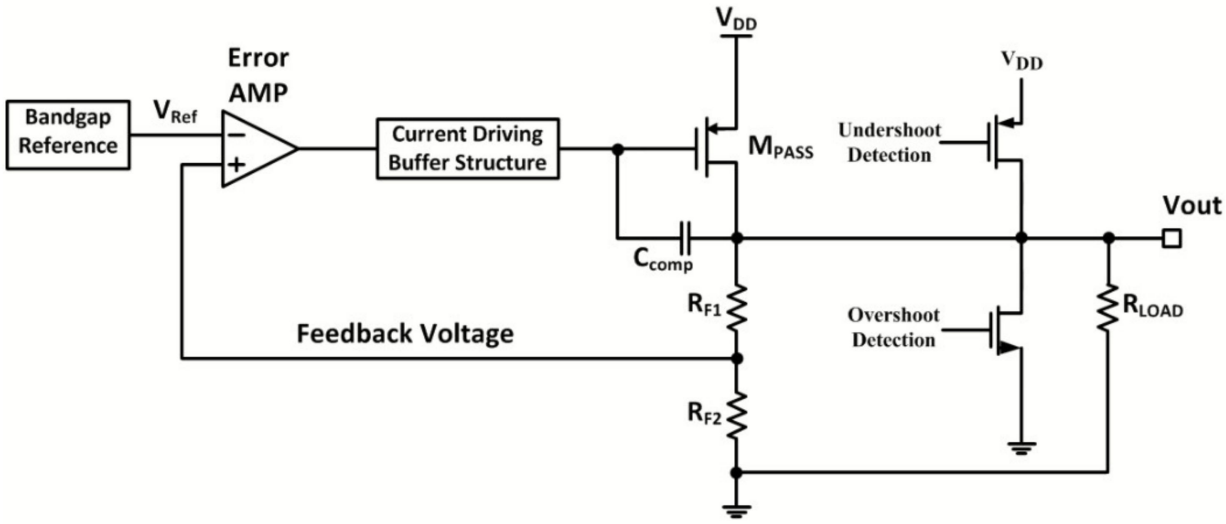

Figure 2. Proposed LDO Regulator.

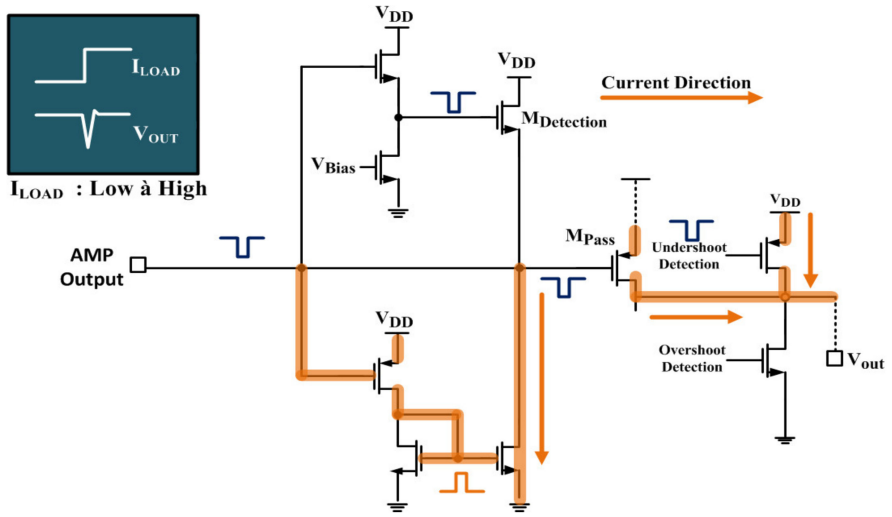

Figure 3. Current Driving Buffer Structure with undershoot in the proposed LDO regulator.

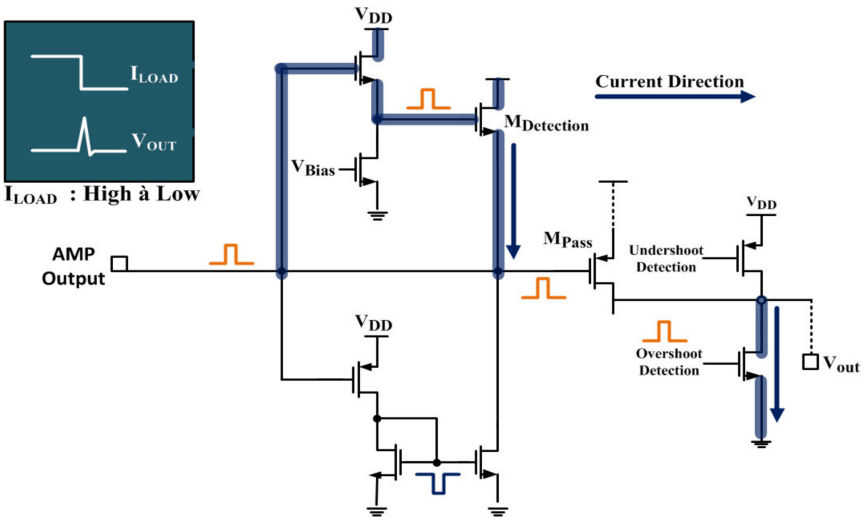

Figure 4. Current Driving Buffer Structure with overshoot in the proposed LDO regulator.

2.2. LVTSCR-Based ESD Protection Structure

Figures 5 and 6 show a cross-section of the proposed ESD protection circuit and an equivalent circuit diagram. The proposed SCR-based ESD protection circuit is designed based on the existing LVTSCR. In addition, it is formed on the deep N well to block the P-type leakage path. The addition of the P-well region and the P+ implant to the left of the N-well region was conducted, and the N+ implant was formed to the right. The P+ implant region on the left supports the forward junction of the P-well and N-well junctions, and the N+ implant region on the right has the effect of increasing doping concentration and lowering the element trigger voltage at the avalanche breakdown point. In addition, the MOSFET structure was inserted in the same way as LVTSCR, and the base region of the parasitic NPN bipolar transistor (Q3) was minimized by adjusting the gate length. The operating principle of the proposed ESD protection circuit is as follows. First, during normal operation, the protection circuit does not operate normally due to the reverse junction of the N+ bridge area on the center-right and the P-well area on the right. When the ESD surge is applied, the electronic current increases the N-well potential and, when the threshold is reached, causes an avalanche breakdown between reverse junctions and produces the electron-hole pair. Among them, hole current enters the negative terminal through the P-well area on the right, increasing the potential of the P-well. The parasitic NPN bipolar transistor (Q3) is illuminated when the potential applied to Rp2 reaches the forward bias of

the P-well and N+ cathodes on the right. This parasitic NPN bipolar transistor (Q3) supplies the base current of the parasitic PNP bipolar transistor (Q2), and finally the parasitic NPN transistor (Q1, Q3) turns on in turn. Therefore, three parasitic bipolar transistors (Q1–Q3) are operated to form a positive feedback loop and effectively discharge ESD current. An additional parasitic NPN bipolar transistor (Q1) exists in the discharge path, as seen in the proposed equivalent circuit, increasing the voltage of the proposed ESD protection circuit and significantly increasing the holding voltage. Therefore, the proposed ESD protection circuit has a surface-facing current path compared to the conventional LVTSCR, and the relatively high current gain NPN bipolar transistor can minimize the increase in dynamic resistance and robustness deterioration due to the increase in current discharge length. Therefore, an additional NPN bipolar transistor Q1 is used to provide lower on-resistance characteristics. It is designed to be optimized for the 3.3 V application, the minimum operating voltage of the proposed LDO regulator [25–35].

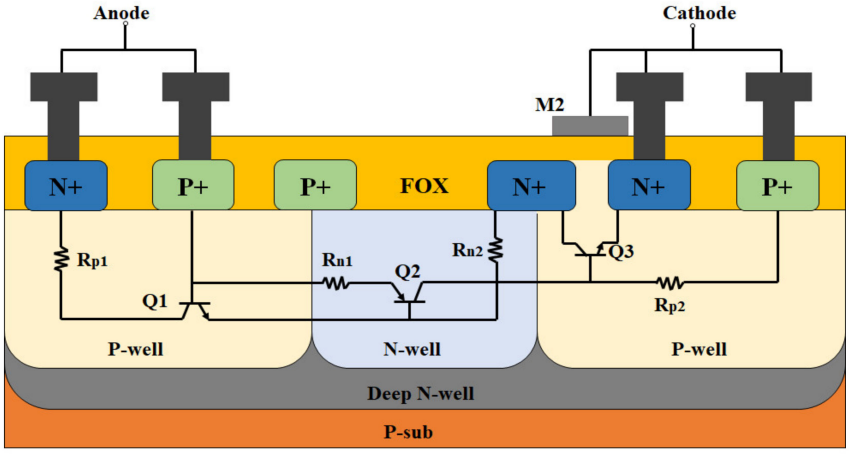

Figure 5. LVTSCR-Based ESD Protection Structure.

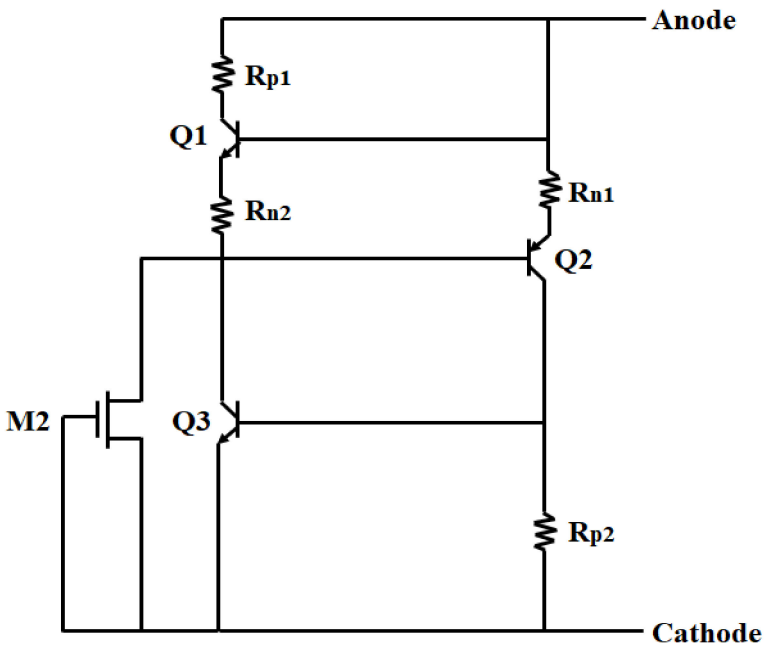

Figure 6. Equivalent circuit of SCR-based ESD protection structure.

3. Simulation Result

Figure 7 shows the simulation results of transient response characteristics of the proposed LDO regulator. The LDO regulator with the current driving buffer structure was provided with an additional feedback path in accordance with the change in the instantaneous load current, ensuring a stable output power voltage. Through simulations, the proposed LDO regulator kept an undershoot voltage of 20 mV and an overshoot voltage of 17 mV in accordance with a load current of 250 mA. As shown in Figure 8, it was confirmed that the current driving buffer structure supplies and discharges current like a switch according to the instantaneous generation of the load current.

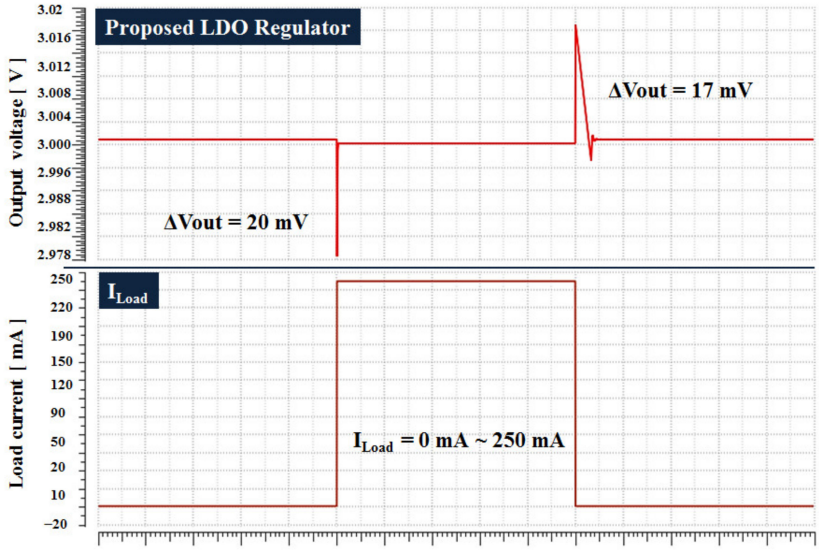

Figure 7. Results of simulation of transient response characteristics of the proposed LDO regulator.

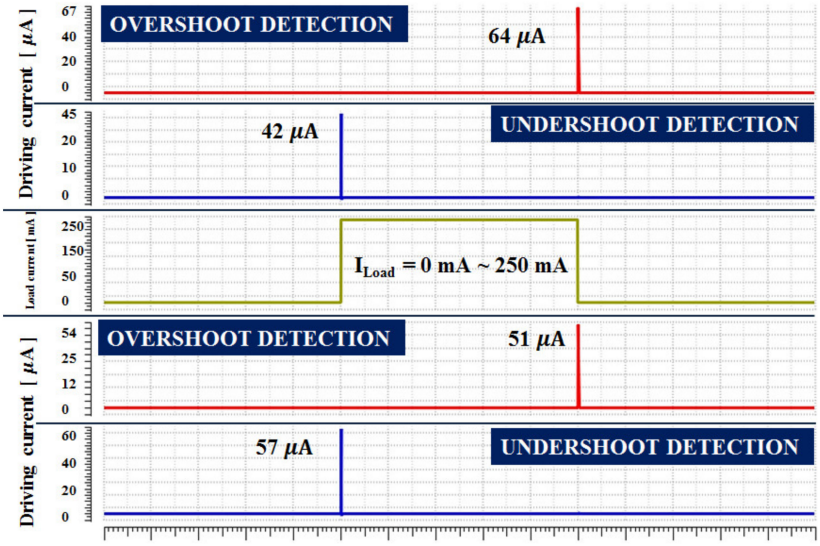

Figure 8. Simulation on the performance of the current supply and discharge path operated in the current driving buffer structure according to variation of load current.

If an undershoot voltage occurs with a load current of 250 mA, the current driving buffer structure is operated through feedback. A generation of undershoot voltage means that the current of the pass transistor is increased by the reduction of the voltage of the gate node of the pass transistor. The proposed current driving buffer structure provided an additional current discharge path to the gate node of the path transistor. At the same

time, the output node of the proposed LDO regulator is provided a supply current path that can effectively increase the output voltage. When an undershoot voltage occurs, the current driving buffer structure is ensured a gate node current discharge path of a path transistor of 42 µA and an output node current supply path of an LDO regulator of 57 µA. In addition, the generation of the overshoot voltage means that the voltage of the gate node of the pass transistor is increased by the reduction of the current of the pass transistor. The proposed current driving buffer structure is provided an additional current supply path to the gate node of the path transistor. At the same time, the power terminal of the proposed LDO regulator is provided a current discharge path that can effectively reduce the power voltage. When an overshoot voltage occurs, the current driving buffer structure is ensured a gate node current supply path of a path transistor of 64 µA and an output node current discharge path of an LDO regulator of 51 µA. The current driving buffer structure is provided the additional supply and discharges current to the path transistor and the output node. The proposed LDO regulator with the current driving buffer structure can be provided the additional supply or discharge paths of the driving current of 99 µA for undershoot and 115 µA for overshoot. The magnitude of the additional supplied and discharged current is in µA, so it may feel small. This is because the undershoot/overshoot situation is caused by an instantaneous change in load current. Namely, when undershoot occurs, if the voltage applied to the gate node of the pass transistor has a lower voltage, the current flowing into the pass transistor is effectively increased. Accordingly, the output node of the LDO regulator is supplied with the required current. When an overshoot occurs, if the voltage applied to the gate node of the pass transistor may have a higher voltage, the current flowing into the pass transistor is effectively decreased. Even in this condition, the output node of the LDO regulator keeps the required current. The proposed LDO regulator with the current driving buffer structure is selectively supplied or discharged the additional current to two nodes compared to the required current. In addition, since the path transistor of the proposed LDO regulator is a very large-sized device, it is designed to effectively control the high current by the additional current driving buffer structure. As a result, it is confirmed that the proposed LDO regulator stably kept the output power supply voltage regardless of the instantaneous change of large load current.

4. Measurement Result

Figure 9 shows the chip layout of the proposed LDO regulator with the current driving buffer structure. The manufactured chip dimension of the proposed LDO regulator is 479 × 343 um. In addition, the damage and destruction of the semiconductor integrated circuit may occur because more than a few amperes of current are received in a short time from the ESD phenomenon. To prevent this, the ESD protection circuits are embedded in the POWER CLAMP and I/O CLAMP of the proposed LDO regulator. Consequently, the high reliability characteristics of the proposed LDO regulator were ensured by protecting the internal circuit from ESD and discharging the ESD current.

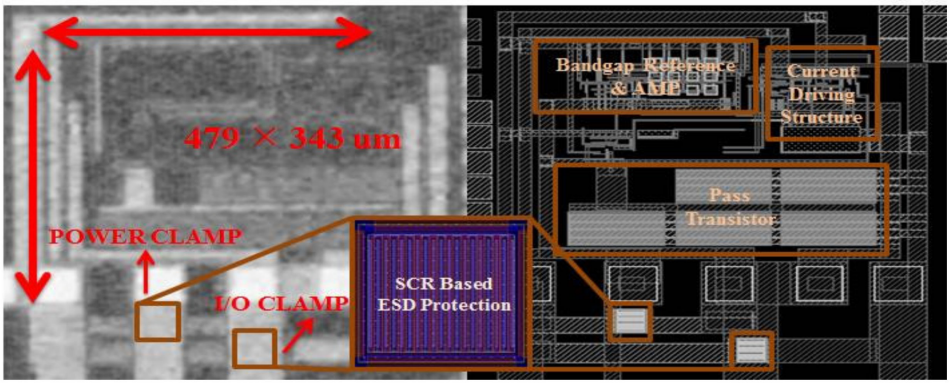

Figure 9. Chip layout of the proposed LDO regulator.

Figure 10 shows the measurement results of transient response characteristics of the proposed LDO regulator. A stable voltage change is kept by equalizing the output voltage of the LDO regulator according to the load current. It was confirmed that it had an undershoot voltage of 14 mV and an overshoot voltage of 12 mV when a load current of 100 mA occurred. As shown in Figure 11, undershoot voltage of 19 mV and overshoot voltage of 15 mV were ensured at a load current of 200 mA. In addition, as shown in Figure 12, a small undershoot voltage of 22 mV and a small overshoot voltage of 19 mV were ensured even with a large load current of 250 mA. The current driving buffer structure generated additional current supply and discharge at the gate node of the path transistor and the output node of the LDO regulator. The undershoot/overshoot voltage depending on the load current may cause a major problem in the system of the LDO regulator, so a stable output power voltage shall be ensured. As a result, it was verified that the proposed LDO regulator has a stable peak voltage through the additional current supply and discharge paths through the current driving buffer structure, even with a large load current.

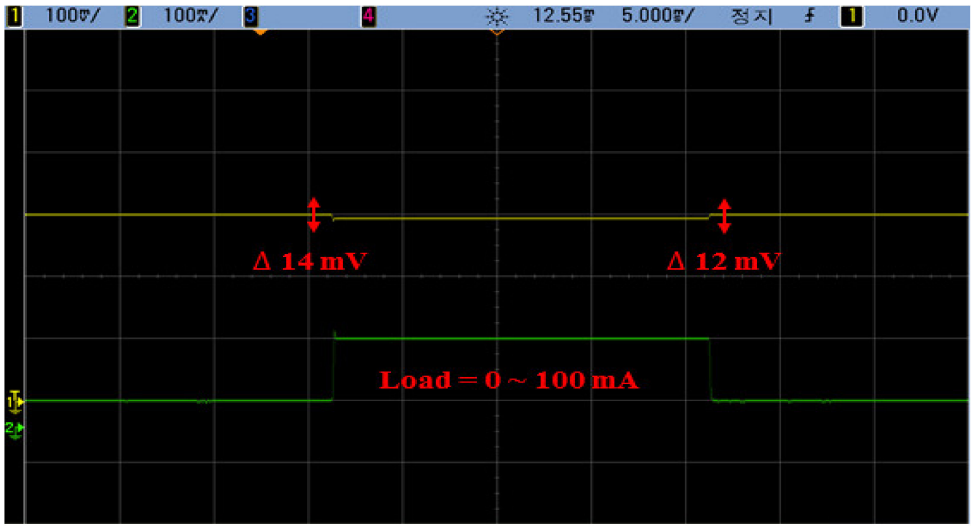

Figure 10. Load transient of the proposed LDO regulator (Load = 100 mA).

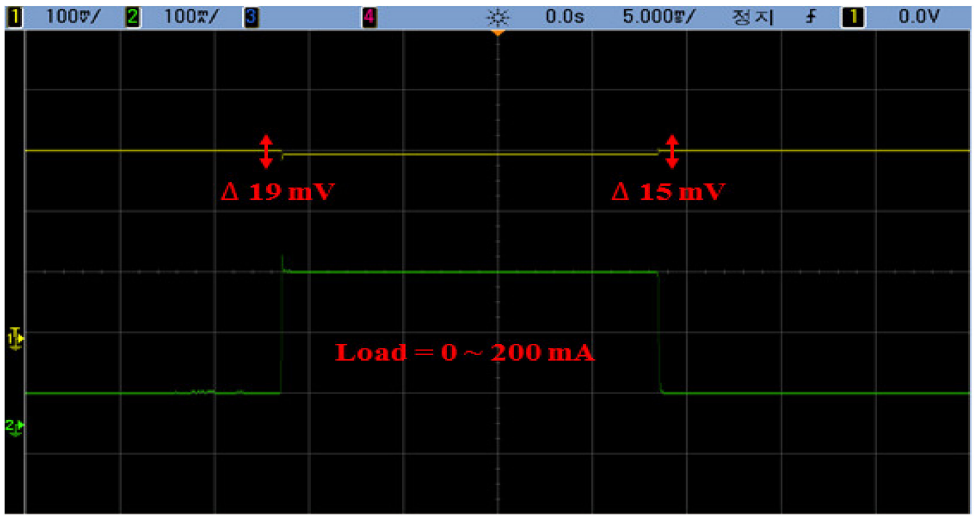

Figure 11. Load transient of the proposed LDO regulator (Load = 200 mA).

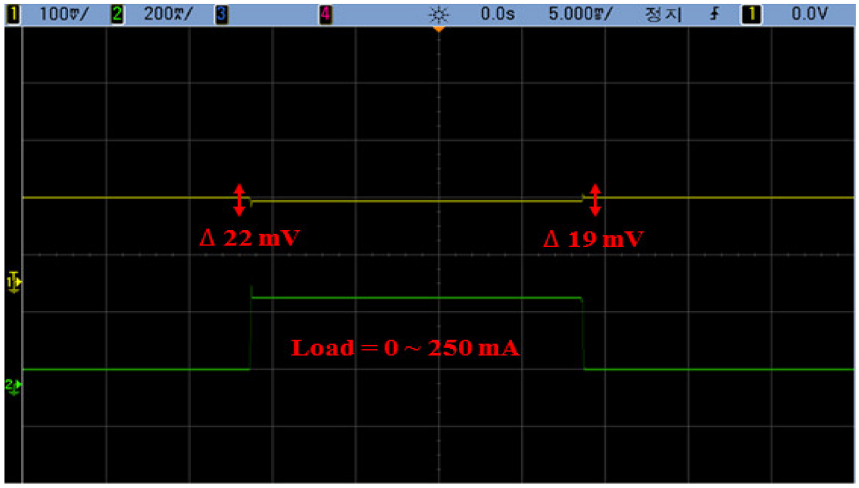

Figure 12. Load transient of the proposed LDO regulator (Load = 250 mA).

Figure 13 shows the measurement results of load regulation kept by continuously increasing the load current up to 250 mA in the proposed LDO regulator. It was confirmed that a change of 7 mV occurred in the load current range of 0 mA to 250 mA in the proposed LDO regulator. It was verified that the proposed LDO regulator with the current driving buffer structure has a stable output power voltage despite the constant increase of the load current.

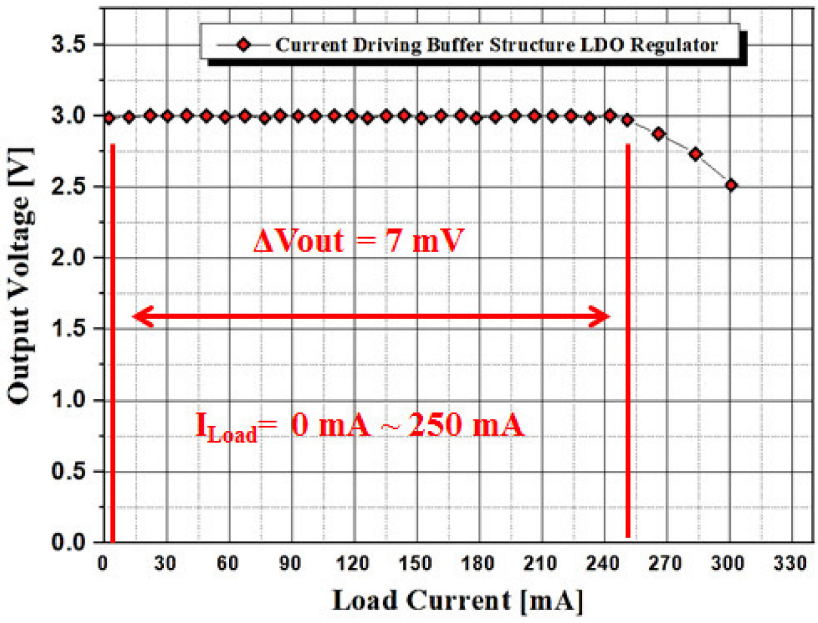

Figure 13. Load regulation of the proposed LDO regulator.

Figure 14 shows the measurement results of input control kept by continuously increasing the input voltage range from 3.3 V to 4.5 V in the proposed LDO regulator. It was confirmed that the voltage change of 12 mV occurred in the input voltage range of 3.3 V to 4.5 V in the proposed LDO regulator. The LDO regulator with the current driving buffer structure has a stable output power voltage value despite the continuous increase of the input voltage. In addition, the input voltage range of the proposed LDO regulator was set at a line not exceeding 15 mV.

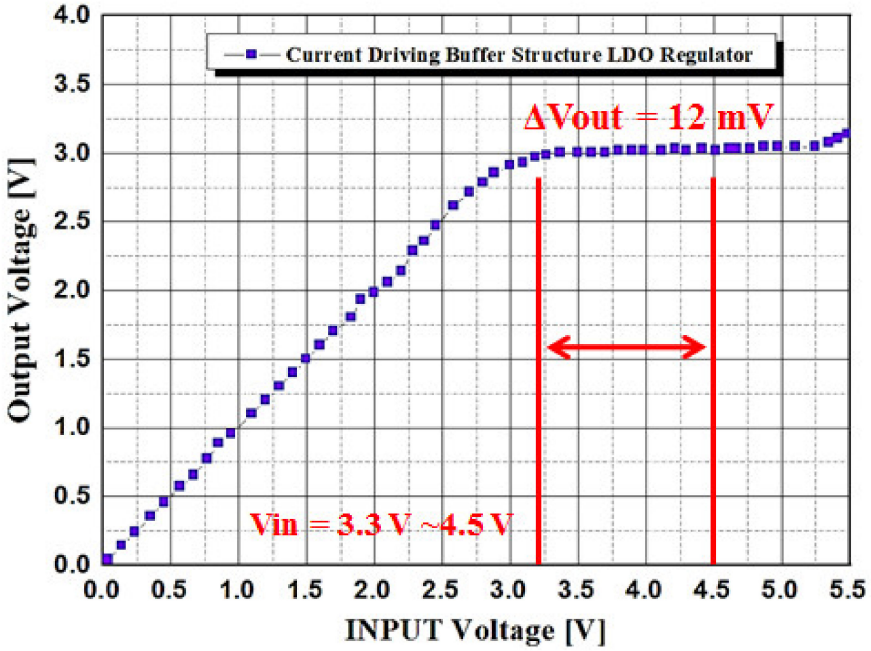

Figure 14. Line regulation of the proposed LDO regulator.

Figure 15 shows the quiescent current of the proposed LDO regulator. In mobile applications, low-voltage LDO regulators are often used. Therefore, the management of low quiescent current it is essential to effectively improve the life of a mobile device. The proposed LDO regulator secured a quiescent current of at least 47 μA and up to 49 μA.

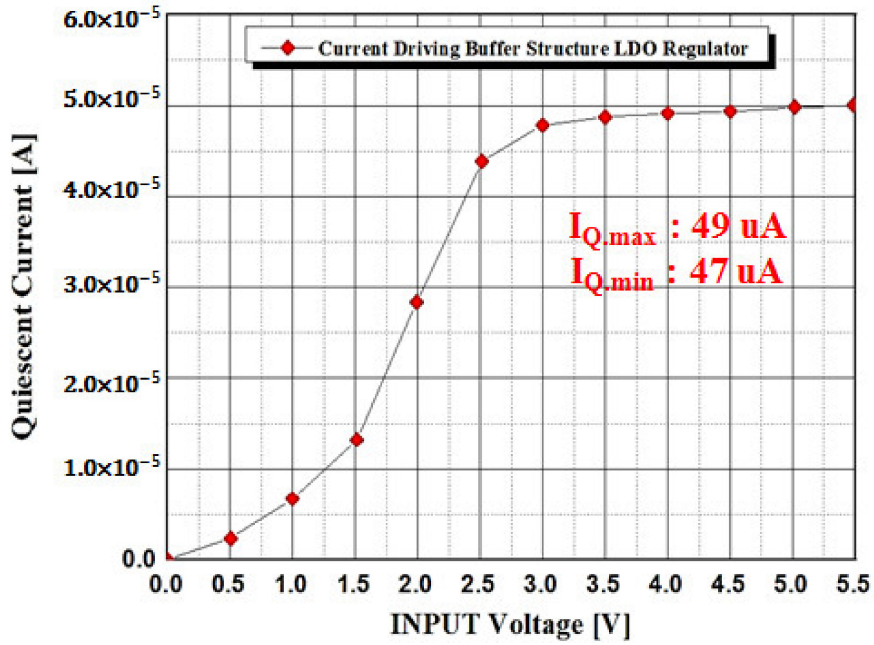

Figure 15. Quiescent current of the proposed LDO regulator.

In addition, Figure 16 shows the measurement result for evaluating the temperature characteristics of the proposed LDO regulator. The recommended operating junction temperature for LDO regulators is −40 °C to 125 °C. It was validated that the output voltage of the proposed LDO regulator changes only 3.8 mV in the temperature range of −40 °C to 140 °C.

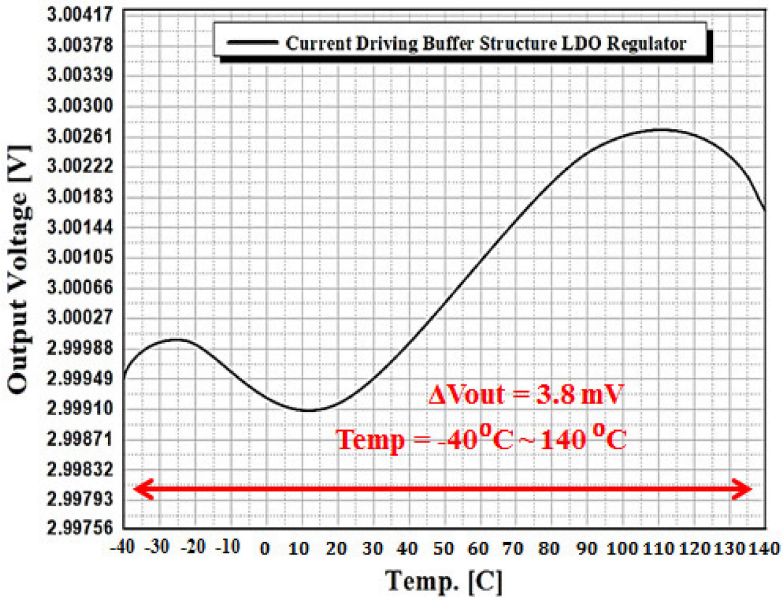

Figure 16. Temperature characteristics of the proposed LDO regulator.

Figure 17 shows the measurement results using Transmission Line Pulse (TLP) to confirm the electrical properties of SCR, LVTSCR, and the proposed ESD protection circuit. The design window of the proposed ESD protection circuit was set between 3.66 V of +10% margin of an operating voltage and 12.5 V of the gate-oxide breakdown region in the 0.18 μm BCD process. Thus, an ESD design window formed in which the operating voltage of the proposed LDO regulator is 3.3 V. As a result of the measurement, the trigger voltage of 9.14 V and the holding voltage of 4.55 V were observed. In addition, it was confirmed that the parasitic NPN bipolar transistor with a high current gain has a secondary breakdown current It2 with about 7 A due to the operation. Therefore, it was confirmed to have a higher retention voltage and a lower trigger voltage compared to the conventional SCR and LVTSCR.

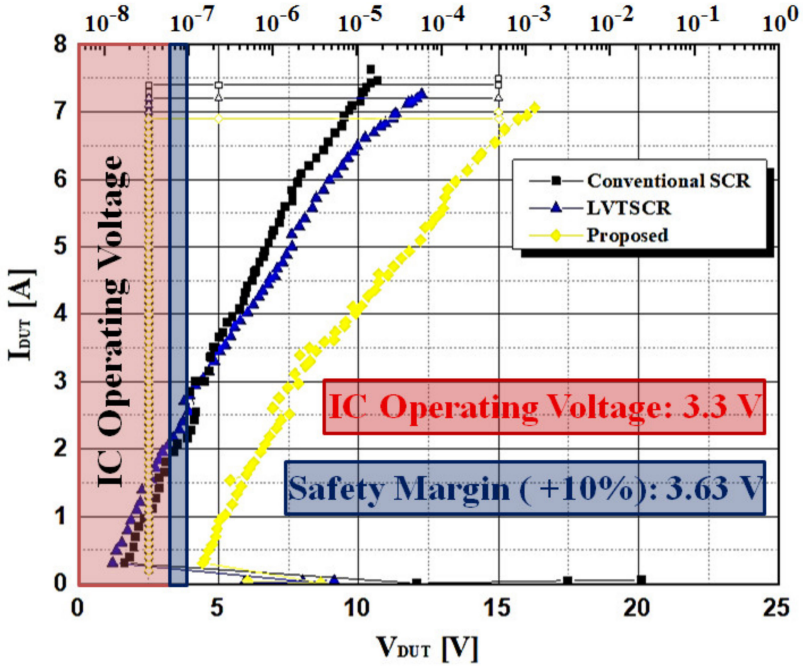

Figure 17. TLP I-V curve of proposed ESD clamp.

Figures 18 and 19 show the results of the thermal reliability evaluation at high temperatures (300 K–500 K) of the proposed ESD protection circuit. The thermal reliability was evaluated by a hot chuck controller, and I-V characteristics were measured by TLP. The high-temperature characteristic is very important because it affects the ESD protection circuit and the electrical characteristics of It2. In addition, the decrease in carrier mobility and the increase in well resistance components due to temperature rise are important factors affecting the electrical and sensitivity characteristics of the ESD protection circuit. As a result of the measurement, the proposed ESD protection circuit kept a holding voltage of 6.2 V (safety margin of operating voltage + 10% or more) at a temperature of 500 K, has It2 value 5.1 A and HBM 6 kV (calculated from It2 × (1500 + Ron)), and its excellent robustness was verified.

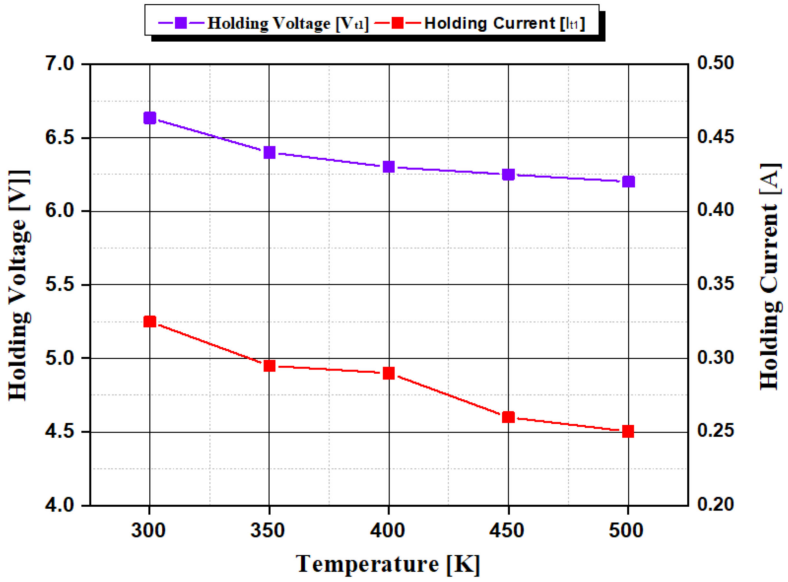

Figure 18. Holding current and voltage at high temperature (300 to 500 K).

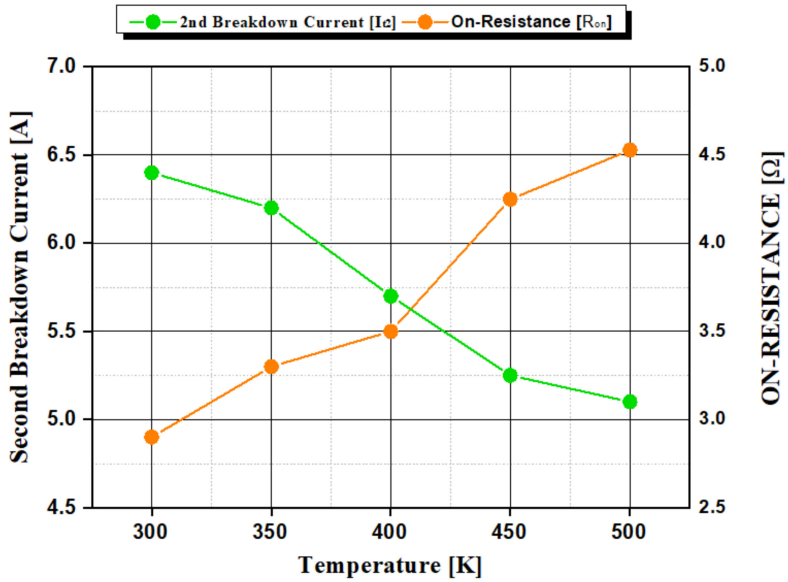

Figure 19. Secondary trigger current and on-resistance (300 to 500 K).

Table 1 shows the circuit structure of the LDO regulator and the results of various types of measurements. Although there will be design variables and various environmental

factors, it has been verified that the proposed LDO regulator can provide a stable output voltage even with large load currents compared to the results of other researchers.

Table 1. Performance summary and comparison with reported prior study.

Measurement	[1]	[2]	[3]	[7]	[8]	[12]	[14]	This Work
Technology (μm)	0.35	0.13	0.35	0.35	0.35	0.13	0.13	0.18
Supply Voltage(V)	3.3	2.7	1.2	3.3	2.5	1.2	1.2	3.3
Output Voltage (V)	2.9	2.5	1	3	2.35	1	1	3
Load Current: I_{MAX} (mA)	100	100	100	200	100	50	100	250
Quiescent Current (μA)	55	72	-	147	7	42	0.7	49
Load Transient (I_{LOAD} Rising) (mV)	90	-	45	100	236	140	76	22
Load Transient (I_{LOAD} Falling) (mV)	160	-	42	110	227	80	198	19
Load Regulation (mV)	-	100	4.2	45	8	10	10	7
Line Regulation (mV)	-	20	3	34	1	30	16.6	12
COUT (pF)	100	2.2×10^6	100	1×10^6	0–100	400	0–1×10^6	100
Year	2016	2013	2007	2010	2020	2019	2020	2022

5. Conclusions

This study was carried out to propose an LDO regulator with the transient response characteristics improved by adding a current-driving buffer structure to the feedback path of an existing LDO regulator. Thereby, the proposed LDO regulator can effectively control the peak voltage varied according to the load current. It was confirmed that the node between the pass transistor and the output node of the error amplifier improved the transient response characteristics of the LDO regulator by supplying and discharging the current according to the load current. Consequently, it was confirmed that the proposed LDO regulator maintained an undershoot voltage of 22 mV and an overshoot voltage of 19 mV at the load current of 250 mA. Namely, since the proposed LDO regulator with a current driving buffer structure provides a feedback path operated selectively for additionally supplying and discharging a driving current, it was verified that the proposed LDO regulator with a current driving buffer structure designed to additionally form a new feedback control path instead of the existing feedback loop can effectively control the peak voltage regardless of the change of load current. The performance of the proposed LDO regulator was evaluated in comparison with existing studies, as shown in Table 1. Since the blocks installed at the LDO regulators are applied to the various load currents, the LDO regulator proposed in this study is judged to be a suitable system that can easily respond to these requirements. In addition, stability and reliability are also some of the most important issues in ICs. The proposed LDO regulator has a built-in high-performance ESD protection circuit in I/O stage and power line. It was verified that the proposed LDO regulator bypasses the high voltage surge by ESD and maintained excellent current driving capability, stable power supply, and high reliability. The ESD protection circuit with the new SCR-based structure has excellent thermal reliability. In addition, the ESD protection circuit provides a suitable solution for high-temperature characteristics and low voltage applications above HBM 6 kV.

Author Contributions: Conceptualization, S.-W.K.; Formal analysis, S.-W.K.; Project administration, Y.-S.K.; Supervision, Y.-S.K.; Validation, S.-W.K.; Writing—original draft, S.-W.K.; Writing—review & editing, S.-W.K. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by Korea Evaluation Institute of Industrial Technology (KEIT) grant funded by the Ministry of Trade, Industry & Energy (20009739, "Development of Low Noise 3phase BLDC Motor Drive SoC for Electric Vehicles with Power Switch and Hall Sensors") and (RS-2022-00143842, "Single/Three-phase AC/DC Converter Smart Power IC using SiC MOSFET devices").

Data Availability Statement: No new data were created or analyzed in this study. Data sharing is not applicable to this paper.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Moon, J.; Hyun, J.; Kim, S.-W. Design of low-power, fast-transient-response, capacitor-less low-dropout regulator for mobile applications. *IEICE Electron. Express* **2016**, *13*, 0882. [CrossRef]
2. Koo, Y.S. A design of low-area low drop-out regulator using body bias technique. *IEICE Electron. Express* **2013**, *10*, 20130300. [CrossRef]
3. Lau, S.K.; Mok, P.K.T.; Leung, K.N. A low-dropout regulator for SoC with Q-reduction. *IEEE J. Solid-State Circuits* **2007**, *42*, 658. [CrossRef]
4. Jun, J.W.; Koo, Y.S.; Lee, K.Y. Design of high-reliability LDO with current limiting characteristics with built-in new high tolerance ESD protection circuit. *IEICE Electron. Express* **2013**, *10*, 20130516. [CrossRef]
5. Manikandan, P.; Bindu, B. A transient enhanced cap-less low-dropout regulator for wide range of load currents and capacitances. *Microelectron. J.* **2021**, *115*, 105207. [CrossRef]
6. Chong, S.S.; Chan, P.K. A 0.9-/spl mu/A Quiescent Current Output-Capacitorless LDO Regulator with Adaptive Power Transistors in 65-nm CMOS. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2013**, *60*, 1072. [CrossRef]
7. Wang, J.; Gao, D.; Hu-Guo, C.; Jaaskelainen, K.; Hu, Y. A High Load Current, Low-Noise, Area-Efficient, Full On-Chip Regulator for CMOS Pixel Sensors. *IEEE Trans. Nucl. Sci.* **2012**, *59*, 582. [CrossRef]
8. Ming, X.; Li, Q.; Zhou, Z.K.; Zhang, B. An Ultrafast Adaptively Biased Capacitorless LDO With Dynamic Charging Control. *IEEE Trans. Circuits Syst. II Express Briefs* **2012**, *59*, 40–44. [CrossRef]
9. Duan, Q.; Li, W.; Huang, S.; Ding, Y.; Meng, Z.; Shi, K. A Two-Module Linear Regulator with 3.9-10 V Input, 2.5 V Output, and 500 mA Load. *Electronics* **2019**, *8*, 1143. [CrossRef]
10. Liu, N.; Chen, D. A Transient-Enhanced Output-Capacitorless LDO with Fast Local Loop and Overshoot Detection. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 3422. [CrossRef]
11. Han, W.; Lee, H. A 340-nA-Quiescent 80-mA-Load 0.02-fs-FOM Active-Capacitor-Based Low-Dropout Regulator in Standard 0.18-μm CMOS. *IEEE Solid-State Circuits Lett.* **2021**, *125*, 125–128. [CrossRef]
12. Lavalle-Aviles, F.; Torres, J.; Sánchez-Sinencio, E. A High Power Supply Rejection and Fast Settling Time Capacitor-Less LDO. *IEEE Trans. Power Electron.* **2019**, *34*, 474–484. [CrossRef]
13. Peng, S.-Y.; Liu, L.-H.; Chang, P.-K.; Wang, T.-Y.; Li, H.Y. A Power-Efficient Reconfigurable Output-Capacitor-Less Low-Drop-Out Regulator for Low-Power Analog Sensing Front-End. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 1318. [CrossRef]
14. Răducan, C.; Grăjdeanu, A.-T.; Plesa, C.-S.; Neag, M.; Negoiţă, A.; Ţopa, M.D. LDO With Improved Common Gate Class-AB OTA Handles any Load Capacitors and Provides Fast Response to Load Transients. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *37*, 3740–3752. [CrossRef]
15. Torres, J.; El-Nozahi, M.; Amer, A.; Gopalraju, S.; Abdullah, R.; Entesari, K.; Sanchez-Sinencio, E. Low Drop-Out Voltage Regulators: Capacitor-less Architecture Comparison. *IEEE Circuits Syst. Mag.* **2014**, *14*, 6. [CrossRef]
16. Chen, J.J.; Yang, F.-C.; Kung, C.-M.; Lai, B.-P.; Hwang, Y.-S. A capacitor-free fast-transient-response LDO with dual-loop controlled paths. In Proceedings of the 2007 IEEE Asian Solid-State Circuits Conference, Jeju, Korea, 12–14 November 2007; Volume 12. [CrossRef]
17. Park, K.-H.; Yang, I.-S.; Koo, Y.-S. A Design of Low-dropout Regulator with Adaptive Threshold Voltage Technique. *J. Semicond. Technol. Sci.* **2018**, *18*, 287. [CrossRef]
18. Do, K.I.; Jin, S.-H.; Lee, B.-S.; Woo, J.-W.; Koo, Y.-S. Design of All-Directional ESD Protection circuit with SCR-based I/O and LIGBT-based Power clamp. In Proceedings of the 2021 International Conference on Electronics, Information, and Communication (ICEIC), Jeju, Korea, 31 January 2021–3 February 2021; p. 20533020. [CrossRef]
19. Koo, Y.-S. Electrical characteristics of novel SCR - based ESD protection for power clamp. *IEICE Electron. Express* **2012**, *9*, 1479. [CrossRef]
20. Do, K.I.; Koo, Y.-S. A Novel Low Dynamic Resistance Dual-Directional SCR With High Holding Voltage for 12 V Applications. *IEEE J. Electron Devices Soc.* **2020**, *8*, 635–639. [CrossRef]
21. Do, K.I.; Jin, S.-H.; Lee, B.-S.; Koo, Y.-S. 4H-SiC-Based ESD Protection Design with Optimization of Segmented LIGBT for High-Voltage Applications. *IEEE J. Electron Devices Soc.* **2021**, *9*, 1017–1023. [CrossRef]
22. Koo, Y.-S.; Lee, K.Y.; Kim, K.-D.; Kwon, J.-K. The design of high holding voltage SCR for whole-chip ESD protection. *IEICE Electron. Express* **2008**, *5*, 624. [CrossRef]
23. Do, K.I.; Lee, B.; Kim, S.G.; Koo, Y.S. Design of 4H-SiC-Based Silicon-Controlled Rectifier with High Holding Voltage Using Segment Topology for High-Voltage ESD Protection. *Electron Device Lett.* **2020**, *41*, 1669–1672. [CrossRef]
24. Koo, Y.-S.; Lee, K.-Y. SCR-based ESD protection device with low trigger and high robustness for I/O clamp. *IEICE Electron. Express* **2012**, *9*, 200. [CrossRef]
25. Do, K.I.; Song, B.-B.; Koo, Y.S. A Gate-Grounded NMOS-Based Dual-Directional ESD Protection with High Holding Voltage for 12 V Application. *IEEE Trans. Device Mater. Reliab.* **2020**, *20*, 716–722. [CrossRef]
26. Do, K.I.; Koo, Y.S. Silicon-controlled Rectifier-based Electrostatic Discharge Protection Circuit with Additional NPN Parasitic Bipolar Junction Transistor for 5-V Application. *J. Semicond. Technol. Sci.* **2021**, *21*, 101. [CrossRef]

27. Koo, Y.-S. Analysis of the electrical characteristics of SCR-based ESD Protection Device (PTSCR) in 0.13/0.18/0.35um process technology. *IEICE Electron. Express* **2011**, *8*, 8. [CrossRef]
28. Do, K.I.; Lee, B.-S.; Koo, Y.-S. A New Dual-Direction SCR With High Holding Voltage and Low Dynamic Resistance for 5 V Application. *IEEE J. Electron Devices Soc.* **2019**, *7*, 601–605. [CrossRef]
29. Do, K.I.; Lee, B.-S.; Koo, Y.-S. Study on 4H-SiC GGNMOS Based ESD Protection Circuit with Low Trigger Voltage Using Gate-Body Floating Technique for 70-V Applications. *IEEE Electron Device Lett.* **2019**, *40*, 283–286. [CrossRef]
30. Song, B.-B.; Do, K.-I.; Koo, Y.S. SCR-Based ESD Protection Using a Penta-Well for 5 V Applications. *IEEE J. Electron Devices Soc.* **2018**, *6*, 691–695. [CrossRef]
31. Do, K.I.; Song, B.-B.; Koo, Y.S. A Novel Dual-Directional SCR Structure with High Holding Voltage for 12-V Applications in 0.13-µm BCD Process. *IEEE Trans. Electron Devices* **2020**, *67*, 5020–5027. [CrossRef]
32. Song, B.-B.; Lee, B.-S.; Yang, I.-S.; Koo, Y.-S. Analysis of a Parasitic-Diode-Triggered Electrostatic Discharge Protection Circuit for 12 V Applications. *ETRI J.* **2017**, *39*, 746–755. [CrossRef]
33. Do, K.I.; Koo, Y.S. A New SCR Structure with High Holding Voltage and Low ON-Resistance for 5-V Applications. *IEEE Trans. Electron Devices* **2020**, *67*, 1052–1058. [CrossRef]
34. Do, K.I.; Lee, B.-S.; Chae, H.-G.; Seo, J.-J.; Koo, Y.S. A Novel Low Trigger SCR with Latch up Immunity for 5 V Application. In Proceedings of the European Conference on Electrical Engineering and Computer Science (EECS), Bern Switzerland, 20–22 December 2018. [CrossRef]
35. Do, K.I.; Won, J.-I.; Koo, Y.S. A 4H-SiC MOSFET-Based ESD Protection with Improved Snapback Characteristics for High-Voltage Applications. *IEEE Trans. Power Electron.* **2021**, *36*, 4921–4926. [CrossRef]