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Total-Ionization-Dose Radiation Effects and Hardening Techniques of a Mixed-Signal Spike Neural Network in 180 nm SOI-Pavlov Process

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Abstract: A mixed-signal spiking neural network (SNN) chip is presented, and its radiation effect-Total Ionizing Dose (TID) was studied. The chip was fabricated in a 180 nm silicon-on-insulator (SOI) integration process with an area of 3.75 mm^2; the total doses were set at 300 krad (Si), 500 krad (Si), and 1 Mrad (Si). The TID radiation experimental results showed that the average spike frequency and spike amplitude of the output signal of the SNN circuit decreased after the irradiation because of the leakage current caused by the charge trapped in the buried oxide. Sensitive nodes were identified through the analysis of the critical path of the circuit, and guidance toward a radiation-hardening neuron circuit was proposed. The proposed circuit maintains good robustness with firing frequency variation.

Keywords: SOI technology; SNN; Pavlov; TID; radiation-hardening technology

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1. Introduction

The amount of computation in neural network algorithms continues to increase. As computers based on Von Neumann architecture encounter the issue of "storage access bottlenecks", computational efficiency and power consumption can no longer meet the needs of complex artificial intelligence algorithms [1]. To address this problem, a spiking neural network (SNN) acceleration method that simulates the human brain was proposed [2]. It mainly adopted circuits to simulate biological neurons (computational units) and synapses (storage units) and form a neural network structure through very large-scale integration (VLSI) to implement neuromorphic hardware. The SNN in the mixed-signal method has proven to be one of the effective solutions for the trade-off between power consumption and computational complexity [3,4].

The SNN-based AI system has extremely important prospects in space applications, such as target recognition, on-orbit perception, automatic control, and deep space exploration. [5] Hence, the SNN circuit must have a strong tolerance to radiation. Research on the radiation effect and hardening scheme is of great significance to develop a space-born AI system.

To improve the radiation resistance of neuromorphic circuits in space, a typical option is to use SOI technology because a thin insulating layer of buried oxide insulation is used, which improves the electrical isolation between the channel and the substrate. Another option is to find sensitive nodes in the circuit and harden them. Typically, chips for space applications implement radiation resistance through a combination of both circuits and processes. However, research on the effects of TID on neuromorphic circuits has mainly focused on RRAM-related work [6] and there is a lack of research on SOI-based neural circuits.

This paper presents a mixed-signal implementation of a Pavlov SNN circuit, fabricated in 180 nm PDSOI technology with an area of 3.75 mm^2. In Section 2, this paper shows how to use analog circuits to implement biophysically complex neural and synaptic dynamics behaviors and discusses the problem of implementing neuromorphic algorithms with circuits. In particular, the paper exploits the properties of the PDSOI technique to design an SNN circuit that reproduces Pavlov's experiment.

Section 3 discusses the chip testing and the TID effect up to a dose of 1 Mrad (Si). The radiation effects of the neuromorphic hardware were analyzed using the experimental results, and the sensitive nodes of the circuit were explored. Moreover, a feasible radiation-hardening strategy was proposed to guarantee reliable operation in space.

2. Mixed-Signal Pavlov SNN Circuit

2.1. SOI Process Advantages

SOI CMOS technology is a critical factor in providing excellent performance of the IC in radiation-sensitive environments. Performance and reliability are significantly increased by adding a silicon dioxide layer to isolate the transistors from the substrate. The better performance of SOI CMOS compared with bulk CMOS is improved by:

(a) Low Noise and Crosstalk: SOI CMOS enables novel process and design techniques to achieve a very low noise operation and lower crosstalk to support high-performance mixed-mode circuits.

(b) Reduce Parasitic: Isolation from the lumped silicon substrate reduces the capacitive load, thus providing better performance and lower power consumption.

In addition, bulk effects, such as source/drain leakage, latch-up, parasitic source/drain junction capacitances, and substrate noise coupling, are significantly reduced. The lower doping features lead to less threshold voltage variation and device mismatch across the chip.

2.2. Key Circuit in 180 nm PDSOI Process

In this section, we implement the basic units required for neuromorphic computations, such as neurons and synapses, by combining transistors based on an analog circuit design approach.

(1) Mixed-Signal Spike Neuron Circuit

The spike neuron circuit implements the Izhikevich model [7] and the equations that describe the computational model, which are given in the following:

$$\begin{cases} \frac{dV_{\mathrm{mem}}(t)}{dt} = 0.04V_{\mathrm{mem}}(t)^2 + 5V_{\mathrm{mem}}(t) + 140 - U(t) + I(t) \\ \frac{dU(t)}{dt} = a(bV_{\mathrm{mem}}(t) - U(t)) \end{cases} \quad (1)$$

$$\text{if } V_{\mathrm{mem}}(t) \geq V_{\mathrm{th}}, \text{ then } V_{\mathrm{mem}}(t+\Delta t) = c \text{ and } U(t+\Delta t) = U(t) + d \quad (2)$$

where V_{mem}(t) represents the cell membrane voltage of the neuron; U(t) is the negative feedback variable of the cell membrane voltage; and a, b, c, and d are four dimensionless parameters representing the recovery rate, reset value, etc. Typically, a is 0.02, b is 0.2, c is −65.0, and d is 8.0.

As shown in Figure 1, the mixed-signal spike neuron circuit schematic can be subdivided into four functional blocks [8].

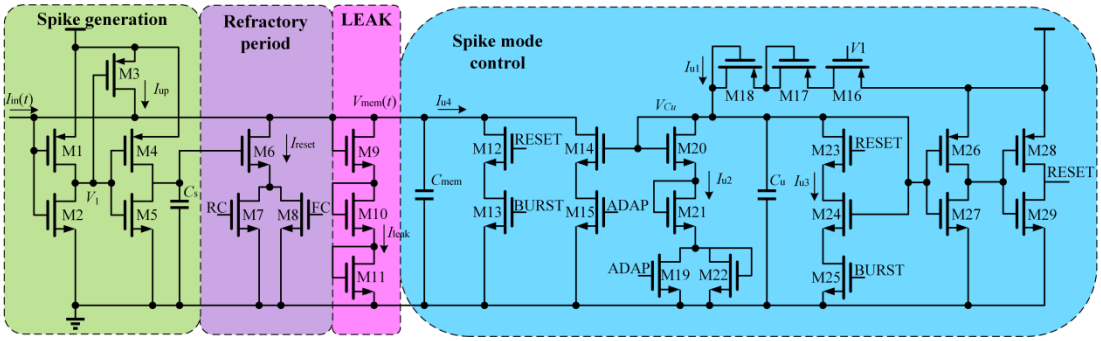


Figure 1. Mixed-signal spike neuron circuit.

The spike generation module (M1–M5) implements the neuronal membrane threshold mechanism (M1–M2) and spike signal generation. The current $I_{in}(t)$ charges the neuron membrane capacitor C_{mem}. When its membrane voltage V_{mem} exceeds the switching threshold of M1 and M2, transistors M3 and M4 charge Cs and generate a spike signal.

The refractory period module (M6–M8) models the effect of potassium conductance, resetting the neuron and implementing a refractory period mechanism. The bias voltage RC and FC control the discharge speed of membrane capacitance.

The LEAK circuit (M9–M11) models the neuron's leak conductance.

In the spike mode control module, four digital signals, namely RC, FC, ADAP, and BURST, turn the neuron circuit into seven kinds of response modes, which can exhibit a wide range of neural behaviors, such as spike-frequency adaptation property, the refractory period mechanism, and adjustable the spiking threshold mechanism.

The neuron membrane capacitance C_{mem} is charged by the current I_{IN}. When $V_{mem}(t)$ exceeds the switching thresholds of M1–M2, $V_{mem}(t)$ is first pulled high by M3 and then pulled low by the reset branch M6–M8 to V_{reset}, which in turn generates a spike signal at the V1 node. Here, the low-level V_{reset} corresponds to parameter c in the Izhikevich model. The reset branch of capacitor C_{mem} consists of three MOS transistors, M6 to M8, where the on and off states of M7 and M8 are controlled by the digital signals RC and FC, respectively. By selecting the appropriate transistor size, C_{mem} is discharged at different rates through M7 and M8 so that $V_{mem}(t)$ can be reset to different V_{reset} values through M7 and M8, respectively.

The spike model control module is used to implement the function of U(t) in the Izhikevich model, which generates different spike response patterns by controlling the discharge rate of C_{mem} in the spike generation module. The negative feedback of the spike model control module to the spike generation module is achieved by M12 to M15, which generate the current Iu4 to discharge the capacitor C_{mem} in the spike generation module, which is controlled by the external signals BURST and ADAP and the capacitor voltage $V_{Cu}(t)$. The external signals BURST and ADAP control the on and off of M12–M13 and M14–M15, respectively, while $V_{Cu}(t)$ controls Iu4 in response to $V_{Cu}(t)$ via M14.

(2) Synapse Circuit

In the Pavlov experiments, the main research targets are the excitatory synapses. They generate the excitatory current I_{EPSC} to stimulate the activation of the post-neuron.

An excitatory synapse is presented in Figure 2, which models the synaptic response behavior as a first-order linear system. The input spike applied to the V_{pre} node is integrated into I_{EPSC}, which obeys the following dynamic equation:

$$\tau_{syn}\frac{dI_{EPSC}}{dt} + I_{EPSC} = I_w \quad (3)$$

where I_{EPSC} is the synapse output current, I_w is a current set by V_w, and τ_{syn} is the synapse time constant with the hidden capacitance C_{syn}.

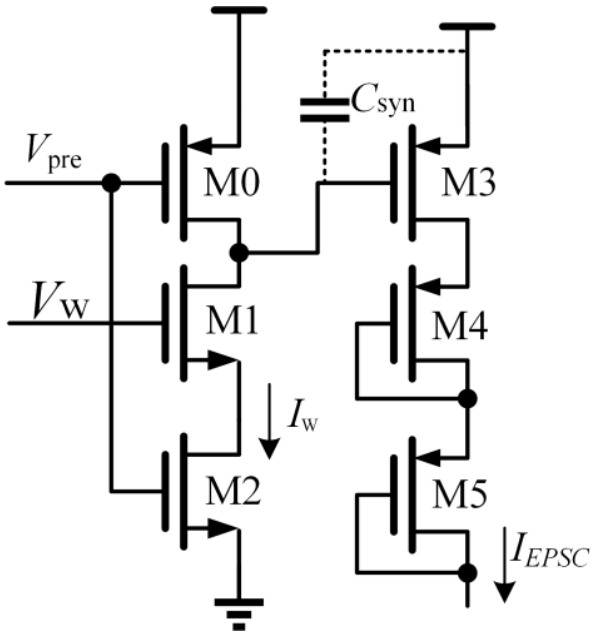


Figure 2. Excitatory synapse.

In this paper, the synapse weights V_w are binary logic (0 or 1.8 V), which can be adjusted between 0 and 1.8 V according to the SDSP regulation mechanism circuit. When V_w is high (1.8 V), the synaptic circuit generates the excitation current I_{EPSC} to charge the capacitor C_{mem} of the posterior neuron during the interval when V_{SPIKE} is high. When V_w is low (0 V), the synapse circuit is off, and no excitation current I_{EPSC} is generated. Therefore, the weight of the synapse circuit indicates the connection between the neurons. When the synapse weight is 1.8 V, the neurons at both ends of the synapse are connected; otherwise, there is no connection between the two ends of the circuit.

(3) Spike-Based Learning Algorithm

The structure of the spike-driven synaptic plasticity (SDSP) learning algorithm is shown in Figure 3. It consists of three blocks: (1) a spike monitoring circuit simulating neuron activity by monitoring the spike frequency; (2) a weight control circuit used for evaluating the algorithm's weight update and "stop-learning" condition; and (3) the bi-stable weight update circuit adjusting the synapse weight according to the real-time status of the weight [9].

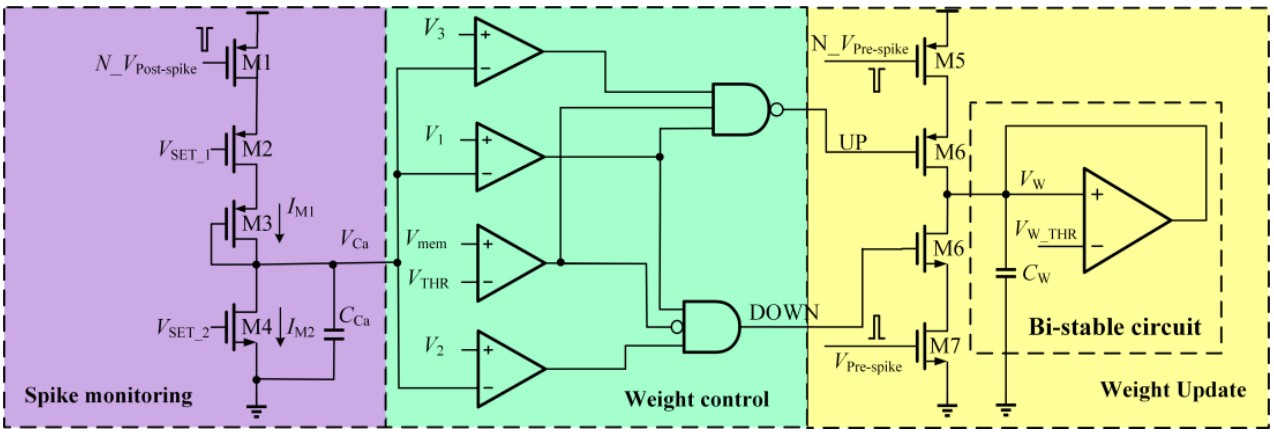


Figure 3. SDSP learning algorithm circuits.

As shown in Figure 3, when the post-neuron spike $V_{Post\text{-}spike}$ arrives, the branch M1-M3 generates a current I_{M1} to charge the capacitor C_{Ca} and pull V_{Ca} up to a high level; when it is absent, the transistor M4 generates a current I_{M2} to pull V_{Ca} down to a low level. V_{SET1} and V_{SET2} control the charge and discharge speeds of C_{Ca}, respectively, so that the voltage V_{Ca} is proportional to the spike frequency generated by the post-neuron. The voltage V_{Ca} through the comparator circuit of the weight control block generates the digital signals UP (active low) and DOWN (active high) and is used to control the adjustment direction of synaptic weight. V_{mem} represents the post-neuron's membrane potential, and V_{THR} is a threshold term that determines whether the weight should be increased or decreased; the terms V_1, V_2, and V_3 are three fixed thresholds that determine the conditions in which the weights should be increased, decreased, or not updated. In the bi-stable weight update block, upon the arrival of each pre-neuron spike, synapse weight increases if the signal UP is low and the signal DOWN is high, and in other situations, the weight should not be updated. In parallel with the instantaneous weight update, the weight is constantly being driven toward one of two stable states through a bi-stable circuit, depending on whether it is above or below a given threshold voltage V_{W_THR}.

The learning algorithm updates the synapse weight according to the timing sequence of the pre-neuron spike, the state of the post-synaptic neuron's membrane potential, and its recent spiking activity. The specific structure can be referred to in Figure 4.

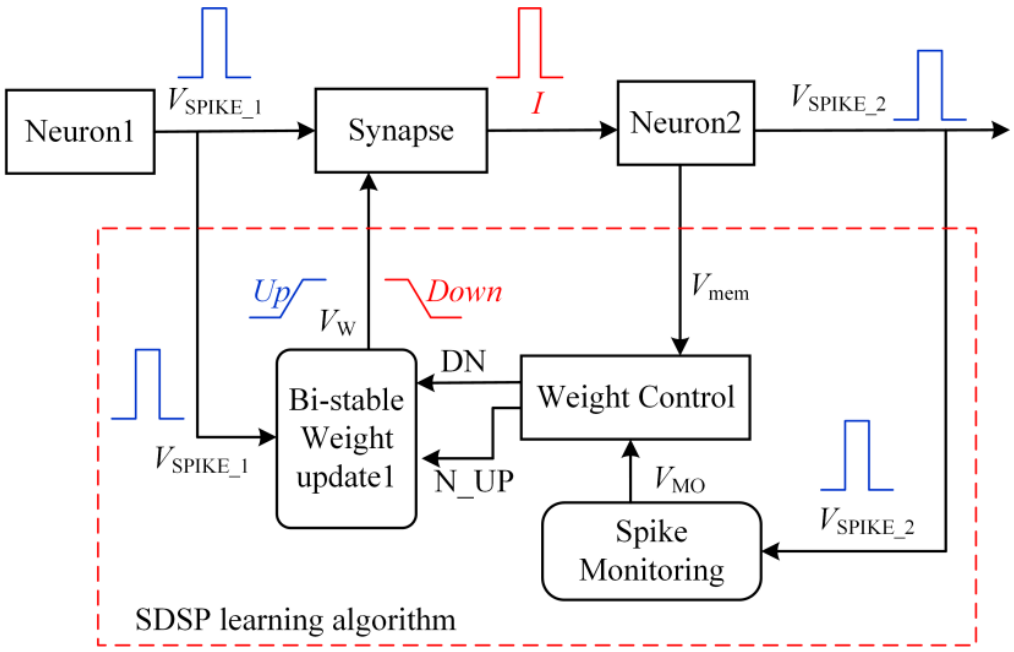


Figure 4. SDSP learning algorithm structure.

When the output spike signal V_{SPIKE_1} from the pre-synaptic neuron is high, the SDSP regulates the synaptic weights by means of Equation (4). Otherwise, the SDSP pulls $V_W(t)$ toward the steady-state V_{MAX} (1.8 V) or V_{MIN} (0 V) via Equation (5). When V_{MO} is not within the range shown in Equation (4) (V_1–V_2 vs. V_1–V_3), the SDSP algorithm does not regulate the synaptic weights, which prevents the neural network from over-regulating the synaptic weights during the learning process.

$$\begin{cases} V_{\mathrm{W}}(t) = V_{\mathrm{W}}(t-\Delta t) + \Delta V_{\mathrm{W\_UP}} & \text{if and} \quad V_{\mathrm{mem}}(t) > V_{\mathrm{MEM\_THR}} \\ & \quad V_1 < V_{\mathrm{MO}} < V_3 \\ V_{\mathrm{W}}(t) = V_{\mathrm{W}}(t-\Delta t) - \Delta V_{\mathrm{W\_DN}} & \text{if and} \quad V_{\mathrm{mem}}(t) < V_{\mathrm{MEM\_THR}} \\ & \quad V_1 < V_{\mathrm{MO}} < V_2 \end{cases} \tag{4}$$

$$\begin{cases} \frac{\mathrm{d}V_{\mathrm{W}}(t)}{\mathrm{d}t} = +V_{\mathrm{Pull\_UP}} & \text{if and} \quad V_{\mathrm{W}}(t) > V_{\mathrm{W\_THR}} \\ & \quad V_{\mathrm{W}}(t) < V_{\mathrm{MAX}} \\ \frac{\mathrm{d}V_{\mathrm{W}}(t)}{\mathrm{d}t} = -V_{\mathrm{Pull\_DN}} & \text{if and} \quad V_{\mathrm{W}}(t) < V_{\mathrm{W\_THR}} \\ & \quad V_{\mathrm{W}}(t) > V_{\mathrm{MIN}} \end{cases} \tag{5}$$

ΔV_{W_UP} and ΔV_{W_DN} are the amounts of change in the synaptic weights during regulation. V_1, V_2, and V_3 are 300 mV, 900 mV, and 1.5 V, respectively; V_{W_THR}, V_{MAX}, and V_{MIN} are 900 mV, 1.8 V, and 0 V, respectively.

2.3. Mixed-Signal Pavlov SNN

The main building blocks of the Pavlov SNN circuit in the mixed-signal implementation are shown in Figure 5. It consists of three parts: (1) the spike neuron circuit with three Izhikevich models; (2) two long-term configurable plasticity synapse circuits; (3) spike-driven synaptic plasticity (SDSP) learning algorithm circuits to control the synapses. A mixed-signal analog–digital crosstalk-free characteristic was achieved. The plasticity synapse circuit that realizes biologically realistic response properties and spiking neurons can exhibit a wide range of SNN behaviors [8].

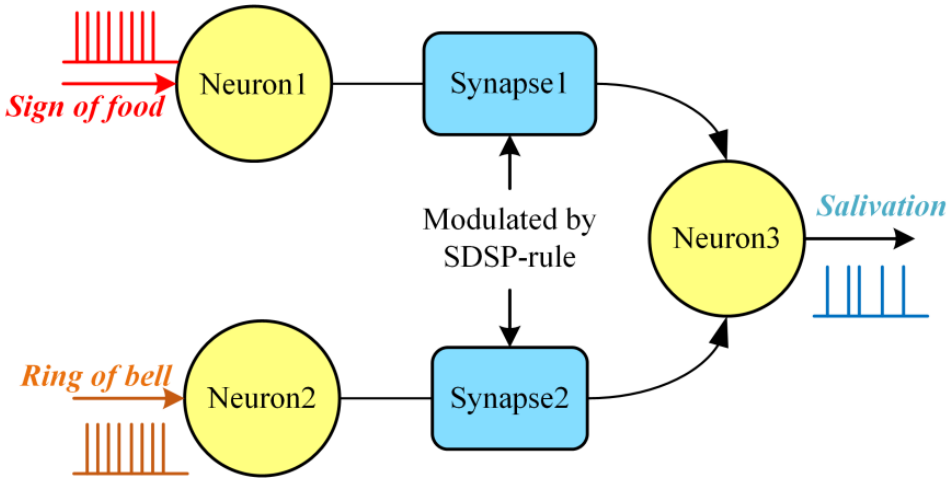


Figure 5. Pavlov SNN network model.

The Pavlov learning process can be classified into three categories as follows:

(a) Before learning: with just the bell stimulus, neuron 3 has no spike response, while neuron 3 provides a spike response with only the food stimulus. (b) Learning stage: the bell stimulus and food stimulus are applied simultaneously; neuron 3 produces a spike response, and neurons 1 and 2 establish associative learning. (c) After learning: the bell stimulus makes a spike response by neuron 3, which is consistent with the Pavlov experiment.The simulation results of Pavlov's experiment can be divided into four parts, as shown in Figure 6.

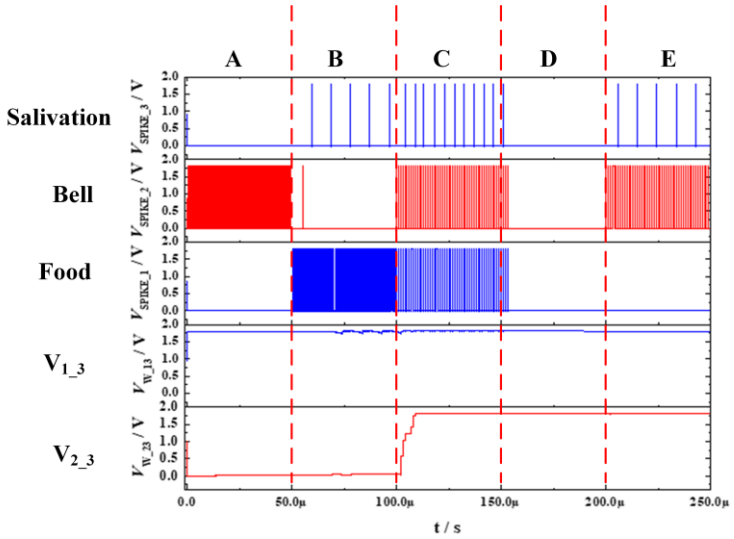


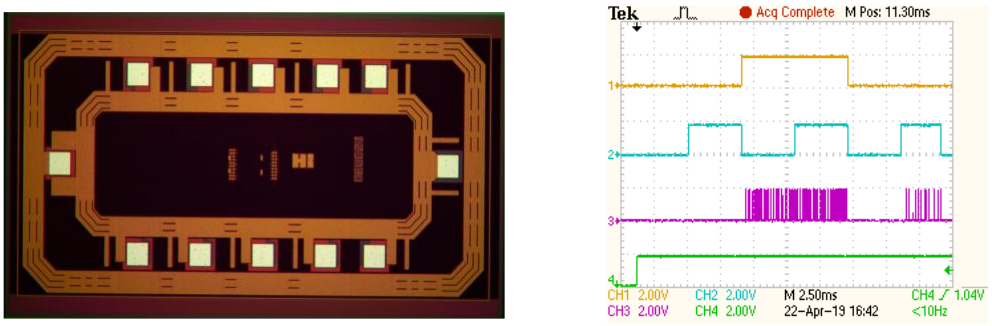
Figure 6. Pavlov SNN network simulation result. The simulation time is divided into five parts "A–E" in units of 50 microseconds.

(A) With just the bell stimulus, neuron 3 had no spike response. Obviously, the salivation signal did not correlate with the bell signal in any way. (B) With just the food stimulus, neuron 3 had a spike response, and there was an intrinsic link between the salivation signal and the bell signal. V_{1_3} is 1.8 V, representing a strong connection between neuron 1 and neuron 3. This is because stage C established a strong connection between neuron 2 and neuron 3. (C) When the bell stimulus and food stimulus were applied at the same time, V_{2_3} gradually increased from 0 to 1.8 V, which represented the process of establishing a connection between neuron 2 and neuron 3. (D) No input, no output. (E) With just the bell stimulus, neuron 3 had a spike response. This is because stage C established a strong connection between neuron 2 and neuron 3.

Pavlov's experiment was characterized by the establishment of connections between signals that were otherwise unconnected.

2.4. Prototype and Test

The prototype was fabricated with a 1P5M 180 nm PD-SOI process. It occupied a chip area of 2.5 × 1.5 mm^2. Figure 7a shows the chip micrograph. The typical power supply was 1.8 V. The experimental results are shown in Figure 7b. Channels 1, 2, 3, and 4 were the neuron 1 input stimuli (a sign of food), the neuron 2 input stimulus (ringing of the bell), the neuron 3 output signal Vspike3 (salivation), and the enable signal (sim_test). After learning, the post-neuron (neuron 3) could emit spikes only under stimulation of the second pre-neuron (neuron 2), verifying its feasibility.



(**a**) (**b**)

Figure 7. (**a**) Micrograph (**b**) test result of the Pavlov SNN chip.

3. Experimental Results and Discussion of Radiation-Hardening Techniques

3.1. Experimental Results

The TID radiation experiment was carried out at the ^{60}Co laboratory, Peking University, at room temperature. The device under test (DUT) was packaged within a printed circuit board (PCB), which was held by the supporting structure. The radiation dose rate was 100 rad (Si)/s, and the total doses were set at 300 krad (Si), 500 krad (Si), and 1 Mrad (Si). The gamma radiation facility and the test board are shown in Figure 8.

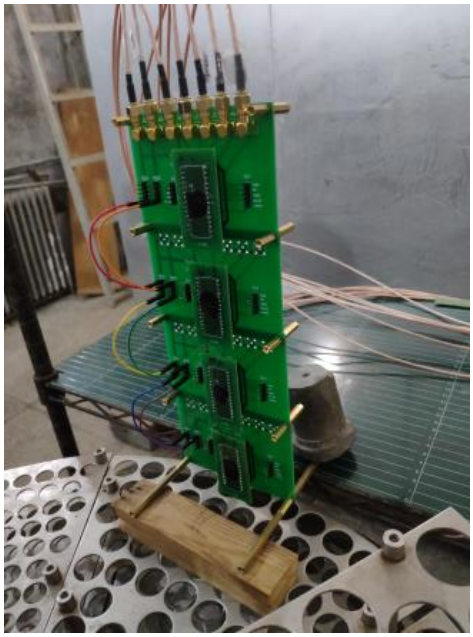


Figure 8. Gamma radiation facilities and the test board.

The SNN chip was tested immediately, within 30 min after irradiation, to avoid an annealing effect. The important signals that are influenced by the total dose are shown in Figure 9. As the dose increased, the output spike rate and the spike amplitude of neuron 3 decreased gradually (channel 3), and the spike monitoring signal of neuron 3 decreased (channel 4); the reason for this was the insufficient charging of capacitors in the neurons. A detailed analysis follows.

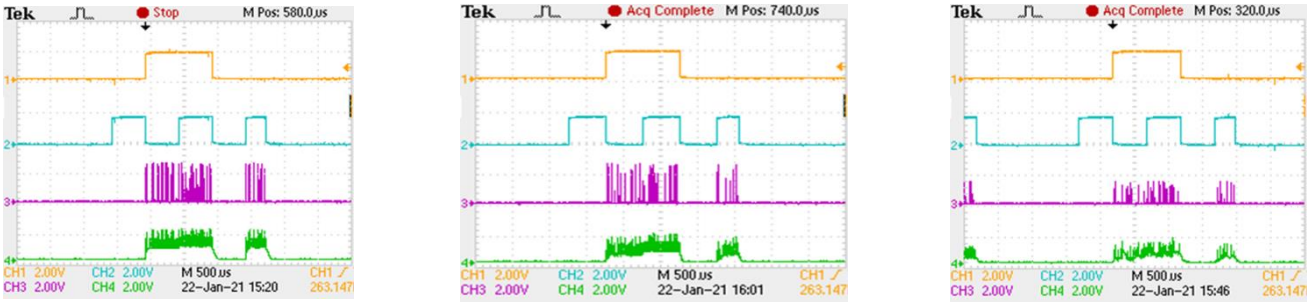


Figure 9. Test results of the Pavlov SNN chip (from left to right: TID 300 krad (Si), 500 krad (Si), 1 Mrad (Si)).

The spike information transmitted in the SNN did not have substantial differences in terms of amplitude and width, which can be regarded as a series of points over time. However, the spike rate is extremely important for the information coding and communication of the SNN.

Within a certain window of time, the neuron received the same stimulus. Its spike sequence pattern was time-dependent, whereas the average number of spikes sent out was the same, i.e., the average spike rate was the same, leading to the success of the information coding and communication. In the same time window, the average output spike rate of neuron 3 decreased gradually as the dose increased, and the spike monitoring signal of neuron 3 decreased, as shown in Figure 10. A critical issue was introduced by the charge trapped in the BOX and the leakage current of the SOI device.

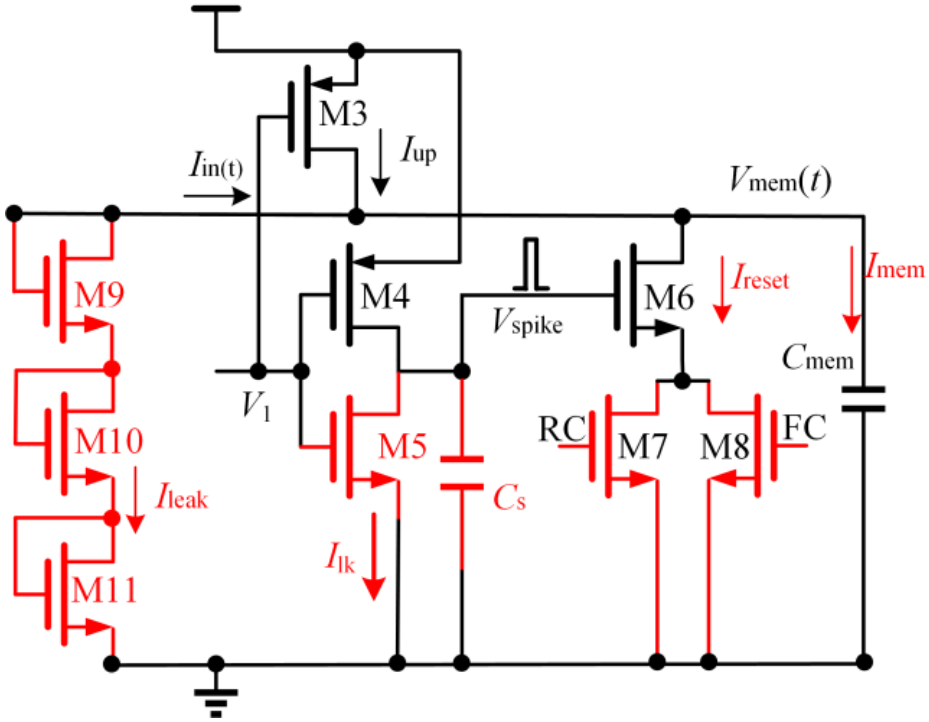


Figure 10. Injection current analysis of neuron after irradiation.

The pathway of the neuron circuit in relation to the membrane voltage is shown in Figure 8. The injection current of neuron membrane capacitance can be expressed as $I_{mem} = I_{in}(t) - I_{leak} - I_{reset}$. On one hand, as the TID-induced leakage current I_{leak} increased, the current I_{mem} decreased, leading to a decrease in the spike frequency. On the other hand, with the increase in the current across the channel (M6–M8), the neuron membrane capacitance took a longer time to charge. The neuron refractory period became longer, and the output spike frequency decreased as well. Therefore, the TID effect seriously affects the spike coding and information transmission across the SNN system.

As shown in Figure 11, I_{M1} and I_{M2} control the charge and discharge speed of C_{Ca}; in terms of charging current, the reduction in the output spike frequency led to a reduction in the current I_{M1}. In terms of leakage current, the leakage current caused by TID led to an increase in I_{M2}. As a result, the balance of the capacitor Cca circuit was broken, and the variation in the monitoring signal swung at a lower value.

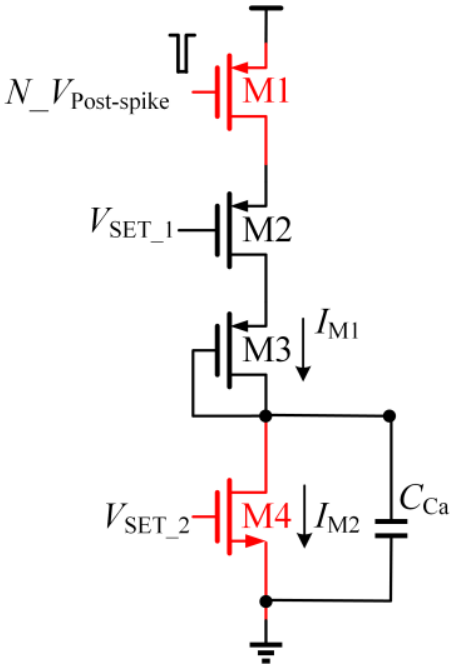


Figure 11. Spike monitoring module after irradiation.

Obviously, the sensitive nodes of the circuit are all related to capacitance. The imbalance between charging and discharging of the capacitor after irradiation is the main cause of the output variation.

3.2. Discussion of Radiation-Hardening Techniques

The leakage current is a critical issue for the SNN circuit under radiation. To alleviate leakage-induced degradation, we considered the rad-hard schemes in terms of the circuit.

Because the synapse current is proportional to the spike frequency of the pre-neuron, by setting the size of the transistor in the synapse circuit, the pre-neuron membrane capacitor and post-neuron membrane capacitor can help to achieve the same charging voltage under the same spike frequency. Therefore, we added a monitoring module to the input layer, as shown in Figure 12.

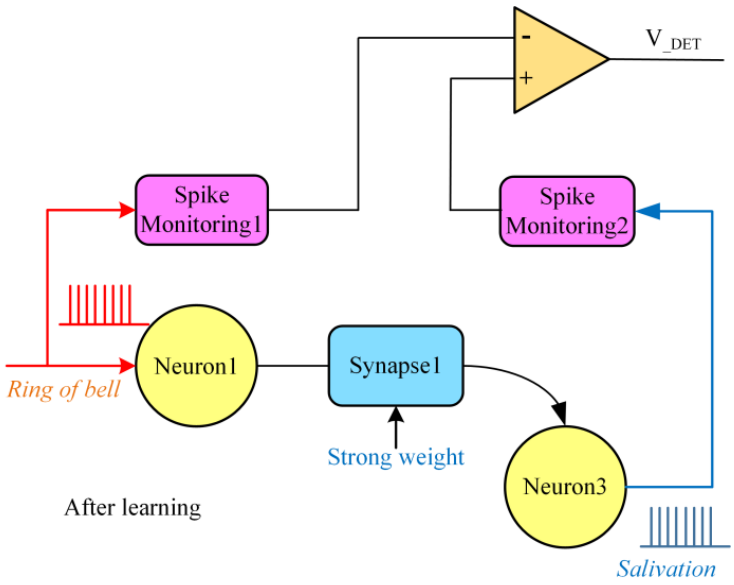


Figure 12. Circuit for radiation monitoring.

After learning, the weak weight of synapse 1 becomes strong, and a salivation signal can be generated by the ring of a bell without a sign of food. Without a signal decrease due to radiation, the pulses of the salivation signal and the bell signal should correspond one-to-one. Consequently, if the output of the comparator ($V_{\_DET}$) is low voltage, it means that the neuron circuit is affected by radiation. Moreover, the signal at the output usually travels through several buffers and has a stronger drive power, so $V_{\_DET}$ should always be high in the absence of radiation.

Although the leakage current cannot be reduced, the circuit can be restored by increasing the charging current of the membrane capacitor. The structure of the neuron circuit itself dictates that its output frequency is positively correlated with the input current, and as the input current increases, so does the output frequency of the neuron.

As shown in Figure 13, if the value of $V_{\_DET}$ is at a low level, it means that the neuron circuit is affected by radiation; then, the analog switch is changed, and the body bias of PMOS is set to a lower voltage to achieve a higher charge current. Otherwise, the body bias has to be connected to VDD without the help of the radiation-tolerant circuit. Of course, the change in body voltage brings with it a slight increase in leakage and power consumption.

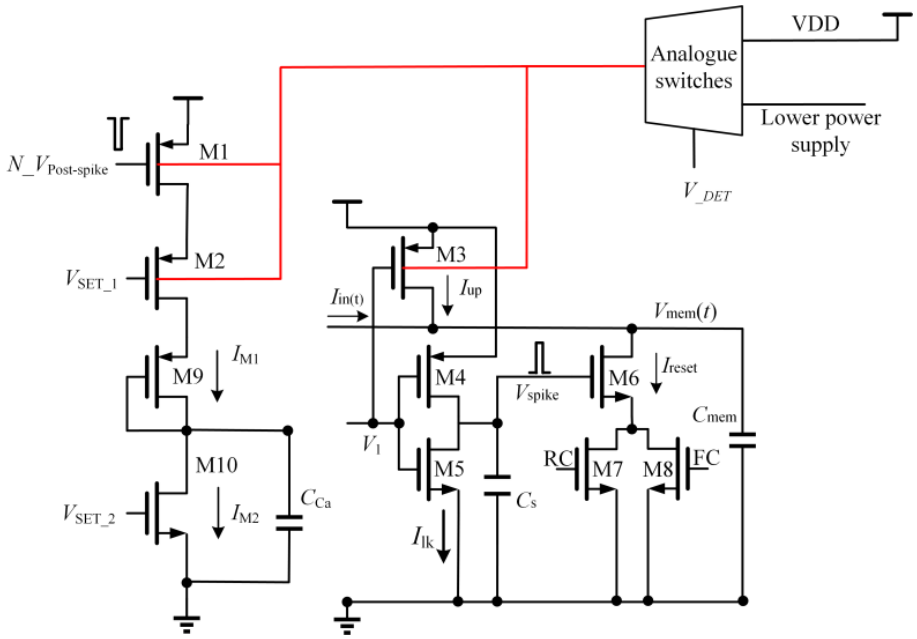


Figure 13. Radiation tolerance circuit for spike amplitude decay.

As shown in Figure 14, an additional auxiliary charging module is also worth considering. If the value of $V_{\_DET}$ is at a low level, meaning that the neuron circuit is under the influence of radiation, then the current mirror is turned on, and the neuron membrane capacitor receives an additional charging current Ic, which can increase the output spike frequency of the neuron. In fact, similar structures have been applied to the design of neurons in the sub-threshold region [10]. The advantage of this structure is the ability to accurately supplement the current, and its disadvantage is that it requires an additional analog bias voltage.

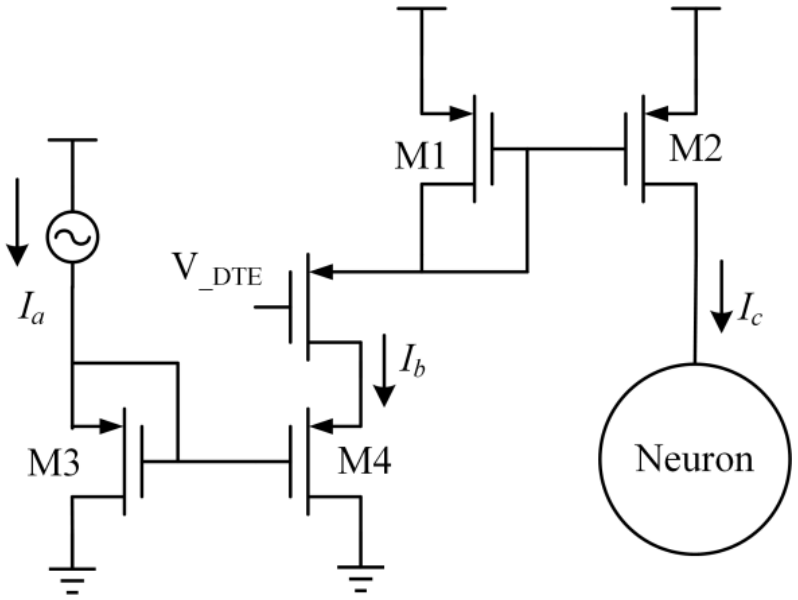


Figure 14. Radiation tolerance circuit for spike frequency decay.

Furthermore, we propose two hardening schemes from the perspective of layout technique: one is to widen the distance between the active regions, and the other is to increase the length of the extremely sensitive transistors.

To evaluate the sensitivity of the circuit to irradiation, we ran a series of Monte Carlo simulations. We performed this analysis with 500 runs for this neuron circuit, with DC current injected into the LEAK block and with bias voltages set to obtain a firing rate of approximately 100 Hz while switching OFF the spike frequency adaptation circuit.

The results of the Monte Carlo analysis with 500 runs showed that the neuron's mean firing rate was centered at 101.9 Hz. Furthermore, its standard deviation was 8.9 with a relative error of firing rate (Std Dev/Mean) of 8.8%, as shown in Figure 15.

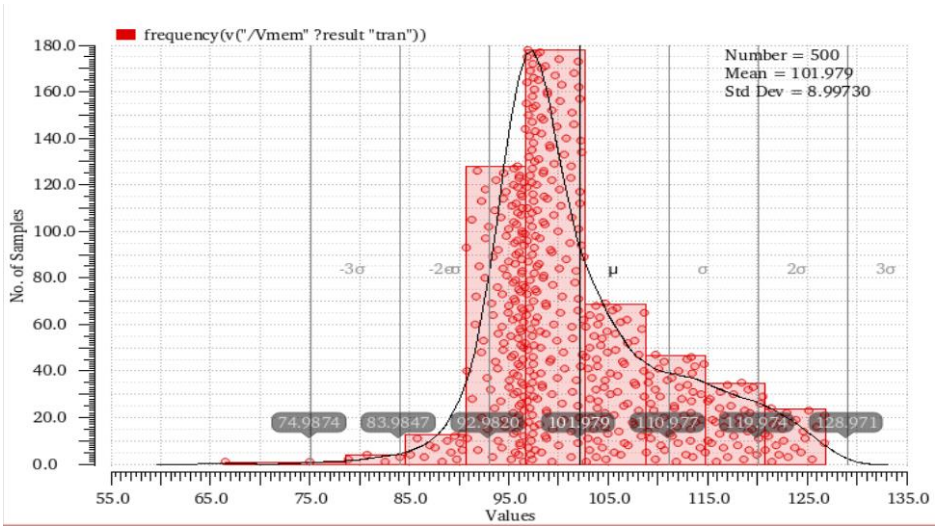


Figure 15. Monte Carlo analysis results.

4. Conclusions

This paper demonstrated the SOI-based mixed-signal Pavlov SNN chip and discusses its TID effect. The experimental results indicate that the average output spike frequency and the spike amplitude of the neuron decrease as the radiation dose increases. The effects of radiation on related circuits and sensitive transistors were identified. A deep insight is that the leakage compensation circuit of the capacitor is one of the critical building blocks for radiation-hardening SNN. Several approaches to guarantee a better tolerance to radiation are proposed in terms of the circuit and layout.

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