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Electronically Tunable Full Wave Precision Rectifier Using DVCCTAs

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Abstract: This work presents a Voltage mode scheme of a full-wave precision rectifier circuit using an analog building block differential Voltage current conveyor transconductance amplifier (DVCCTA) including five NMOS transistors. The proposed design is essentially suited for low Voltage and high-frequency input signals. The operation of the proposed rectifier design depends upon the region of operation of NMOS transistors. The output waveform of the presented rectifier design can be made electronically tunable by controlling the bias Voltage. The functional correctness and Verification of the presented design are performed using 0.25-µm TSMC technology under the supply Voltage of ±1.5 V. The absence of a resistor leads to a minimal parasitic effect. To obtain further insight on the robustness of the circuit, a Monte Carlo simulation and corner analysis are also presented. The circuit is Verified experimentally by incorporating a breadboard model with the help of commercially available ICs CA3080 (operational transconductance amplifier) and AD844AN (current feedback operational amplifier) and offers remarkable compliance with both theoretical and simulation outcomes. The presented design has been laid out on Cadence Virtuoso, which consumes a chip area of 9044 µm^2.

Keywords: current mode circuit; full-wave rectifier; DVCCTA; high input impedance; low output impedance

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1. Introduction

Rectifiers are Very common in analog signal conditioning and processing circuits and have potential applications in areas such as AC Voltmeter, ammeter, wattmeter, RF demodulator, averaging circuit, polarity, and peak detectors [1]. The rectifier using a diode is not capable of rectifying the low-level signal having an amplitude less than the threshold Voltage of silicon and germanium. A precision full-wave rectifier circuit implemented using an operational amplifier can also be implemented with a View to overcoming threshold Voltage issues. The op-amp-based design can rectify the low-level signal amplitude without facing the threshold problem. However, the limitation of the slew rate offered by an op-amp distorts the signal at the output of the rectifier. Therefore, the op-amp-based rectifier design is not suitable for solving the threshold Voltage issue due to the small signal transient [2]. The small-signal transient problem can be resolved by using the current mode approach since it provides a higher slew rate over Voltage-mode counterparts. The precision rectifier implemented using current-mode analog building

block can be used to overcome the small-signal transient problem and can be operated at low Voltage, high frequencies, and also provides tunability features.

Several rectifier designs are reported in the literature based on Various active blocks using a Voltage/current mode [2–22] approach for the full-wave rectifier. A full-wave rectifier circuit using one second-generation current conveyor (CCII) and one current mirror as an active element with two grounded and two floating resistors are reported in [2], but the design does not provide low output impedance and does not have tunability features. The rectifier circuit in [3] employs two CCII with four diodes and a few grounded and floating resistors but does not provide low output impedance. In [4], the rectifier circuit is designed using three current-controlled conveyors (CCCII) with more resistors but does not provide low output impedance. The rectifier circuit presented in [5] consists of one operational transconductance amplifier (OTA) with four diodes, one grounded and floating resistor each, but does not provide low output impedance as well as high input impedance. In [6], two CCII and three NMOS transistors are used to design the rectifier circuit but do not provide high input impedance and low output impedance. A rectifier circuit is presented in [7] using one Dual-X current conveyor with three NMOS transistors to provide high input impedance, but does not provide low output impedance. The rectifier circuit is presented in [8] using one CCII and one OA with three resistors. A minimal precision configuration full-wave rectifier circuit using two different types of active block namely CCII and universal Voltage conveyor (UVC) along with two diodes and a few resistors is used in [9]. Recently, a new Versatile precision full-wave rectifier circuit was reported in [10] using a current or Voltage conveyor as an active element with two diodes but it requires an additional Voltage reference. In [11,12], two CCII and four diodes are used to design the rectifier circuit, but do not provide low output impedance. A rectifier design is presented in [13] using two second-generation current conveyors (CCII), one PMOS transistor, one Voltage follower (VF) along with two floating/grounded resistors but do not provide high input impedance. In [14], one negative type CCII, two diodes, and one floating/grounded each resistor are used, but it also fails to provide high input impedance as well as low output impedance. In [15], high input impedance and low output impedance are achieved by using one CCII but an additional 28 MOS transistors are used with one grounded resistor and does not provide tunability features. In [16], two differential Voltage current conveyors (DVCC) and in [17] two current feedback operational amplifiers (CFOA) are used to implement rectifier, having high input impedance and low output impedance but the output Voltage is not tunable. The tunability features of precision rectifier design are not available in [2–17]. In [18], Voltage mode electronically tunable full-wave rectifier circuit is presented using a multi-output current controlled conveyor (MO-CCCII) and capable of tunability but neither offers a high input impedance nor a low output impedance since the circuit is designed using BJT techniques and uses one zero-crossing detector. High input impedance and low output impedance can be achieved in [8,9,15–17], as mentioned in Section 8, while other existing rectifier designs do not provide both features. The rectifier design presented in [6,7,17] does not require any passive elements for their circuit implementation. Moreover, recent articles in the literature [19–24] address the design of the rectifier, but do not provide tunability features. In [25], the current mode precision rectifier design is presented using EXCCII, but the circuit does not provide tunability features. A current-mode full-wave rectifier circuit using DDCC along with three passive resistors is presented in [26]. The full-wave precision rectifiers presented in [27,28] do not provide high input impedance and low output impedance. Moreover, it is worth mentioning that the rectifier circuit in [25–28] does not provide tunability features. In [29], two OTA and DVCC based rectifier circuits have been demonstrated using diode and few grounded resistors. A full wave rectifier design has been presented in [30] consisting of CCCII active block, however no experimental Verification of the circuit is provided. In [31], the presented rectifier design is complex consisting of several BJT based ICs. CMOS based precision rectifier design has been presented in [32] consisting of current comparator, current mirrors and diodes. In [33], the rectifier circuit consists of three OTAs as active elements with few

grounded resistors. The rectifier design in [34] consists of an OTRA block with several passive floating resistors. A diode based rectifier design has been presented in [35] using CDTA block as an active element. A current mode precision rectifier has been presented in [36] using an improved Wilson current mirror. Most of the rectifier circuits in [29–36] are not capable of providing tunability features.

The work carried out in this paper proposes a new precision full-wave rectifier circuit using two DVCCTA active blocks and five NMOS transistors and demonstrates its performance. The objective of the proposed full-wave rectifier is to provide high input impedance as well as low output impedance by utilizing the features of an analog building block without using passive components. The high input impedance minimizes the loading effect and the low output impedance provides the maximum output load Voltage. These two parameters are important properties of a rectifier to be used with other analog circuits. The proposed design can be made electronically tunable by controlling the output Voltage through the bias Voltage. The tunability feature provides an external parameter to control the rectified output of the proposed model without altering the other parameters of the design. The simulation result Validates the theoretical model of the proposed full-wave rectifier circuit. The circuit is Verified experimentally by making a prototype on a breadboard using commercially available ICs CA3080 (operational transconductance amplifier) and AD844AN (current feedback operational amplifier) and shows good agreement with theoretical and simulation results.

The organization of the paper is as follows: Section 2 provides brief description about the DVCCTA block and its properties. Section 3 describes the proposed full wave rectifier circuit along with its mathematical model. Non-ideal analysis and the effect of parasitic are discussed in Sections 4 and 5 respectively. The Validation of the rectifier design by simulation and experimental results is presented in Sections 6 and 7, respectively. Comparison of the proposed model with the existing literature has been discussed in Section 8. Finally, Section 9 provides the conclusion of the research work.

2. DVCCTA—Building Block and Its Properties

DVCCTA is an active analog hybrid building block designed by cascading differential Voltage current conveyor (DVCC) with an operational transconductance amplifier (OTA) where DVCC is a differential amplifier with unity gain feedback and current mirror [23,24]. The symbol of DVCCTA is shown in Figure 1. The impedance at input terminal Y_1 and Y_2 are Very high, so that the current through these terminals is zero. Terminal X provides the difference between the Voltages appearing at terminals Y_1 and Y_2. The same current flows through both Z and X terminals. Transconductance (g_m) is responsible for converting the current at terminal O to an analogous Voltage at terminal Z. The tuning of the transconductance can be achieved by external Voltage V_c. Equation (1) denotes the port relationship in matrix form for an ideal DVCCTA:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_Z \\ I_O \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & g_m & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_Z \\ V_O \end{bmatrix} \quad (1)$$

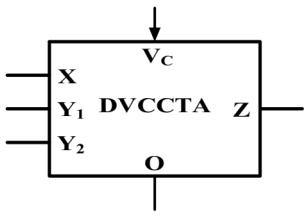

Figure 1. Symbol of DVCCTA.

The CMOS-based internal structure of DVCCTA [23] is shown in Figure 2. The transconductance (g_m) [23] is expressed in (2):

$$g_m = k\{(V_c - V_{ss})/2 - V_t\} \quad (2)$$

where k is μCoxW/L, μ is effective channel electron mobility, Cox represents the per unit area gate oxide capacitance, whereas W/L denotes the aspect ratio of the MOS transistor.

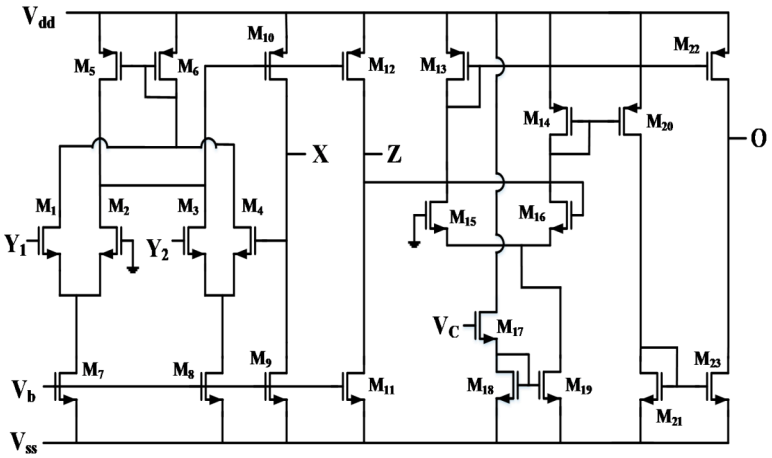

Figure 2. Internal structure of CMOS based DVCCTA.

Every MOS transistors used here are in the saturation region of operation. The rail-to-rail supply Voltage is shown as V_{DD} and V_{SS} respectively for positive and negative Voltage. V_t represents the threshold Voltage of the MOS transistor. The transconductance (g_m) can be controlled by adjusting the bias Voltage V_c. The aspect ratio for MOS transistors used in the DVCCTA design implemented here is shown in Table 1. The simulation is performed using 0.25 μm TSMC process technology with the supply Voltage of ±1.5 V.

Table 1. Aspect ratio of MOS transistors used in DVCCTA.

Transistors	*W* (μm)/*L* (μm)
M_1–M_4	10/0.5
M_5, M_6	5/0.5
M_7, M_8	27/0.5
M_9, M_{11}	44/0.5
M_{10}, M_{12}	8.5/0.5
M_{13}–M_{23}	15/0.5

3. Mathematical Model of the Proposed Full-Wave Rectifier Circuit

In this section, a full-wave rectifier circuit using two DVCCTAs as active current mode building blocks along with five NMOS transistors is proposed as shown in Figure 3. The aspect ratio of NMOS transistors M_A, M_B, M_C, M_{D1}, and M_{D2} are 30/0.5, 25/0.5, 23/0.5, 5/0.5, and 5/0.5 respectively where W and L are in μm. The implementation using transistor M_{D1} and M_{D2} represents an active resistor (R_D) and its resistance can be controlled by using an external terminal (V_g) as shown in Figure 3. The active resistor provides the required resistance without the cost of wasting large area on the chip. The effect of parasitic is least using active resistor compared to passive resistor and also provides relaxation in the matching requirements. Moreover, the resistance can be controlled using the external terminal of active resistor. A sinusoidal input signal Voltage is applied at terminal Y_1 of DVCCTA-1 for rectification. For the positive half-cycle of the applied input signal (V_{in} (t)+), transistor M_A is in the cut-off region, transistors M_B, and M_C is

in the saturation region. The applied input Voltage is conveyed from the terminal Y_1 of DVCCTA-2 to its X terminal using the port relationships given in (1), giving rise to a current through the NMOS transistor M_B. Since the transistor M_A is in the cut-off region, the current through terminal X and Z of DVCCTA-1 is zero. Using the port relationships of DVCCTA given in (1), the same current in the same direction passes through transistor M_B and M_C. The current passing through transistor M_B can be written as:

$$I_{d2} = \frac{K_n}{2}\left[V_{in}(t)_+ + V_{tn} - V_{tn}\right]^2 = \frac{K_n}{2}\left[V_{in}(t)_+\right]^2 \quad (3)$$

where V_{tn} denotes the threshold Voltage and K_n depicts the device parameter of the NMOS transistor. The expression for the current through the transistor M_C can be written as:

$$I_{d3} = \frac{K_n}{2}[V_Z(t) + V_{tn} - V_{tn}]^2 = \frac{K_n}{2}[V_Z(t)]^2 \quad (4)$$

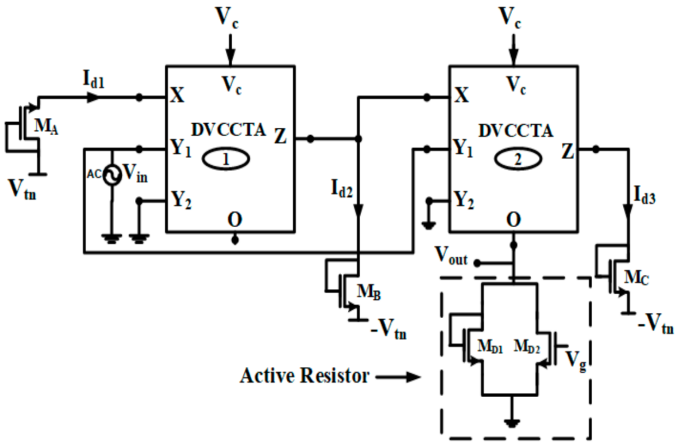

Figure 3. Full-wave rectifier circuit using DVCCTA.

Since the current through transistor M_B and M_C is same, the Voltage appearing at terminal Z of DVCCTA-2 is the same as the positive half-cycle of applied input Voltage and can be written as:

$$V_Z(t) = V_{in}(t)_+ \quad (5)$$

For the negative half-cycle of the applied input Voltage ($V_{in}(t)_-$), transistor M_A, M_B, and M_C are in saturation, cut-off, and saturation region respectively. The applied input Voltage is conveyed from the terminal Y_1 of DVCCTA-1 to its X terminal using the port relationships given in (1) and produces current passing through the NMOS transistor M_A. The same current in the same direction flows across the terminal X and Z of DVCCTA-1. Since the transistor M_B is in the cut-off region, the current through terminal X of DVCCTA-2 is the same as the current through the Z terminal of DVCCTA-1. Using the port relationships given in (1), the current flowing through terminal Z and X of DVCCTA-2 is identical in the same direction. The current passing through transistor M_A can be written as:

$$I_{d1} = \frac{K_n}{2}\left[V_{tn} - V_{in}(t)_- - V_{tn}\right]^2 = \frac{K_n}{2}\left[-V_{in}(t)_-\right]^2 \quad (6)$$

The routine analysis yields the same current through transistor M_A and M_C. The current passing through the transistor M_C is given in (4). The Voltage appearing at terminal Z of DVCCTA-2 can be obtained by manipulating Equations (4) and (6). The Voltage at the Z terminal of DVCCTA-2 is found to be the same as the negative half-cycle of applied input Voltage and can be written as:

$$V_Z(t) = -V_{in}(t)_- \quad (7)$$

Thus, the overall Voltage produced at terminal Z of DVCCTA-2 for a full-wave input signal can be written as:

$$V_Z = |V_{in}(t)| \tag{8}$$

The current produced at terminal O of the second DVCCTA can be written as:

$$I_o = g_m V_z = g_m |V_{in}(t)| \tag{9}$$

The Voltage appearing at terminal O can be written as:

$$V_{out} = g_m R_D |V_{in}(t)| \tag{10}$$

where $R_D = \frac{1}{K_n\left(V_g - 2V_{tn}\right)}$, the resistance offered by NMOS transistor M_{D1} and M_{D2} connected at terminal O of DVCCTA-2. The input signal level must be taken into consideration while implementing the full-wave rectifier circuit using DVCCTA. The presented design of the full-wave rectifier circuit provides high input impedance and low output impedance. The proposed design is capable of providing tunability features and possesses the ability to rectify small-amplitude analog signals.

4. Non-Ideal Analysis of the Proposed Rectifier Circuit

Taking into account the non-ideal gain as a result of the physical implementation of DVCCTA, its port relationships as specified by (1) can be further modified as:

$$V_X = \alpha_i V_{Y1} - \alpha_j V_{Y2};\ I_{Y1} = I_{Y2} = 0;\ I_Z = \beta_i I_X;\ I_0 = \gamma_i g_m V_Z \tag{11}$$

where α_i and α_j are the non-unity Voltage gain, β_i is the non-unity current gain and γ_i is the non-unity transconductance gain. Considering non-ideal current and Voltage gain, (3) can be rewritten as:

$$I_{d2} = \frac{K_n}{2}\left[\alpha_2 V_{in}(t)_+ + V_{tn} - V_{tn}\right]^2 = \frac{K_n}{2}{\alpha_2}^2\left[V_{in}(t)_+\right]^2 \tag{12}$$

The potential at terminal Z of DVCCTA-2 for positive half-cycle using Equations (4), (11) and (12) can be expressed as:

$$V_Z = \alpha_2\sqrt{\beta}_2 V_{in}(t)_+ \tag{13}$$

For the negative half-cycle of the applied input Voltage, (6) can be rewritten as:

$$I_{d1} = \frac{K_n}{2}\left[V_{tn} - \alpha_1 V_{in}(t)_- - V_{tn}\right]^2 = \frac{K_n}{2}{\alpha_1}^2\left[-V_{in}(t)_-\right]^2 \tag{14}$$

The Voltage at terminal Z of DVCCTA-2 for negative half-cycle using Equations (4), (11), and (14) can be written as:

$$V_Z = -\alpha_1\sqrt{\beta_1\beta}_2 V_{in}(t)_- \tag{15}$$

Thus, the overall Voltage produced at terminal Z of DVCCTA-2 for a full-wave input signal can be written as:

$$V_Z = \alpha_2\sqrt{\beta_2} V_{in}(t)_+ - \alpha_1\sqrt{\beta_1\beta_2} V_{in}(t)_- \tag{16}$$

Considering the non-ideal gain, Equation (10) can be modified as:

$$V_{out} = g_m R_D \gamma_2\left\{\alpha_2\sqrt{\beta_2} V_{in}(t)_+ - \alpha_1\sqrt{\beta_1\beta_2} V_{in}(t)_-\right\} \tag{17}$$

It can be observed from the above equation that the gain obtained in the positive and negative half-cycle of the applied input Voltage signal is not identical. So, keen attention

must be paid while implementing DVCCTA to make sure that the output Voltage is given by (10) is met. To compensate for the non-unity gain α_i, β_i, and γ_i, a slight adjustment in the biasing Voltage used to bias the NMOS transistor is needed.

5. Parasitic Analysis of the Proposed Rectifier Circuit

The behavior of the proposed design of the full-wave rectifier will be influenced due to the presence of parasitic resistance and capacitance. R_{X1}, R_{X2}, R_{Z1}, R_{Z2}, R_{Y11}, R_{Y12}, and R_O are the parasitic resistances at terminal X, Z, Y, and O respectively. C_{X1}, C_{X2}, C_{Z1}, C_{Z2}, C_{Y11}, C_{Y12}, and C_O are the parasitic capacitances at the terminal of X, Z, Y, and O respectively. The Value of parasitic resistances and capacitances connected in parallel at Y, Z, and O terminals are R_Y = Very high, R_Z = 190 kΩ, R_O = 175 kΩ, C_Y = 40 fF, C_Z = 0.9 pF, C_O = 12 fF. The parasitic resistance connected in series at X terminal is 11 Ω. The parasitic resistance at the X terminal of DVCCTA has not been considered for the sake of calculation. These resistances will not have much effect at a higher frequency, but make the calculation much more complex.

Considering the parasitic component present at the terminal of DVCCTA as shown in Figure 4, the current I_{d2} and I_{d3} for the positive half-cycle of the applied input signal can be written as:

$$I_{d2} = \frac{K_n}{2}\left[V_{in}(t)_+\right]^2 + \frac{V_{in}(t)_+}{(R_{Z1} \parallel C_{Z1})} \tag{18}$$

$$I_{d3} = \frac{K_n}{2}\left[V_Z(t)\right]^2 + \frac{V_Z(t)}{(R_{Z2} \parallel C_{Z2})} \tag{19}$$

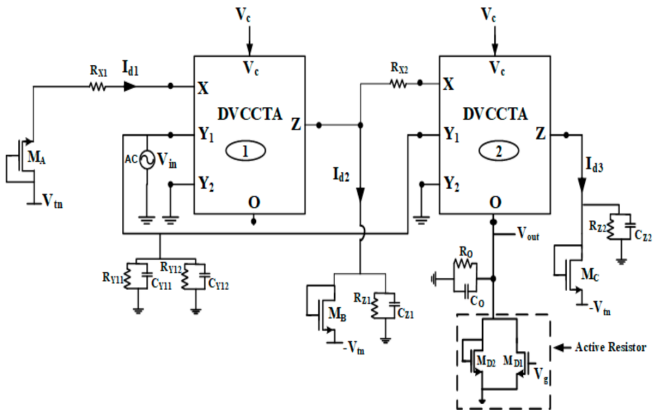

Figure 4. Full-wave rectifier circuit considering parasitic.

Using the port relationships of DVCCTA, the current Equations (18) and (19) are equated and written as:

$$\frac{K_n}{2}\left[V_Z(t)\right]^2 + \frac{V_Z(t)}{(R_{Z2} \parallel C_{Z2})} = \frac{K_n}{2}\left[V_{in}(t)_+\right]^2 + \frac{V_{in}(t)_+}{(R_{Z1} \parallel C_{Z1})} \tag{20}$$

It can be observed that the obtained Equation (20) is non-linear due to the presence of parasitic components for a positive half-cycle. The Voltage at terminal Z of DVCCTA-2 can be written as:

$$V_Z(t) = V_{in}(t)_+ \text{ when } \frac{V_Z(t)}{(R_{Z2} \parallel C_{Z2})} = \frac{V_{in}(t)_+}{(R_{Z1} \parallel C_{Z1})} \tag{21}$$

For the negative half-cycle of the applied input signal, the current I_{d1} can be written as:

$$I_{d1} = \frac{K_n}{2}\left[-V_{in}(t)_-\right]^2 \tag{22}$$

Using the port relationships of DVCCTA, the current Equations (19) and (22) are equated and written as:

$$\frac{K_n}{2}[V_Z(t)]^2 + \frac{V_Z(t)}{(R_{Z2} \parallel C_{Z2})} = \frac{K_n}{2}[-V_{in}(t)_-]^2 \tag{23}$$

It can be observed that the obtained Equation (23) is non-linear due to the presence of parasitic components for the negative half-cycle. The Voltage at terminal Z of DVCCTA-2 can be written as:

$$V_Z(t) = -V_{in}(t)_- \text{ when } \frac{V_Z(t)}{(R_{Z2} \parallel C_{Z2})} = 0 \tag{24}$$

The output of the rectifier circuit using (21) and (23) can be written as:

$$V_O(t) = g_m\{R_D V_Z + V_Z(R_O \parallel C_O)\} \tag{25}$$

When

$$\frac{V_Z(t)}{(R_{Z2} \parallel C_{Z2})} = \frac{Vin(t)_+}{(R_{Z1} \parallel C_{Z1})} \tag{26}$$

It can be observed from (25) that the output of the proposed full-wave rectifier circuit is affected at a higher frequency due to the presence of parasitic components.

6. Simulation Results

This section shows the simulation outcome of the proposed electronically tunable full-wave rectifier circuit simulated using 0.25 µm TSMC CMOS technology having a supply Voltage of ±1.5 V. The internal structure of DVCCTA shown in Figure 2 is used for simulation considering the applied bias Voltage $V_b = -1$ V. The W/L or commonly known as the aspect ratio of transistors used for implementing DVCCTA is provided in Table 1. The threshold Voltage of NMOS transistor M_A, M_B, and M_C used in Figure 3 are 0.425 V, 0.423 V, and 0.44 V respectively are chosen to compensate for the current gain and Voltage gain due to non-ideality as discussed in Section 4. The transconductance parameter of DVCCTA Varied depending on the range of controlling Voltage V_c. The Value of V_c lies in the range of −0.5–0.5 V. The output of the rectifier circuit is obtained from terminal O of DVCCTA-2 by controlling V_g. The Value of the R_D resistor is around 2.5 kΩ. Figure 5 shows the DC Voltage transfer characteristic of the full-wave rectifier circuit at $V_c = 0.5$ V, $V_g = 0.6$ V and it can be observed that the maximum input signal amplitude obtained is approximately 200 mV. The transistor at the input stage of the internal structure of DVCCTA shown in Figure 2 is no longer in the saturation region when the input Voltage lies outside this range.

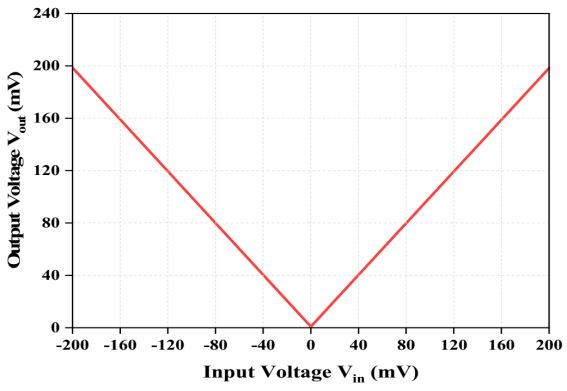

Figure 5. DC Voltage transfer characteristic of the proposed full-wave rectifier circuit.

The transient response of the rectifier circuit is presented in Figures 6–8 considering the magnitude of the applied input signal as 30 mV, 50 mV, and 100 mV, respectively, at

frequency 1 MHz. It can be observed from Figure 6 that the rectified output signal is obtained at V_C = 0.3 V and 0.35 V considering the constant Value of Vg = 0.56 V when the input signal is of 30 mV amplitude at 1 MHz frequency. It can be observed from Figure 7 that the rectified output signal is obtained at V_C = 0.38 V, 0.40 V, and 0.42 V considering the constant Value of Vg = 0.56 V when the amplitude of the applied input signal is 50 mV at 1 MHz frequency. The rectified output coincides with the input signal at V_C = 0.40 V. It can be observed from Figure 8 that the rectified output signal is obtained at V_C = 0.40 V, 0.42 V, and 0.44 V considering the constant Value of Vg = 0.56 V taking input signal as 100 mV in amplitude and having 1 MHz frequency. The rectified output coincides with the input signal at V_C = 0.42 V. It can be observed from Figure 9 that the rectified output signal is obtained at Vg = 0.54 V, 0.56 V, and 0.60 V considering the constant Value of V_C = 0.34 V while using input signal of amplitude 50 mV at 1 MHz frequency. The rectified output coincides with the input signal at Vg = 0.56 V. Figures 6–9 show that the rectified output of the proposed rectifier circuit can be tuned by changing the Value of V_C and Vg. The radical temperature change in the time domain and the DC characteristic is shown in Figure 10.

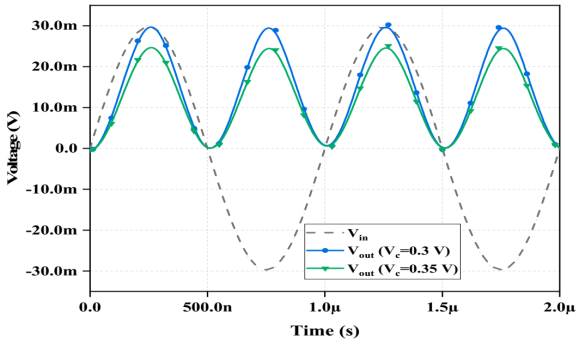

Figure 6. Transient response of full-wave rectifier circuit at frequency f = 1 MHz and V_P = 30 mV considering Variable V_C.

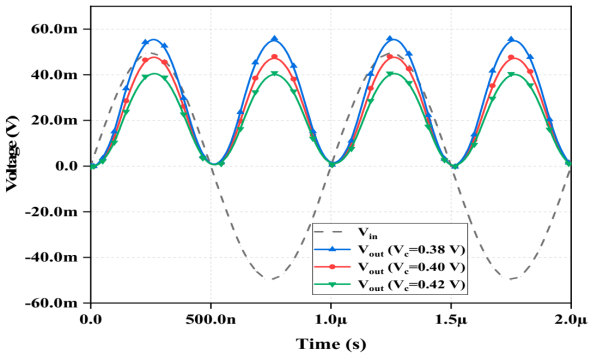

Figure 7. Transient response at frequency f = 1 MHz and V_P = 50 mV considering Variable V_C.

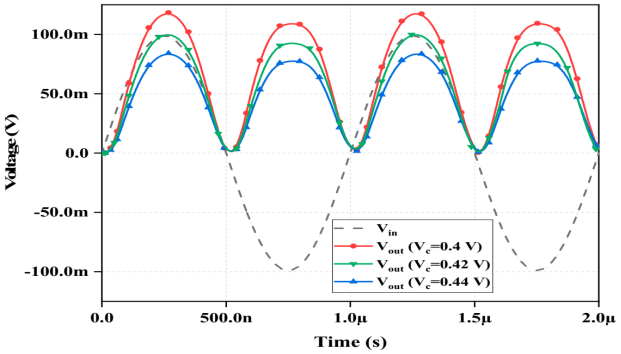

Figure 8. Transient response at frequency f = 1 MHz and V_P = 100 mV considering Variable V_C.

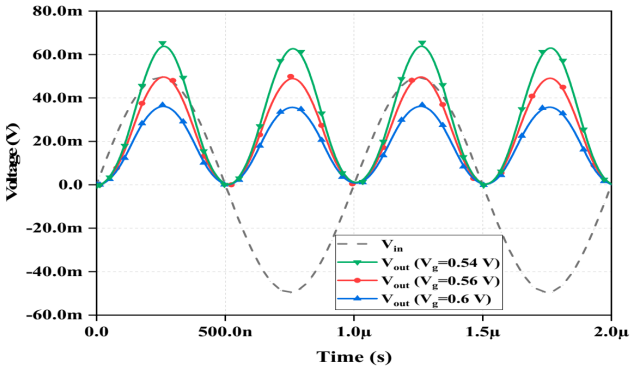

Figure 9. Transient response at frequency f = 1 MHz and V_P = 50 mV considering Variable V_g.

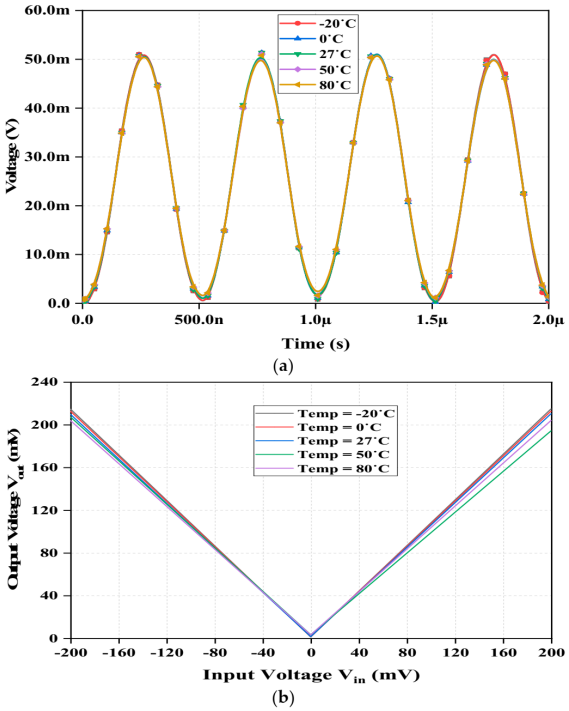

Figure 10. Temperature analysis of the proposed rectifier circuit (**a**) Transient response (**b**) Input and output DC characteristics.

A Variable ambient temperature from −20 to 80 °C is considered to show the robustness of the presented design. It can be observed that the rectified signal amplitude shows a minute deviation with temperature. The performance study that includes the Monte Carlo Sampling simulation offers a unique tool to study and analyze the robustness as well as the uncertainty of the proposed full-wave rectifier circuit for transistor mismatch in the designed circuit when the input signal of amplitude 50 mV is applied at frequency 1 MHz. MCS simulation is done for 200 runs by considering a 3% mismatch in gate oxide thickness (T_{ox}) of all transistors as shown in Figure 11a. The DC Monte Carlo analysis is shown in Figure 11b. It is seen that the rectifier circuit is still operational within acceptable limits despite having a slight deviation in the output response. Corner analyses, such as SS, FF, and TT, have been carried out as shown in Figure 12 and even these analyses show that the rectifier circuit presented here is capable of exhibiting superior operational performance. Henceforth, this makes the proposed circuit suitable in operation under radical conditions and over a wide range of temperatures as well. The layout of the proposed full-wave rectifier circuit is created and depicted as shown in Figure 13 and post-layout simulation has been done to present the effect of the involved parasitics on the overall performance of the rectifier circuit. It covers an overall layout area of 9044 µm^2 (133 µm × 68 µm). It

can be observed from Figure 13c that the transient response of the pre and post-layout simulation differs slightly with respect to one another which clearly shows the effects of parasitic in the design. Due to the presence of significant interconnection resistance, the distributed resistance and parasitic capacitance will influence the overall performance of the rectifier design and even lead to delays between pre- and post-layout results. The important performance parameter of the rectifier circuit is the DC Value transfer (P_{DC}) and RMS error (P_{RMS}) [27,28], which are used to show the accuracy of the rectifier. In the ideal case, the Values of P_{DC} and P_{RMS} should be 1 and 0, respectively. The simulation results of P_{DC} and P_{RMS} have been shown in Figure 14. It can be seen that the deviations in the actual output Voltage can be observed by increasing the frequency and decreasing the magnitude of the input signal. The P_{DC} decreases below one and P_{RMS} increases when the magnitude of the input signal decreases from 100 mV to 10 mV. The simulation results obtained at frequency 1 MHz and V_{in} = 100 mV have been compared with the results provided in [8,29,31] as shown in Figure 15 and it can be observed that [8] responds slowly and has a dead zone due to the presence of diode. Initially, [29] shows phase difference compared to the input signal, and [31] shows Variations in the magnitude of the output response.

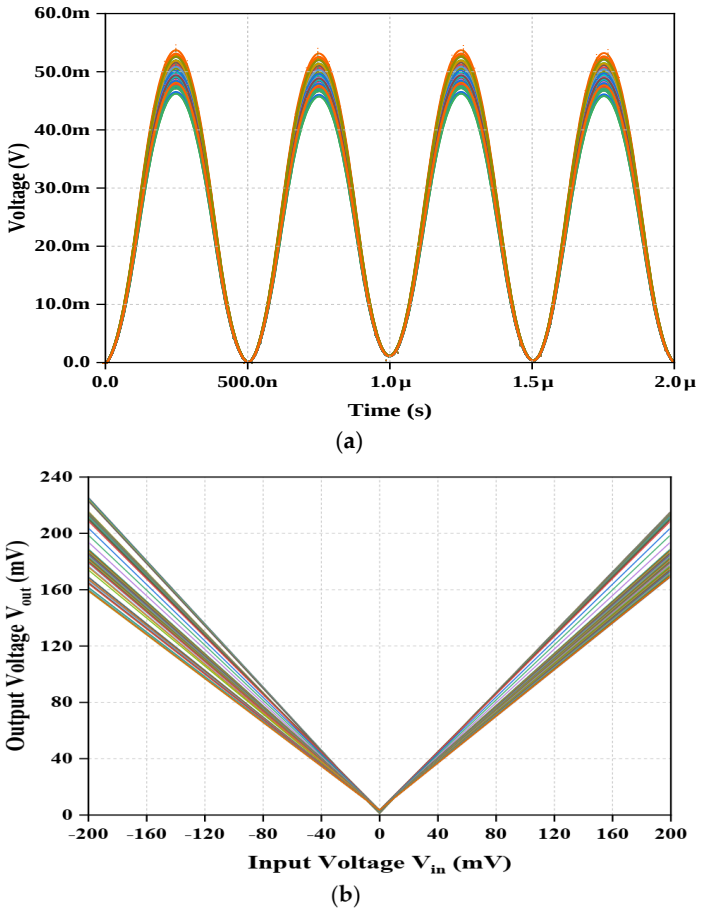

Figure 11. Monte Carlo sampling response of the presented rectifier circuit (**a**) Time response (**b**) Input-output DC characteristics.

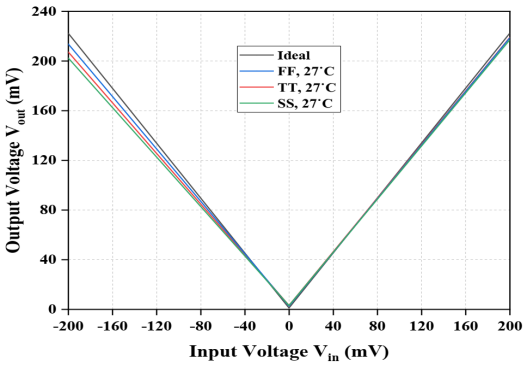

Figure 12. Process corner analysis of the proposed full-wave rectifier circuit.

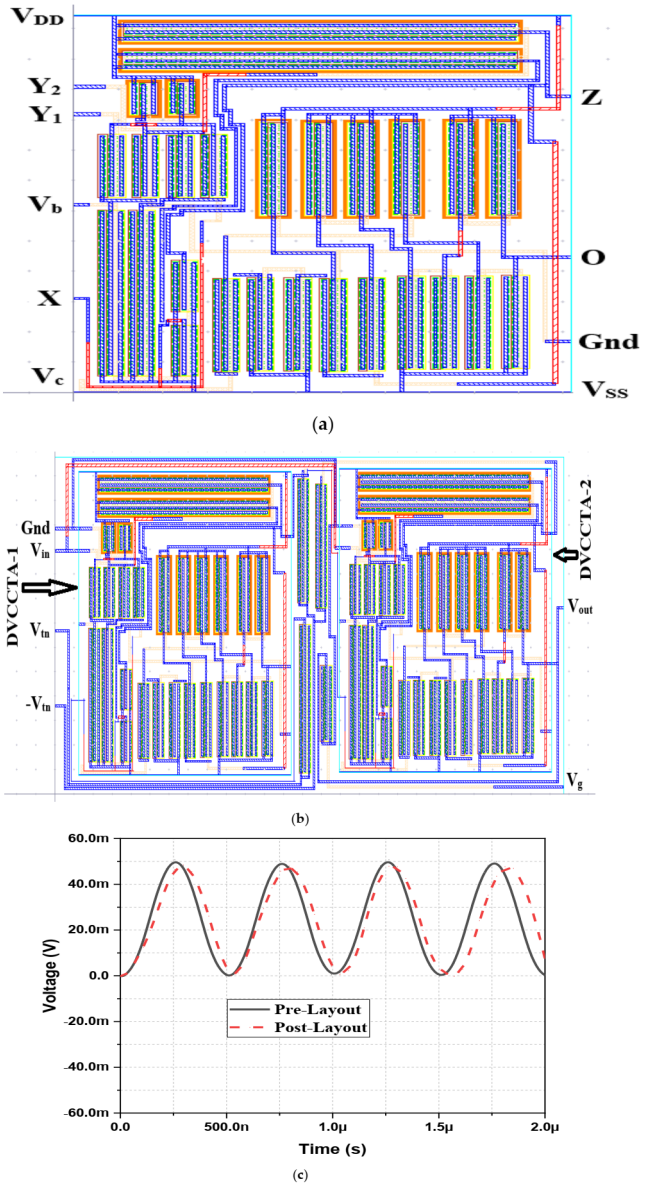

Figure 13. Layout of the proposed rectifier circuit (**a**) Layout of DVCCTA (**b**) Layout of the full-wave rectifier (**c**) Transient response of pre and post-layout simulation.

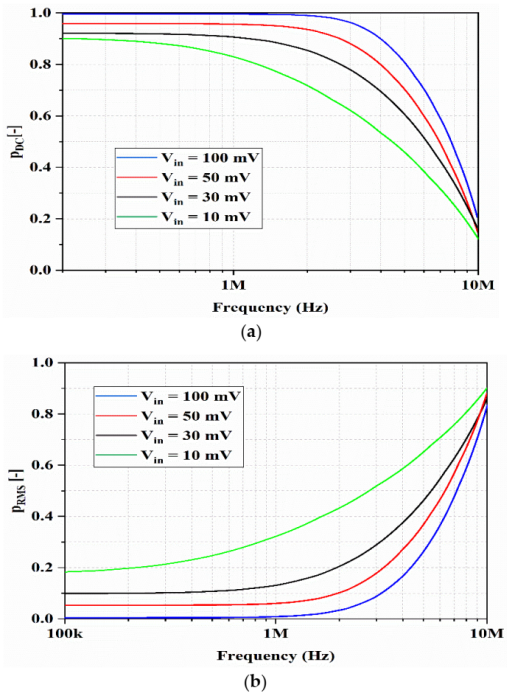

Figure 14. (**a**) Transfer Value P_{DC} for different input signal magnitude (**b**) RMS error P_{RMS} for different input signal magnitude.

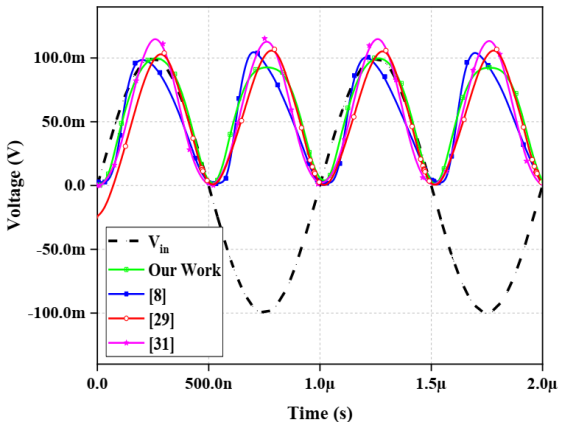

Figure 15. Comparison of simulation results obtained for [8,29,31] with presented rectifier design at frequency 1 MHz and V_{in} = 100 mV.

7. Experimental Results

Since the monolithic IC of DVCCTA is not commercially available, the presented electronically tunable full-wave rectifier circuit based on the current-mode scheme was implemented on the breadboard, using commercially available CA3080 and AD844AN circuits to experimentally justify the operation of the circuit. The MOS-based rectifier design as shown in Figure 3 is implemented using the macro model circuit consisting of commercial ICs for performing the experiment as shown in Figure 16. DVCCTA implementation requires one CA3080 and three AD844AN ICs along with four passive resistors (R), each resistance having a Value of 1 kΩ. Since two DVCCTA blocks are used along with NMOS transistors, a total of six AD844AN and two CA3080 ICs with three NMOS transistors (IRF540N) is required for implementing the experimental prototype. Figure 16a shows the implementation of DVCCTA using commercial ICs. Figure 16b shows the micromodel circuit implementation of the proposed rectifier design using commercial ICs and its implementation on the breadboard is shown in Figure 16c. A sinusoidal input having an amplitude of 50 mV is fed as an input to the circuit and component parameter R_D of 2.2 kΩ

is considered to obtain the output waveform curve as shown in Figure 17. Commonly available Keysight—DSOX3054A digital storage oscilloscope is used for this purpose. The amplitude of the output waveform depends on the bias current and increment in the amplitude is observed with the increment in bias current. The experiment is performed at a frequency of 500 kHz. Commercially available IC CA3080 is current biased (I_B) as shown in the DVCCTA implementation in Figure 17 and it is exploited for Varying the amplitude of the output waveform. It is clearly apparent that the amplitude of the output waveform in the presented precision rectifier Varies in accordance with the bias current of the OTA used in the implementation of DVCCTA.

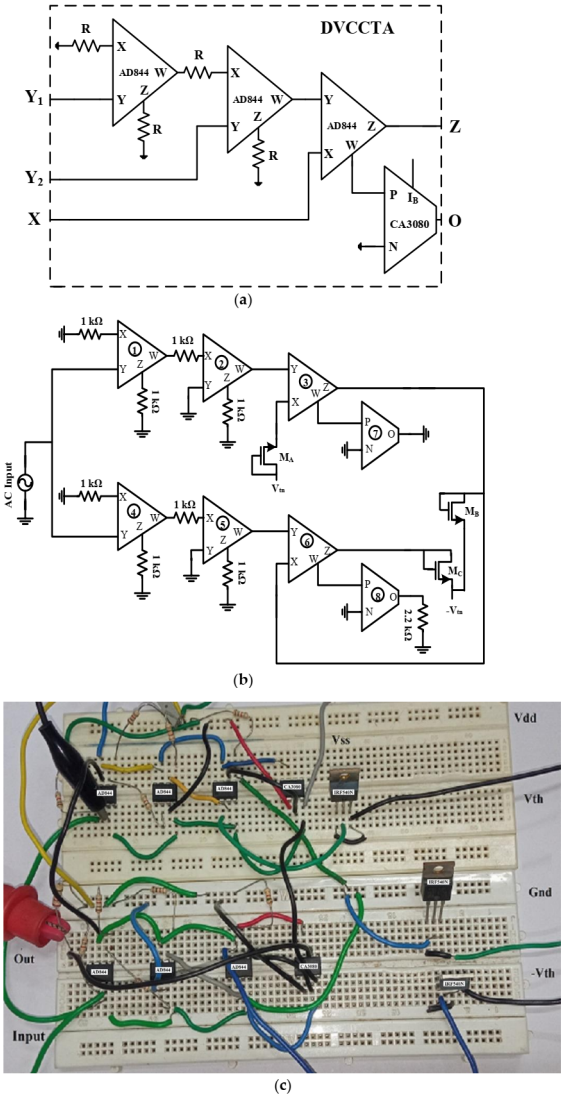

Figure 16. Macro model circuit (**a**) DVCCTA (**b**) Rectifier circuit (**c**) Breadboard implementation using commercial ICs.

It can be observed that the output waveform shows a minute offset owing to the presence of tracking errors, parasitic involved, and mismatch in the transistors. The prototype circuit realized and implemented on a breadboard offers some frequency limitations and it can be noted that the bandwidth in the experimental setup is approximately 2 MHz since these commercial ICs are prone to frequency limitations and parasitic effects arising because of the interconnection between the components.

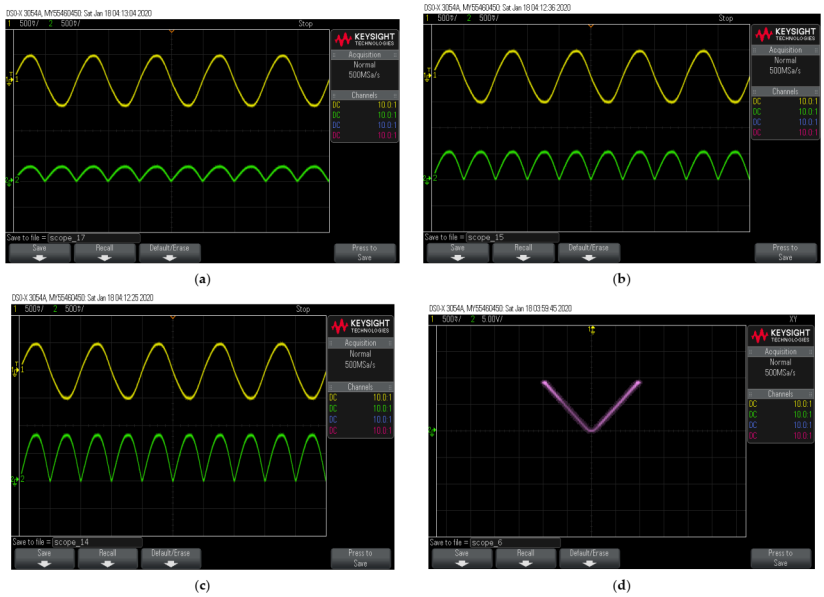

Figure 17. Experimental result obtained using commercial ICs (**a**) At bias current 50 µA (**b**) At bias current 100 µA (**c**) At bias current 200 µA (**d**) DC transfer characteristic.

8. Comparison

The performance of the presented full-wave rectifier circuit is compared with the available existing literature as shown in Table 2 in terms of tunability, the number of passive components, input, and output impedance. As evident from Table 2, the presented design of the full-wave rectifier circuit contains high input impedance along with low output impedance as well. Moreover, it does not require any passive components and provides electronic tunability features. The recent articles in literature [19–22,25–36] present rectifier design, but most of them do not provide tunability features (see Table 2).

Table 2. Comparison of proposed rectifier circuit with existing literature.

Ref. No	Number of Active Components	Tunability	Number of Floating Resistors	Number of Grounded Resistors	High Input Impedance	Low Output Impedance
[2]	1 CCII + 1 CM	No	2	2	Yes	No
[3]	2 CCIIs	No	2	1	Yes	No
[4]	3 CCCIIs	No	5	2	Yes	No
[5]	1 DO-OTA	No	1	1	Yes	No
[6]	2 CCIIs 3 NMOS	No	0	0	No	No
[7]	1 DXCCII 3 NMOS	No	0	0	Yes	No
[8]	1 CCII 1 Op-Amp	No	3	2	Yes	Yes
[9]	1 CCII 1 UVC	No	2	2	Yes	Yes
[10]	1 CCII 1UVC	No	3	3	Yes	No
[11]	2 CCIIs	No	3	1	Yes	No
[12]	2 CCIIs	No	2	1	Yes	No

Table 2. *Cont.*

Ref. No	Number of Active Components	Tunability	Number of Floating Resistors	Number of Grounded Resistors	High Input Impedance	Low Output Impedance
[13]	2 DVCCs 1 NMOS 1 VF	No	3	0	No	Yes
[14]	1 CCII-	No	2	1	No	No
[15]	1 CCII 28 MOS	No	1	1	Yes	Yes
[16]	2 DVCC +	No	2	2	Yes	Yes
[17]	2 CFOAs	No	0	0	Yes	Yes
[18]	1 MO-CCII 1 ZCD 2 MOS	Yes	0	1	No	Yes
[19]	2 VC 2 Diode	No	0	1	Yes	Yes
[20]	1 DO-CCII 12 MOS	No	0	0	No	No
[21]	1 OC 4 CM	No	0	2	NA	NA
[22]	1 DX-CCII 2 MOS	No	1	1	Yes	No
[25]	1 EXCCII 2 MOS	No	0	0	No	No
[26]	1 DDCC 2 MOS	No	0	3	Yes	No
[27]	2 WAT	No	0	0	No	No
[28]	1 CCII 1 DX-CCII 2 Diode	No	1	1	No	No
[29]	1 OTA 2 Diode	Yes	0	2	Yes	No
[30]	1 CCCII 4 MOS	No	0	1	Yes	No
[32]	1 COMP 2 CM 2 Diode	No	0	0	No	No
[33]	1 OTA 2 MOS	Yes	0	2	Yes	No
[34]	3 OTRA 6 MOS	Yes	8	0	No	No
[35]	1 CDTA 4 Diode	Yes	0	1	No	Yes
[36]	2 CM	No	1	0	No	No
Our work	2 DVCCTA 5 NMOS	Yes	0	0	Yes	Yes

9. Conclusions

A precision full-wave rectifier circuit using DVCCTA with five NMOS transistors is presented in this article. The proposed design of the full-wave rectifier circuit offers some useful features, such as tunability, high input impedance, low output impedance, and better

slew rate. Due to the aforementioned features, the circuit designed can be easily cascaded with other Voltage-mode counterparts. The simulation results provide confirmation about the effectiveness of the proposed circuit in operation over a wide range of frequencies. The presented design has a chip area of 9044 μm^2. Moreover, the simulation results and experimental implementation carried out are in agreement with the theoretical model. The impact of non-ideality and tracking errors was assessed to analyze the performance of the proposed rectifier circuit. Moreover, the corner analysis and Monte Carlo sampling were performed to examine the robustness of the presented rectifier circuit design.

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