Journal of
Low Power Electronics and Applications

MDPI

Article

Memristor-Based Loop Filter Design for Phase Locked Loop

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Received: 30 May 2019; Accepted: 26 July 2019; Published: 29 July 2019

Abstract: The main challenge in designing a loop filter for a phase locked loop (PLL) is the physical dimensions of the passive elements used in the circuit that occupy large silicon area. In this paper, the basic features of a charge-controlled memristor are studied and the design procedures for various components of a PLL are examined. Following this, we propose a memristor-based filter design which has its resistance being replaced by a memristor in order to reduce the die area and achieve a low power consumption. We obtained a tuning range of 741–994 MHz, a stable output frequency of 1 GHz from the transfer characteristics of voltage-controlled oscillator (VCO), and an improved settling time. In addition to reduced power consumption and area occupied on the chip, our design shows a high reliability over wider range of temperature variations.

Keywords: filter; hysteresis curve; memristor; phase locked loop; voltage controlled oscillator

1. Introduction

A phase locked loop (PLL) is a mixed-signal feedback system which consists of both analog and digital blocks including the loop filter. Though studies have shown that a voltage-controlled oscillator (VCO) is the most important component of a PLL, the loop filter is equally important because it removes remaining high frequency components in the output of the charge pump and thus stabilizes the control input to the VCO. It is highly notable that PLL applications, in the fields of communications, control systems and power electronics have evolved greatly in recent times. This complements the fact that although the PLL is an old technology, it has proven to be relevant in current trend devices and for future technological advancements. It is, however, desirable to improve the performance of the phase locked loop in terms of its power consumption, tuning range, reliability, lock time, phase noise etc. [1–3]. Apparently, a short frequency hop time would quickly bring the PLL back to normal oscillation when it is shifted to an undesirable frequency. The main goal of this paper was to propose a memristor based filter design for phase locked loop. A loop filter eliminates the high frequency components from the phase comparator so that only the direct current component is provided to the VCO. A memristor is considered a nanoscale device, so it is useful for more applications such as nonvolatile memory applications, low power and remote sensing applications, cross bar latches as transistor replacements, and analog computation and circuit applications [4]. Memristors' ability to maintain a state without requiring external biasing can significantly reduce overall power consumption, while the deep-nanoscale physical dimensions of the device (minimum reported: 5×5 nm) are ideal for its implementation in the field of VLSI (very large-scale integration) [5] and can thus provide a much-needed extension to Gordon Moore's law. Emerging devices, such as memristors, when compared with established elements, tend to manifest advanced properties and often exhibit novel characteristics that can be exploited for enhancing the performance of conventional circuitry (e.g., a loop filter) as well as developing novel designs and applications. In the literature, many memristor-based analog applications have been presented since the announcement of the Helwett

Packard (HP) memristor. Though a memristor is not available yet as a discrete component, the simulation results and analytical models of memristor-based circuits obtained using memristor models available in literature can be used to explain how to design memristor-based filters [6].

2. Memristor

A memristor is considered as a potential candidate for low power circuit design because it can use any value between 0 and 1, unlike conventional devices which use only 0 and 1. The word memristor is derived from two words: MEMory and ResISTOR. It is a passive element similar to fundamental devices like the resistor, inductor, and capacitor, in which these express the relations between voltage and current, flux and current, and voltage and charge, respectively. A memristor, as a component which was first introduced by Leon Chua in 1971 [7], is also considered as the fourth fundamental passive device that expresses the relation between charge and flux [8,9]. Though a memristor could be charge or flux-controlled, we employed a charge-controlled Helwett Packard (HP) titanium oxide (TiO_2) memristor model in this work.

A memristor is said to be charge-controlled if the relation between flux and charge is expressed as a faction of the charge, a property referred to as memristance (M).

$$M(q) = \frac{\mathrm{d}\Phi}{\mathrm{dq}} \tag{1}$$

where ø and q are flux and charge, respectively. Memristance can also be represented in relation to other storage passive elements such as the inductor and capacitor.

The voltage across an inductor and current flowing through a capacitor are described as follows.

$$V_l(t) = L\frac{di}{dt} \tag{2}$$

$$I_c(t) = C\frac{dv}{dt} \tag{3}$$

By combining Equations (2) and (3), we obtain.

$$M(q) = \frac{V_l(t)}{I_c(t)} = \frac{L}{C}\frac{di}{dv} \tag{4}$$

From Equations (1) and (4), it is evident that the memristor is a charge-controlled device.

In order to design a memristor-based loop filter, understanding the behavior of a memristor is paramount. Figure 1 shows equivalent circuit of a memristor for simulation in SPICE. We obtained SPICE simulated results of some of the characteristics of a memristor.

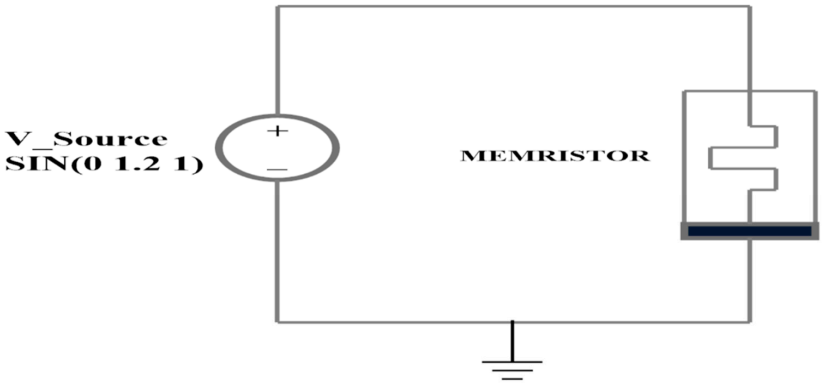
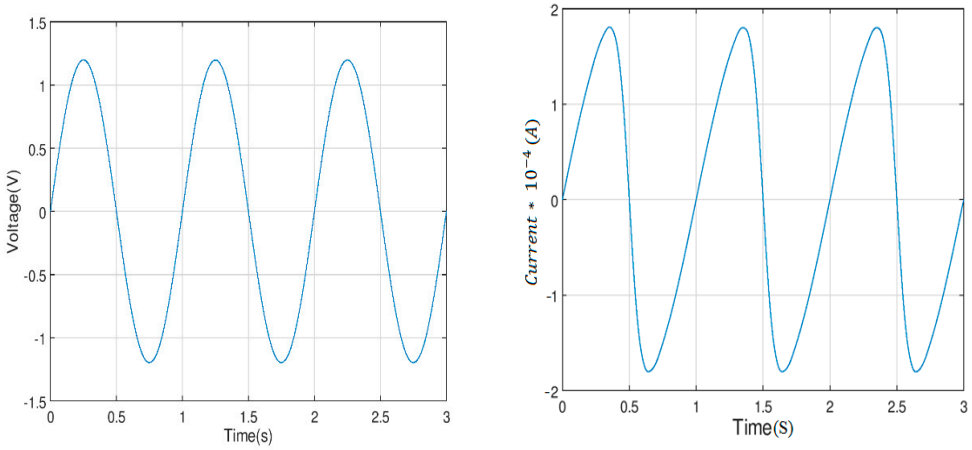


Figure 1. SPICE simulation circuit of the memristor.

Figures 2–5 show the simulation results of a memristor with a sinusoidal input, V_{source} = Asin(wt), where A = 1.2 V and w = 2 π rad/s. However, the basic characteristics of a memristor are described in Figures 3–5.



(**a**) (**b**)

Figure 2. Simulation output of the memristor model: (**a**) Voltage output of the memristor; (**b**) current output of the memristor.

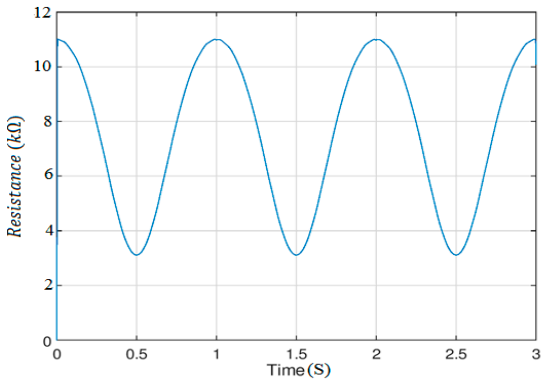


Figure 3. Memristance waveform.

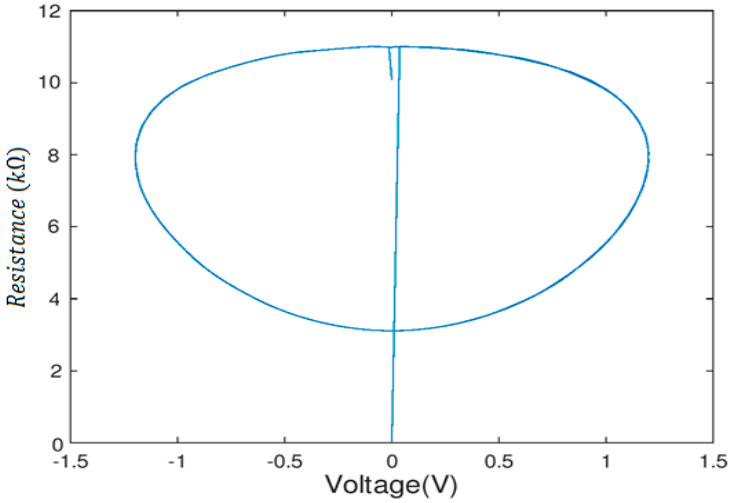


Figure 4. Resistance–voltage loop.

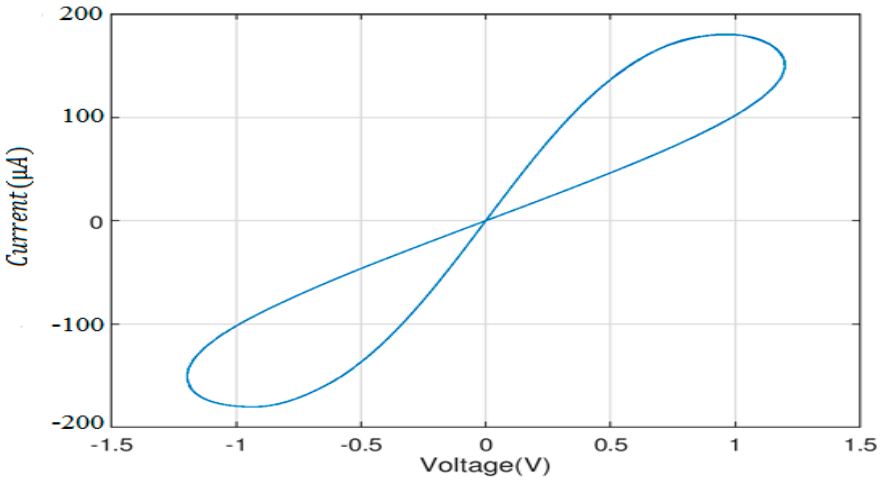


Figure 5. Pinched hysteresis loop of the memristor.

The HP memristor model parameters used are [10,11]: $R_{init} = 11$ kΩ, $R_{ON} = 100$ Ω, $R_{OFF} = 16$ kΩ, D = 10nm, $\mu_v = (10^{-12})$ m^2/V-sec and $p = 10$. The R_{init} *and* p parameters denote the initial resistance and exponent of window function, respectively. R_{ON} is the resistance of the doped memristor and R_{OFF} is for the undoped memristor. D is the width of the thin film and μ_v is the dopant mobility.

Since input voltage and output current have the same zero crossing, as shown in Figure 2, this infers that the memristor is not a voltage storage device.

The resistance versus time characteristics of the memristor are presented in Figure 3. The instantaneous resistance is in the range $[R_{ON}, R_{OFF}]$, depending on the applied voltage. While a memristor can be used at its extreme resistance values in order to provide digital memory, it can also be made to behave in an analog manner. The dynamic negative effect is due to the charge-dependent change in memristor resistance [8]. Similarly, Figure 4 depicts resistance versus voltage characteristics. The memristance value depends not only on the magnitude but also on the sign of $V(t)$. In other words, resistance $[R_{init}, R_{OFF}]$ for $V(t) < 0$ and $[R_{ON}, R_{init}]$ for $V(t) > 0$.

Figure 5 shows the current–voltage characteristics of the memristor, where it exhibits a pinched hysteresis loop. The shape of the pinched hysteresis loop will change with frequency. We see in Figure 6 that the size of hysteresis loops decreases by increasing the frequency. This is due to the fact that the ions have a low mobility and slow inherent motions, and, as such, they finally lose their effectiveness on changing memristor resistance. In this way, the memristor reduces to a simple resistor.

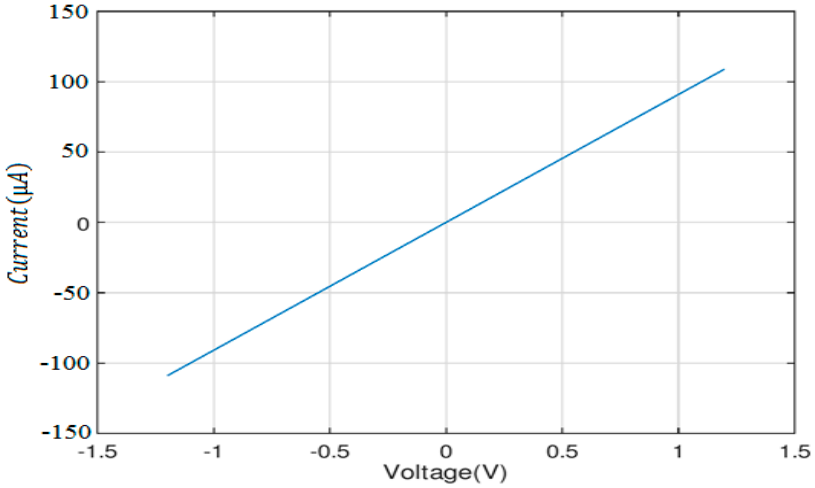


Figure 6. Current (I)–voltage (V) characteristics of the memristor at high frequency.

3. PLL Building Blocks

The architecture of the PLL is shown in Figure 7 In the following, we will describe the building blocks of the PLL.

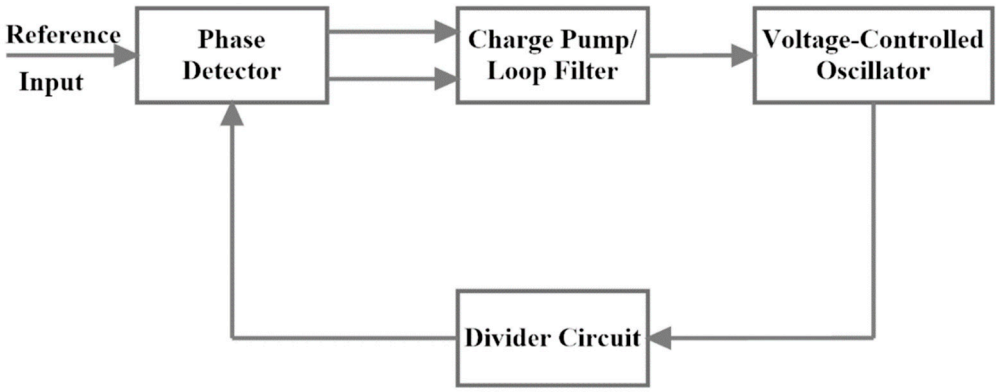


Figure 7. Basic blocks of the phase locked loop (PLL).

3.1. Phase Detector

A phase detector (PD) or phase comparator (PC) detects any phase difference between the off-chip (external) reference input and the clock generated by the frequency divider. A PD is therefore considered as a functional block having an output signal proportional to the phase difference between the two input signals [12]. Figure 8 shows the logic diagram of the phase detector.

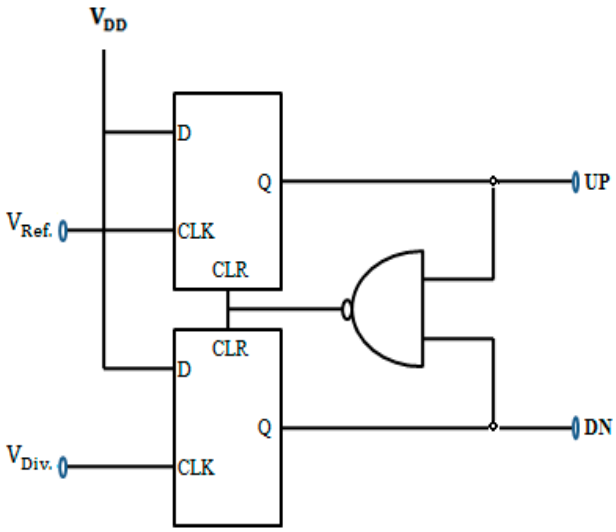


Figure 8. Phase frequency detector.

The UP and DN signals in Figure 8 function as control signals to the charge pump. In this work, the PLL architecture and the phase frequency detector were implemented in a conventional D flip-flop (DFF) based topology. The DFF in Figure 8 was designed using D-latch because it provides a very high speed of operation, considering the minimum transistor size [13], for 0.5 um process technology [14].

When the reference signal is leading or lagging the feedback signal from frequency divider, the difference between the phases of two clock signals is represented by UP or DN pulses, respectively, as shown in Figure 9.

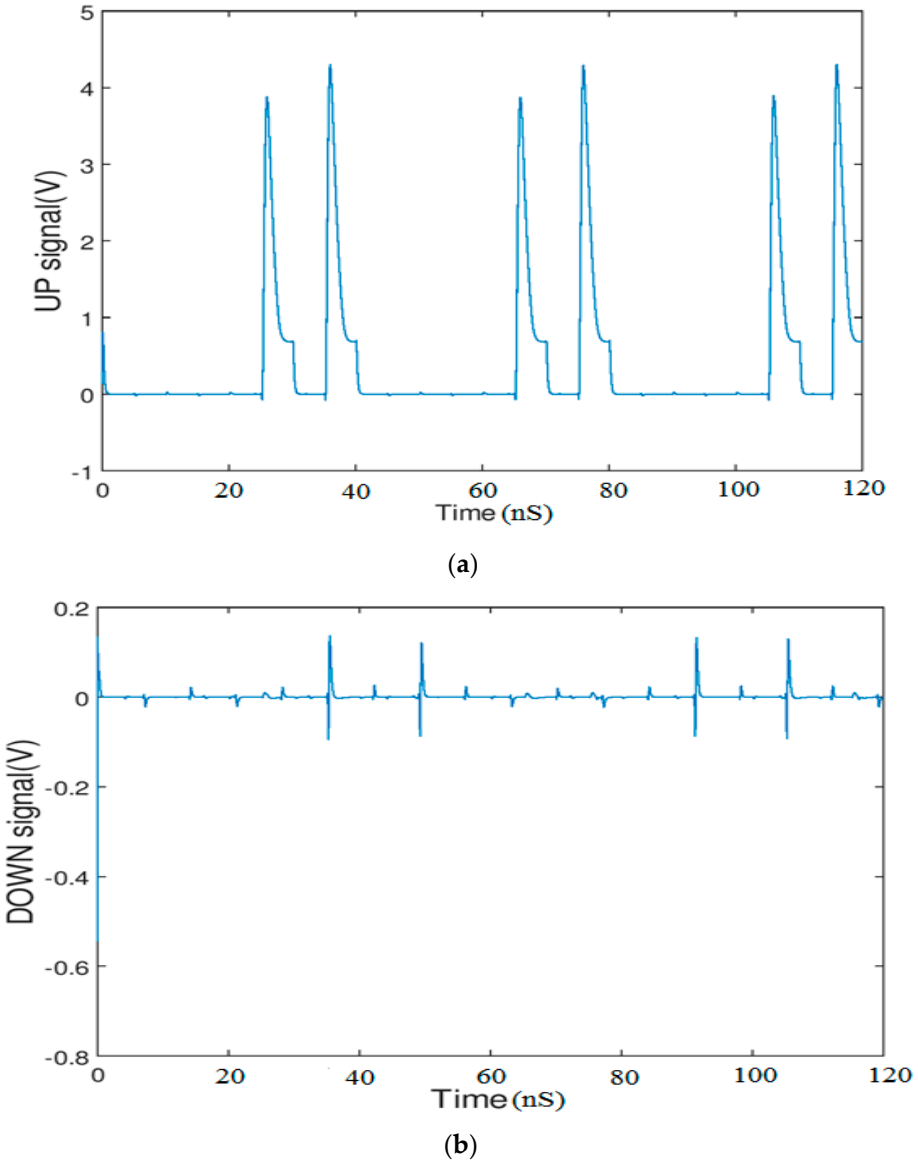


Figure 9. SPICE simulation of phase detector (PD) output waveforms: (**a**) UP signal in Figure 8; (**b**) DOWN signal in Figure 8.

3.2. Charge Pump/Loop Filter

A charge pump, as shown in Figure 10 below, translates the digital UP and DN voltages from the phase detector into a current signal, I_{cp} [15], which is required to charge or discharge the loop filter in order to give the desired control voltage, V_{ctrl}. In Figure 10, the loop resistance is replaced with the memristor. This is because the resistor in the loop filter introduces a ripple in the control voltage of the voltage-controlled oscillator (VCO), even when the loop is locked [14,16,17]. This undesirable ripple may cause a modulation of the VCO output frequency and, therefore, jitter in its output. We showed earlier that the memristor acts like a linear resistor at high frequencies, which makes it suitable for the filter circuit in our proposed phase locked loop design. The memristor, owing to its nanoscale size, occupies less die area and consumes less power. Therefore, the existing analog loop filter circuit topologies with characteristics that depend on resistance can be made with the memristor [18,19]. The tolerance of integrated resistors due to process and temperature variations is large, and this could lead to performance variations of frequency synthesizers using the integrated RC loop filter consisting of

resistor (R) and capacitor (C) network [20]. Furthermore, it might degrade phase margin and even cause loop instability. Hence, the use of the memristor in place of the resistor is desirable.

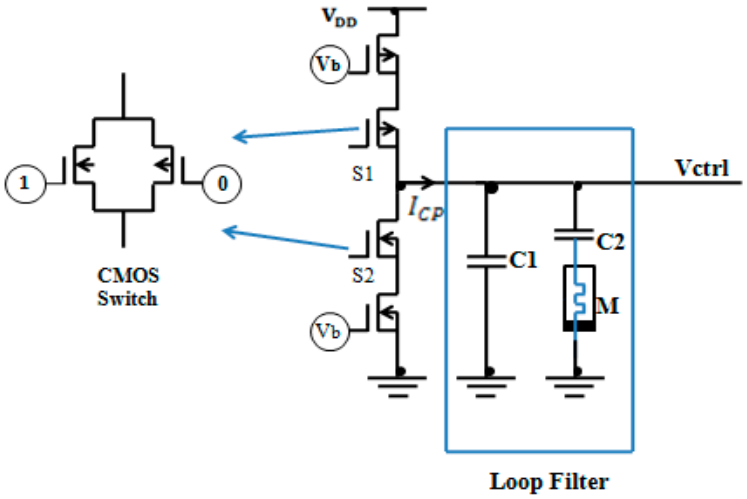


Figure 10. Charge pump/loop filter.

Studies have also shown that the loop filter resistor variation is compensated by using an on-chip bandgap reference voltage and another resistor [21], which incurs a prohibitively large cost for filter design. In this work, we proposed a memristor-based loop filter whose memristance is least affected by process parameter and temperature variations; it also occupies small die area.

Similarly, the wide diversity of memristor characteristics with dependency on frequency and device size makes it a valuable circuit component for various applications, such as the loop filter shown in Figure 10. In addition, memristor technology offers lower heat generation, as it utilizes less energy. As a new nanoscale device, it provides a lot of advantageous features such as high-density, non-volatility, low power and good scalability [22].

From Figure 10, the digital values 1 and 0 in the transmission gates represent UP/DN and inverted signals, respectively. The loop filter is equally highlighted in Figure 10. It integrates the error current to generate control voltage for the VCO. In the loop filter, C_1 is added in parallel to series combination of the memristor, M, and capacitor C_2 to reduce cycle to cycle jitter at the output [23,24]. The output waveform of charge pump/loop filter (CP/LF) is shown in Figure 11.

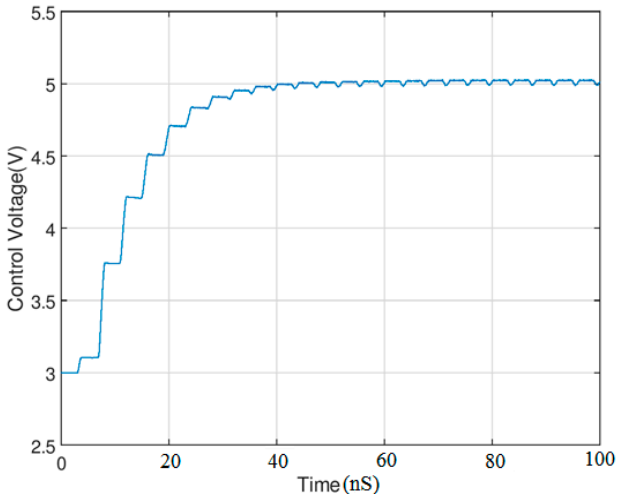


Figure 11. Output waveform of charge pump/loop filter (CP/LF).

Whenever the UP signal is high, it forces the current into the loop filter. Hence, the VCO control voltage rises, as shown in the figure. As shown in Figure 11, we obtained a settling time of 67.89 nS, which is considered shorter than the conventional design using a constant RC loop filter [25]. Additionally, PLLs designed based on the proposed method exhibit less ripple in the VCO control voltage and therefore less jitter in the output.

3.3. Voltage Controlled Oscillator

The voltage-controlled oscillator (VCO) is the most important and complex component of the overall PLL design. In this work, we used single-ended current starved VCO, as shown in Figure 12 [26,27]. The simulation result of the output waveform is shown in Figure 13.

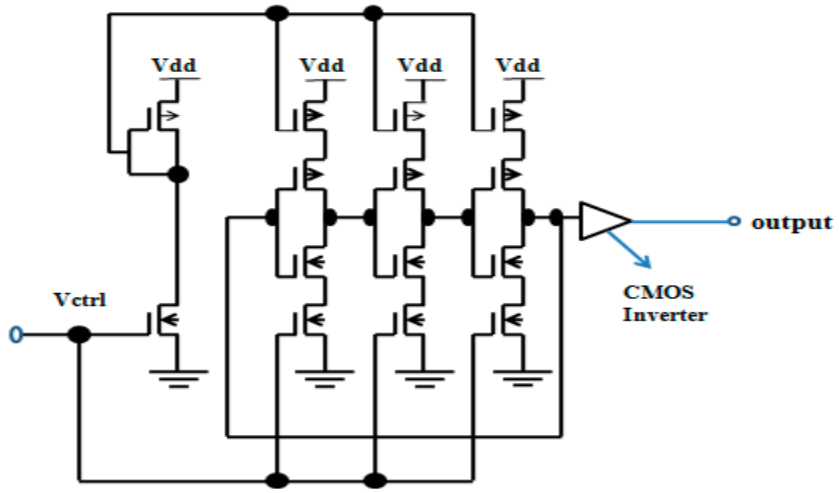


Figure 12. The single-ended current starved voltage-controlled oscillator (VCO).

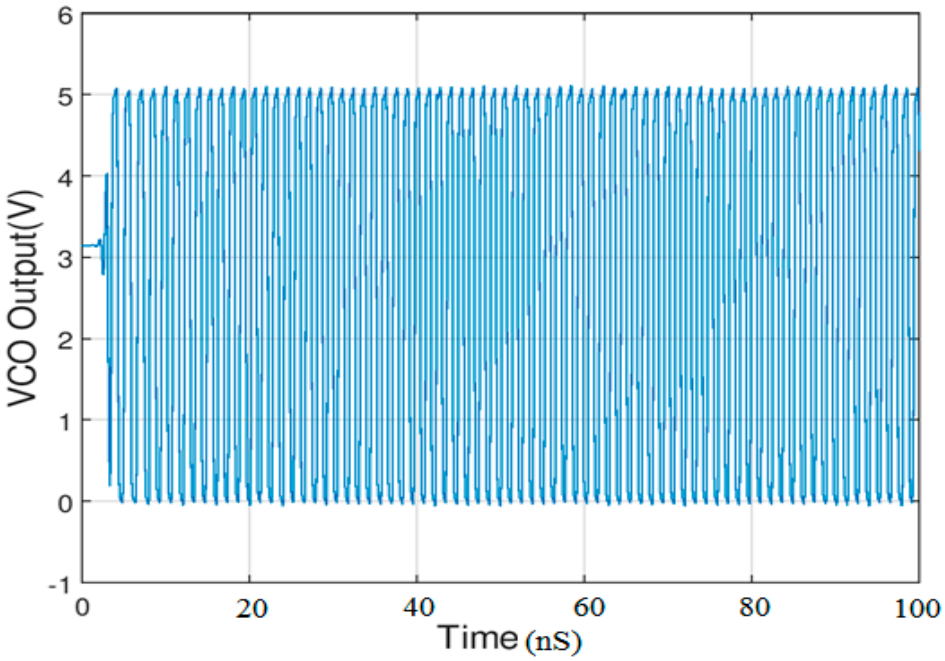


Figure 13. SPICE simulation output of a single-ended current starved VCO.

Figure 14 shows the plot of transfer characteristics of the VCO. It shows that the VCO is a linear system because the frequency of oscillator varies linearly with the control voltage, V_{ctrl} This is consistent with the existing PLL design [26,27]. Additionally, it is desirable for the voltage (V) – frequency (F)

characteristic to have a positive slope, as shown in Figure 14. This means that the maximum operating frequency is achieved at maximum control voltage [28]. The tuning range of the VCO is 741–994 MHz. The result shows that the VCO in our design has a wider tuning range when compared and validated with the work described in [26].

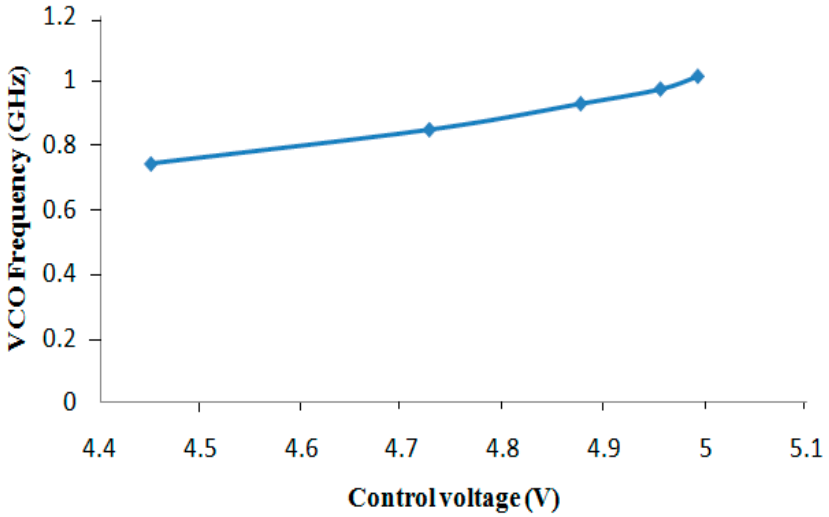


Figure 14. VCO transfer characteristics.

The measurement of the VCO tuning sensitivity (K_{VCO}) was calculated from the simulation results in Table 1 using Equation (5) and is summarized in Table 2.

Table 1. Voltage/frequency captured data.

Control Voltage (V)	VCO Frequency (GHz)
4.450	0.741
4.726	0.846
4.876	0.926
4.955	0.971
4.992	1.010

Table 2. Tuning sensitivity calculated data.

Control Voltage (V)	K_{VCO} (GHz/V)
4.450	0.594
4.726	0.550
4.876	0.592
4.955	0.908
4.992	1.022

Substrates of P-channel MOS and N-channel MOS transistors are connected to supply voltage, V_{DD} and the ground, respectively.

Table 1 shows the variations in frequency of the VCO as the control voltage increases.

$$K_{\mathrm{VCO}} = \frac{\Delta \mathrm{F}}{\Delta \mathrm{V}} \tag{5}$$

where F and V denote the VCO frequency and control voltage, respectively.

Figure 15 shows a sensitivity plot of the voltage-controlled oscillator. The gain of the VCO falls as control voltage increases. However, the gain increases linearly with the control voltage as we approach the tuning frequencies.

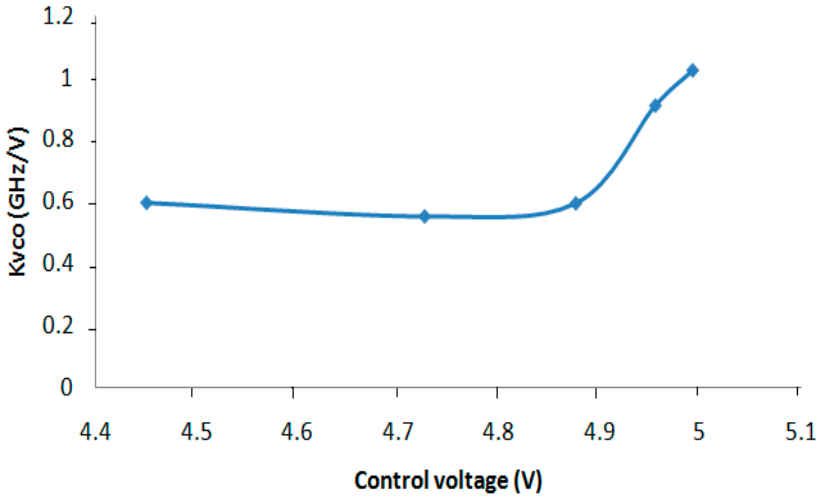


Figure 15. VCO tuning sensitivity curve.

Since the objective of the field of electronics or VLSI design is ultimately to ensure that electronics are reliable, it is worth thinking about the relationship between temperature and reliability. Thermal analysis is important in ensuring the accuracy of timing, noise, and reliability analyses during chip design [29]. In commercial, industrial and military applications, the general temperature specifications of most integrated circuits ranges from −55 °C to 125 °C. This is because the majority of integrated circuit failure mechanisms occur at these temperatures [30]. The loop filter resistor contributes to phase noise, which can affect the performance of the PLL. Since the control voltage, V_{ctrl}, is fixed over wide range of temperatures, the simulation result in Figure 16 shows that our design is less temperature dependent and thus highly reliable.

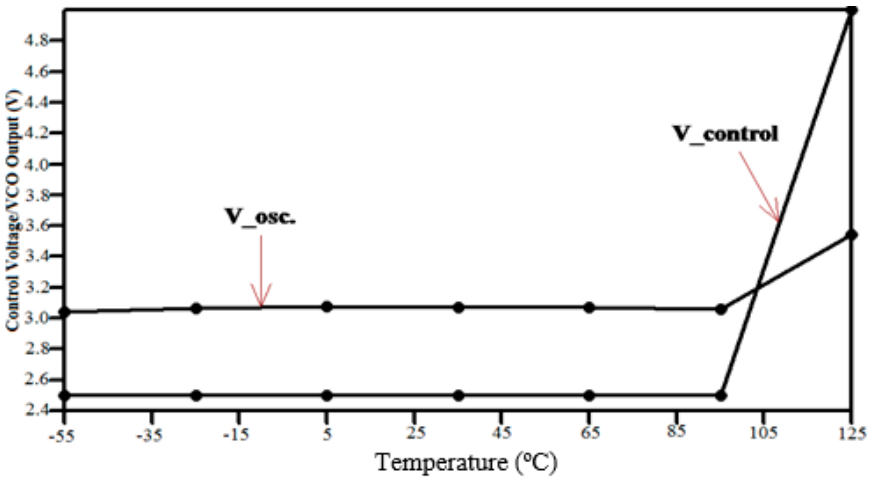


Figure 16. Simulation result of thermal analyses.

3.4. Frequency Divider

A divider circuit divides the frequency of the VCO clock to generate a feedback clock for a phase comparison with reference input [24]. In this work, we employed a fractional N-divider D flip-flop circuitry, which divides the VCO clock by the highest power of two factor to synchronize the reference clock signal and the divider output clock.

The stable output frequency of the VCO is given as:

$$f_{out} = N * f_{ref} \tag{6}$$

where N is the mod counter.

4. Results and Discussion

Our proposed memristor-based loop filter PLL has a tuning range of 741–994 MHz. Figures 14 and 16 show that the target is achieved where there is a phase match between the PLL reference input, V_b, and feedback input from divider circuitry, V_{div} as shown in Figure 17.

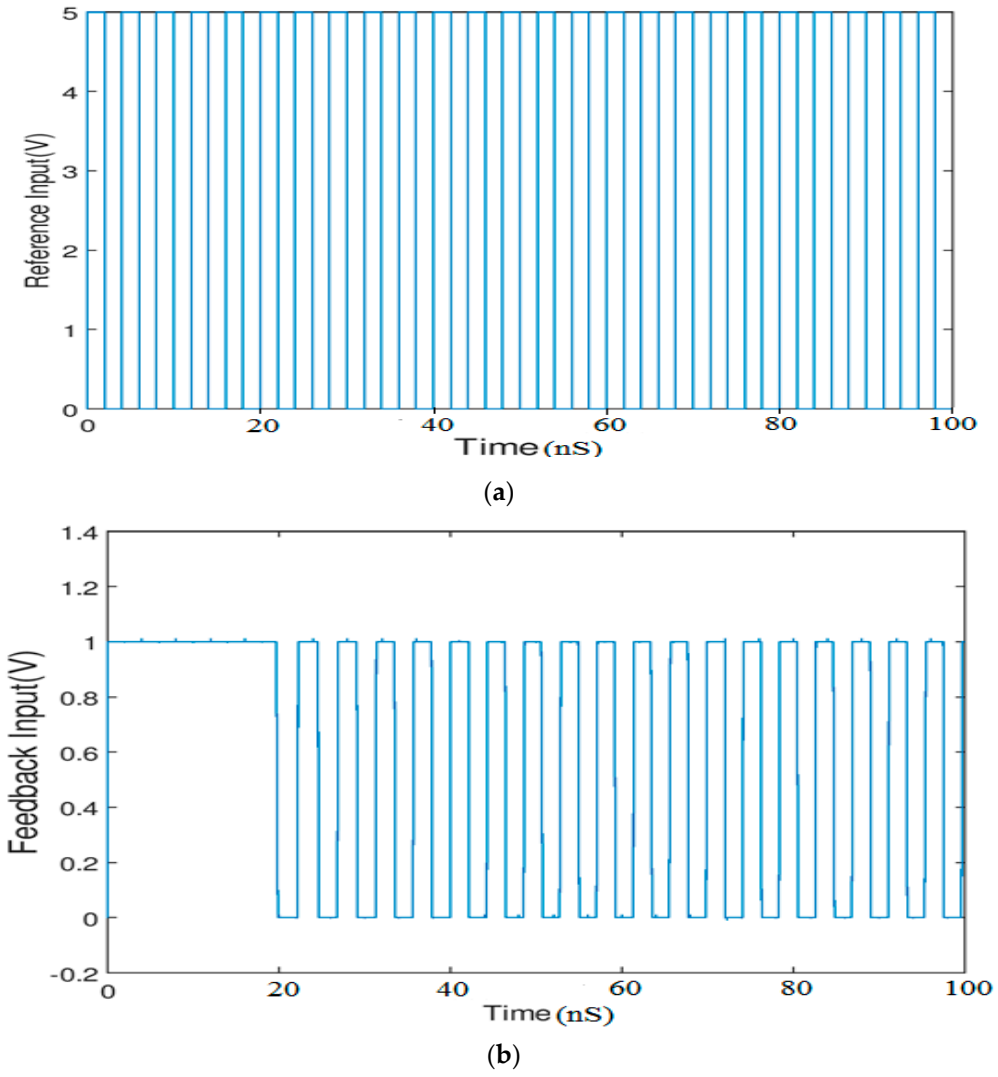


Figure 17. SPICE simulation: (**a**) Reference input; (**b**) feedback input.

We also computed the average power and energy consumption of the memristor, as shown in Figure 18. The values obtained satisfy the conditions of an energy efficient device [31]. Though we employed the memristor only in the loop filter, the memristor is also compatible with CMOS crossbar architecture, so it can be integrated into other components of the PLL in the future work.

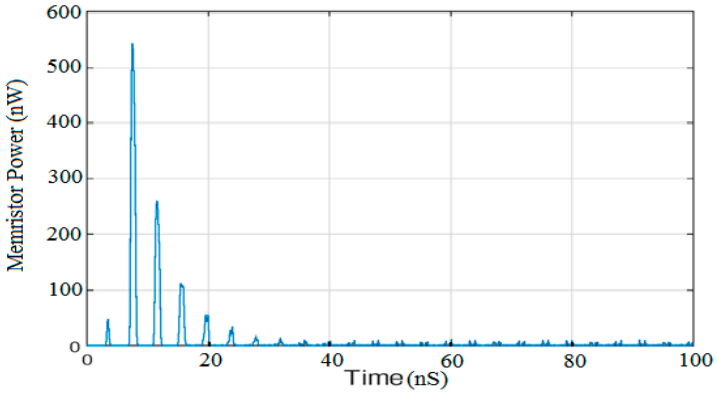


Figure 18. Power consumption of the memristor.

From Figure 18, the average power consumed by the memristor is 8.65 nW, as compared to 8.637 μW, which is the total estimated power consumed by the proposed loop filter. The power consumption of the memristor device is very small, so its impact on the total power consumption in the phase locked loop design is negligible.

5. Conclusions

The advantages of combining memristors and CMOS transistors for the design of a phase locked loop are highlighted in this paper. The use of a nanoscale size memristive device in loop filter design is explored to reduce power consumption and save area. The proposed PLL achieves a tuning range from 741 MHz to 994 MHz with less variations with temperature. As a future work, the fabricated area of the proposed loop filter can be effectively reduced further by replacing the conventional capacitances with nanoscale memcapacitance circuits.

Author Contributions: Research problem was suggested to N.O.A. (PhD student and first author) by A.S. N.O.A. worked on the suggested research problem under the supervision of S.A., prepared first working draft of the work in JLPEA format. Extensive corrections and revisions were made by S.A. including at the final correction of proof. Both authors contributed equally.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

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