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A 0.5 V 68 nW ECG Monitoring Analog Front-End for Arrhythmia Diagnosis

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Abstract: This paper presents a power efficient analog front-end (AFE) for electrocardiogram (ECG) signal monitoring and arrhythmia diagnosis. The AFE uses low-noise and low-power circuit design methodologies and aggressive voltage scaling to satisfy both the low power consumption and low input-referred noise requirements of ECG signal acquisition systems. The AFE was realized with a three-stage fully differential AC-coupled amplifier, and it provides bio-signal acquisition with programmable gain and bandwidth. The AFE was implemented in a 130 nm CMOS process, and it has a measured tunable mid-band gain from 31 to 52 dB with tunable low-pass and high-pass corner frequencies. Under only 0.5 V supply voltage, it consumes 68 nW of power with an input-referred noise of 2.8 μVrms and a power efficiency factor (PEF) of 3.9, which makes it very suitable for energy-harvesting applications. The low-noise 68nW AFE was also integrated on a self-powered physiological monitoring System on Chip (SoC) that is used to capture ECG bio-signals. Heart rate extraction (R-R) detection algorithms were implemented and utilized to analyze the ECG data received by the AFE, showing the feasibility of <100 nW AFE for continuous ECG monitoring applications.

Keywords: analog front end (AFE); electrocardiogram (ECG); IoT; sub-threshold operation; ultralow power

1. Introduction

In recent years, there has been a growing demand for ultralow power (ULP) energy-harvesting body sensor nodes for continuous and low-cost monitoring of patient bio -signal data for diagnosis and prevention of various illnesses, such as heart arrhythmia [1–4]. One of the most important challenges for many of these sensors is the operating lifetime. These sensors often operate in energy-constrained environments where there is a need to harvest energy by different methods, such as photovoltaic cells or thermoelectric generators (TEGs). Additionally, these systems need to operate from very low supply voltages. For example, a 1 cm^3 TEG energy harvester attached to a running person delivers only 2.2 μW of power, and the voltage available at the output of TEG energy harvesters is often only tens of millivolts [5]. Therefore, low-voltage operation of battery-less signal acquisition sensors highly relaxes the voltage boost conversion requirement for generating a usable supply voltage.

Due to the continuous bio-signal monitoring of these sensor nodes, the power consumption of signal acquisition analog front-ends (AFEs) plays an important role in the overall power consumption of the sensors. Recent advancements in state-of-the-art self-powered systems, such as [2], have demonstrated sub-μW operation for these systems. This highlights the requirement for <100 nW AFEs. However, targeting low absolute power often results in poor noise performance. One of the

important requirements of ECG signal acquisition systems is the capability to detect very small input signals on the order of 100 µV to 4 mV at near-DC frequencies, where flicker noise is dominant. Therefore, low noise operation of the AFE is one of the primary specifications of an ECG front-end, and signal acquisition systems often compromise the power consumption of the system to achieve lower input-referred noise specifications or vice versa.

In this work, we present an ultralow power low-noise AFE that meets the requirements of ULP energy-harvesting physiological sensors. By utilizing a weak inversion biasing technique, and with a power consumption of only 68 nW, the AFE realizes a very low flicker noise corner frequency and achieves an input-referred noise of 2.8 μV_{rms}. The AFE operates from a low power supply of 0.5 V, which relaxes the voltage boost requirements of energy-harvesting systems. Fully differential topology is utilized to ensure a high common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR). The AFE in this work attains a noise efficiency factor of 2.78, corresponding to a power efficiency factor [6] (PEF, also known as NEF^2xV_{DD}) of 3.9. The AFE achieves an input-referred noise of <10 μV_{rms} with a <100 nW power consumption, which demonstrates a very good balance for the noise–power trade-off, compared to state-of-the-art amplifiers. Figure 1 presents a comparison of power consumption versus root mean square (RMS) input-referred noise per square root of bandwidth for the recent state-of-the-art signal acquisition systems [6–18]. The proposed AFE has the lowest input-referred noise per square root of bandwidth compared to the state-of-the-art AFEs with power consumptions below 100 nW. Constant PEF contours are shown on the figure, highlighting the low-power and low-noise trade-off for designs of amplifiers with similar PEF. PEF is used here to account for noise, current, and required voltage headroom of amplifiers.

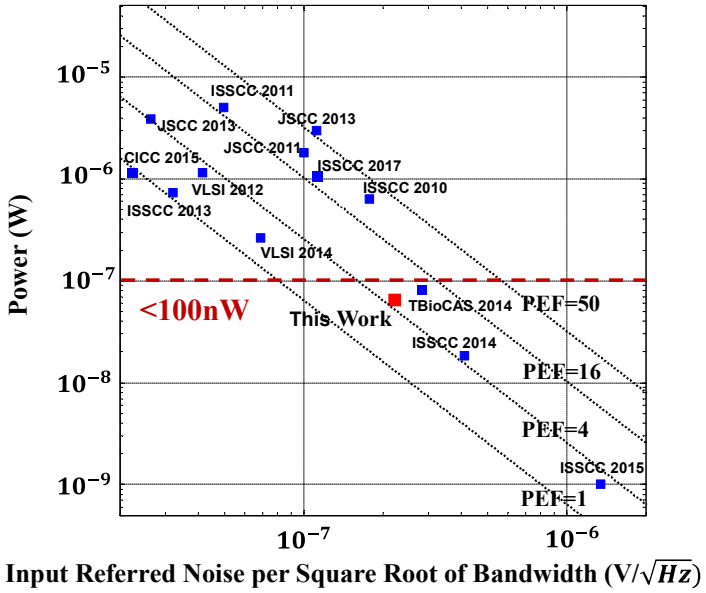


Figure 1. Power efficiency comparison between this work and other state-of-the-art works in power efficiency factor (PEF) (NEF^2xV_{DD}) contours. [6–18].

The presented AFE was also integrated in a self-powered physiological monitoring System on Chip (SoC) [2]. The performance of the AFE was validated in a real-world test scenario, by capturing and processing ECG bio-signals from human subjects. The AFE output signals were digitized on the SoC using an integrated successive approximation (SAR) analog-to-digital (ADC), and they were used to successfully perform ECG heart rate (R-R) extraction.

The outline of the paper is as follows. We introduce the AFE architecture in Section 2, focusing on the three-stage AFE integration and features of circuit building blocks. In Section 3, we discuss the state-of-the art low-noise biopotential amplifiers and present the low-noise amplifier design in

this work. The design considerations for a low-noise low-power design of the AFE are discussed here. Section 4 presents the designs of the low-pass filter and variable gain amplifier. Finally, the measurement results for the AFE chip are discussed in Section 5 and the AFE integration on the SoC and real-world test scenarios for arrhythmia detection are presented, and we conclude in Section 6.

2. AFE Architecture

To meet the low-power and low-noise performance requirements of battery-less signal acquisition sensors, and the specifications for the ECG signal detection, the AC-coupled ultralow-power analog front-end was employed as shown in Figure 2. Achieving minimum input-referred noise performance and high power efficiency at low current levels is a major challenge. This is enabled by several considerations in the architecture and component level design of the AFE. The fully differential non-chopping capacitive feedback architecture was chosen in order to transfer the high dynamic range and hence gain requirements of the AFE to the lower ECG band frequencies, as opposed to chopper amplifiers where the amplification is done at higher chopping frequencies. The low supply voltage and efficient weak inversion biasing approach in the design of the AFE's building blocks enables low-power and high-gain realization of the AFE. Transistor-level low-noise design considerations were implemented in the design of the AFE to enable a low-noise performance. In this work, we present a fully integrated AFE, which realizes a low-noise performance, as well as an ultralow-power consumption, and ensures enough circuit reliability, bandwidth, and precision to enable practical ECG monitoring applications. The AFE consists of three stages and includes a low-noise instrumentation amplifier (LNA), a tunable bandwidth low-pass filter (LPF), and a variable gain amplifier (VGA). A self-biased current reference generator provides bias currents to the building blocks of the AFE, and a digital control scan chain block sets the gain and bandwidth of the AFE by programming the integrated voltage digital-to-analog converters (DACs).

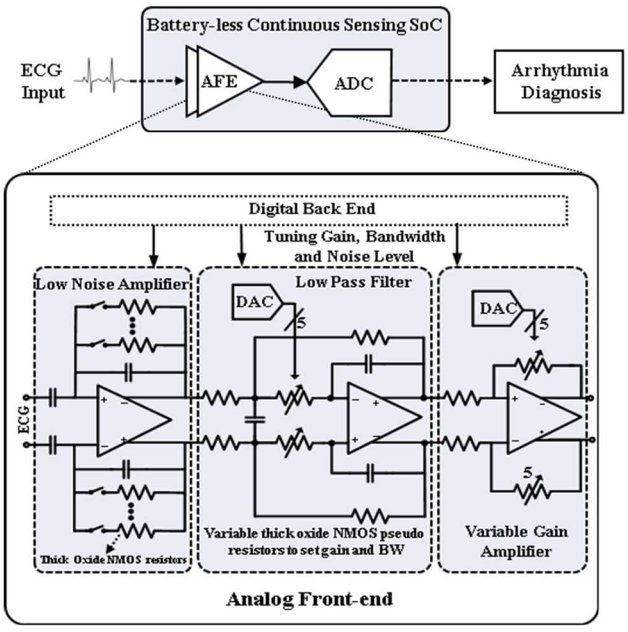


Figure 2. Block diagram of the analog front-end (AFE).

The differential input bio-signals are capacitively coupled to the input LNA to reject DC offsets introduced at the electrode tissue interface. The LNA provides a mid-band gain of 30 dB, and therefore alleviates the following stages input-referred noise requirements. The high-pass corner frequency of the AFE is set by the feedback resistors and capacitors in the LNA. The LNA is followed by a tunable

low-pass filter, which controls the low-pass corner frequency of the AFE and provides a tunable bandwidth of 40–250 Hz. This corner frequency was chosen in order to capture the usable spectral content in a typical ECG signal. The LPF is loaded by the VGA, which has a programmable gain with a 21 dB range. As a result, the total gain of the front-end can be adjusted from 31 to 52 dB based on the input data. Extensive digital tuning, controlled with the digital back-end on the chip, is implemented to account for the sensitivity of pseudo-resistors to process variations.

As for the power distribution among the three stages of the AFE, the LNA consumes 27 nW, which is the most power consumption among all the blocks to enable a low-noise performance. The following stages have much less contribution to the overall noise performance, therefore, the filter has a much lower power consumption at 5 nW. Finally, the third stage, VGA, has a negligible noise contribution but drives larger capacitive loads due to the integration with the ADC; therefore, its power consumption lies between those of the LNA and LPF and is 20 nW.

3. Low-Noise Amplifier Design

3.1. State-of-the-Art Biopotential Low-Noise Amplifiers

Reducing the amplifier power consumption while keeping the noise level the same is crucial for a wide range of energy constraint applications. The input-referred noise of the overall AFE is dominated by the noise performance of the first stage of the amplifier. Therefore, the current consumption in LNAs is often set for an optimized noise–power trade-off. Many outstanding research works have been carried out to address the power–noise tradeoff of AFEs [6–18]. One main idea in these designs is to increase the transconductance (g_m) of amplifiers by keeping the bias current constant. The AFE designs in prior work include inverter-based LNAs, where the amplifier g_m is increased by using stacked PMOS and NMOS pairs [18]. Another design approach is current-reuse through stacking amplifiers to further boost g_m of the overall amplifier [19]. The AFE in [18] achieves a very good noise efficiency factor (NEF) by using a single-stage current-reused differential amplifier topology. However, it requires a high supply voltage due to the cascode configuration and is not suitable for low-voltage ULP energy-harvesting sensors. Additionally, the orthogonal current-reuse amplifier in [19] achieves a high level of current-reuse by using N-time current-reuse between N-channel inputs. The 2N number of outputs are then combined, which results in an increased power consumption due to the additional peripheral circuits, which is not desirable.

In addition to the above techniques, the chopping method has been widely employed to enhance the noise performance of amplifiers [7,8]. Although chopping significantly reduces the flicker noise contribution of amplifiers, it requires amplifiers with larger bandwidths and chopping clock generation circuits that can increase the overall power consumption of the amplifier. In chopper amplifiers, the bio-signals are up-converted to a higher frequency and the amplification is done at high frequencies, therefore, the power consumption performance of the amplifier is not optimized. Additionally, this technique reduces the DC input impedance of the sensing front-ends [9], and the low input impedance can generate harmful offset currents.

In this work, we were able to lower the flicker noise corner frequency of the AFE below 100 Hz by keeping the power consumption less than 100 nW. This is enabled by using weak inversion biasing and low-noise design techniques, without the necessity of using chopping modulators. This allows the amplifier to operate at lower frequencies compared to chopper amplifiers. The frequency domain behavior of the voltages in chopper amplifiers and in the non-chopper approach is presented in Figure 3.

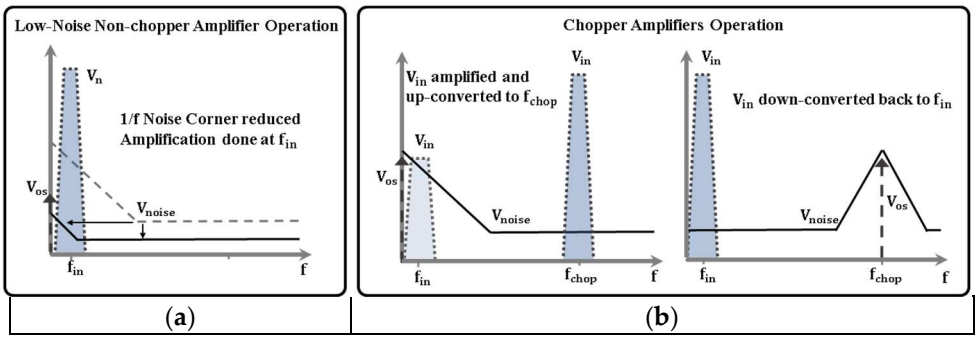


Figure 3. Frequency domain representation of voltages (input signal V_{in}, noise voltage V_{noise} and offset voltage V_{os}) in (**a**) the proposed low-noise amplifier; (**b**) chopper amplifiers.

3.2. Low-Power Low-Noise Amplifier

3.2.1. Capacitively Feedback Amplifier

The LNA block diagram is shown in Figure 4a. It uses capacitive feedback topology, a popular topology in biomedical recording amplifiers [20], and uses capacitors to set the mid-band gain and to reject DC offset from the input signals. A fully differential architecture is used to achieve a high PSRR and CMRR. The ratio of the capacitors C_f and C_{in} sets the gain of the LNA amplifier. The lower cutoff frequency of the amplifier is set by $1/\left(2\pi R_f C_f\right)$, where R_f resistors are implemented by pseudo-resistors. Pseudo-resistors can realize resistances larger than 10^{12} Ω by occupying a small area. We have used thick oxide PMOS devices to implement the pseudo-resistors due their better noise performance. The tunable lower cutoff frequency of the amplifier is adjusted by selecting the pseudo-resistors in the feedback path of the LNA with 4b resolution.

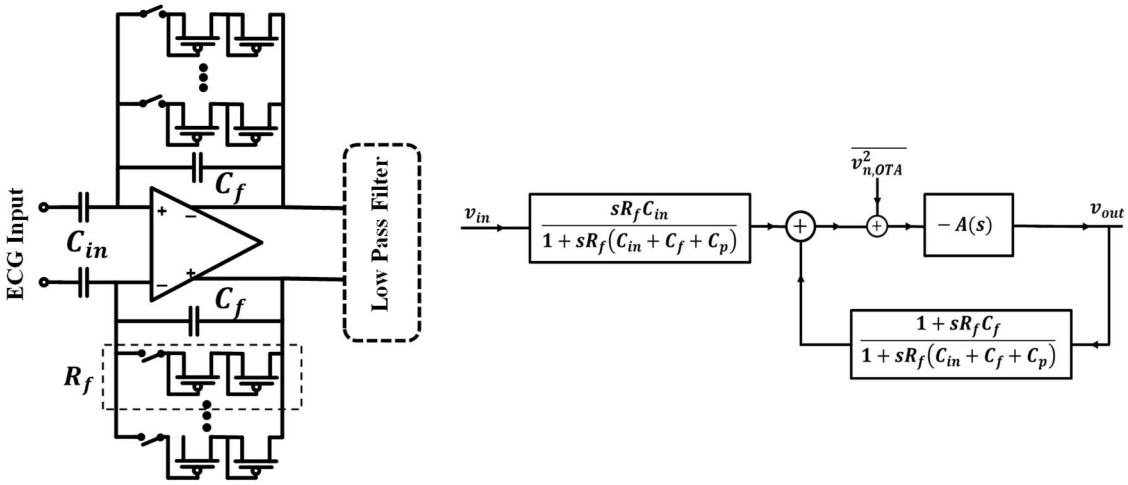


Figure 4. (**a**) Circuit diagram of the low-noise instrumentation amplifier (LNA); (**b**) block diagram representing the operation of the feedback amplifier.

The input-referred noise of the overall amplifier can be estimated using the capacitive feedback circuit diagram of the LNA shown in Figure 4a. From the nodal analysis, the operation of the feedback amplifier can be described by the feedback block diagram of Figure 4b, where $v_{n,OTA}^2$ represents the input-referred noise per unit bandwidth of the operational transconductance amplifier (OTA), and C_p

represents the parasitic capacitance at the input of the amplifier. According to the block diagram of Figure 4b, the overall input-referred noise of the LNA can be expressed as

$$\overline{v_{n,LNA}^2} = \left(\frac{1 + sr_f\left(C_{in} + C_f + C_p\right)}{sr_f C_{in}}\right)^2 . \overline{v_{n,OTA}^2} \quad (1)$$

3.2.2. Design of the OTA

Due to the low supply voltage, cascode and current-reuse topologies for the amplifiers are impractical. Therefore, all three main blocks in the design are implemented by two stage differential common source amplifiers with PMOS input devices for the best noise and power efficiencies. The circuit implementation is illustrated in Figure 5a. Currents and dimensions in the amplifiers are optimized for the input-referred noise, gain, power, and loading conditions in each stage of the AFE. The device dimensions for the main transistors in the OTA for the LNA are shown in Figure 5a.

According to Equation (1), in order to achieve a low-noise performance, the input-referred noise of the OTA, $\overline{v_{n,OTA}^2}$, needs to be minimized. It is well known that to ensure a low input-referred noise, as well as a low power consumption, the G_m of the first stage amplifier in the LNA has to be maximized. Therefore, the currents in the first stage differential pair are set at a higher value than the second stage to meet the noise requirements. The input-referred noise of the OTA can be approximated by the input-referred noise of the first transconductance stage, which is dominated by the noise contributions from the differential PMOS (M_1 and M_2) input pair and the NMOS (M_3 and M_4) load devices. Using the transistor's small signal parameters, the input-referred thermal noise of the OTA can be approximated as

$$\overline{V_{n,OTA,th}^2} = \frac{1}{{g_{m1}}^2}\left(\frac{4kTg_{m1}}{\kappa} + 8kT\gamma g_{m3}\right) \quad (2)$$

where k is the Boltzmann's constant, T is the absolute temperature in kelvin, γ is the noise excess factor of transistors in strong inversion, and κ is the reciprocal of the sub-threshold slope factor n_p.

The input-referred flicker noise can be calculated as:

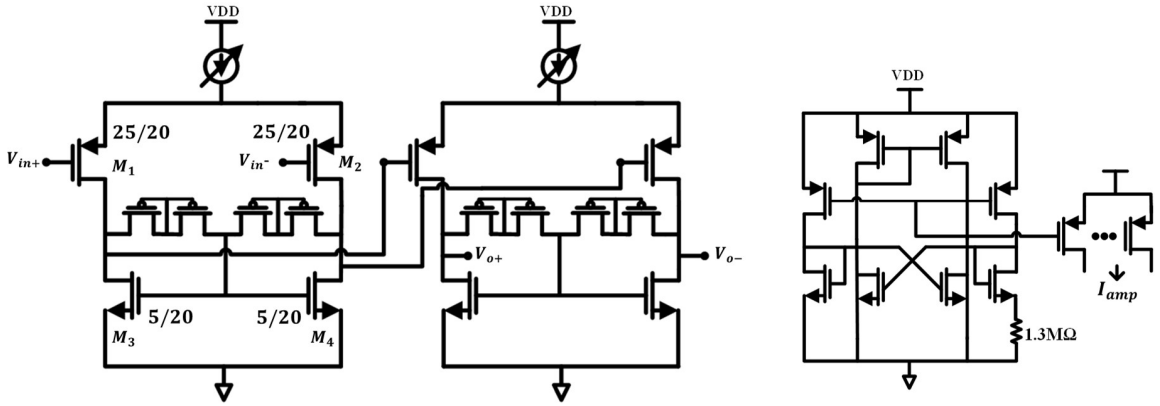


Figure 5. (**a**) Circuit implementation of the operational transconductance amplifier (OTA); (**b**) circuit implementation of the constant g_m current biasing circuit.

$$\overline{V_{n,OTA,1/f}^2} = \frac{1}{C_{ox}}\left(\frac{K_n}{(WL)_1} + \frac{K_p\ {g_{m3}}^2}{(WL)_3{g_{m1}}^2}\right) \quad (3)$$

where C_{ox} is the gate dielectric capacitance, and K_n and K_p are process-dependent values that represent the PMOS and NMOS flicker noise constants.

In order to minimize the input-referred thermal noise and to achieve maximum g_m, transistors M_1 and M_2 are biased in the sub-threshold region with low bias currents. A constant g_m current reference with voltage regulation is used as the current reference generator, providing the bias current for the amplifiers (Figure 5b). In the sub-threshold region, g_m of the transistors is independent of the device width and is proportional to the driving current. Therefore, for a given current level, it is advantageous to operate the input transistors M_1 and M_2 in the sub-threshold region to achieve a high g_m efficiency.

According to [21], PMOS and NMOS devices have a lower noise contribution in the weak inversion region for low frequencies (1 mHz to 100 Hz) compared to strong inversion. However, Equation (2) suggests strong inversion biasing for a low thermal noise contribution for NMOS load devices in the OTA. For an optimized noise performance, in order to minimize the flicker noise contribution of the NMOS devices in low frequencies, as well as to satisfy the low thermal noise requirement suggested by Equation (2), these transistors are biased in the near-threshold region.

In order to further reduce the flicker noise and to lower the noise corner frequency, the input devices are implemented with large gate area PMOS transistors ($M_{1,2}$). In addition, long NMOS devices M_3 and M_4 (L = 20 μm) are employed as the load in the differential pair to achieve a lower $g_{m3,4}$ (transconductance of M_3 and M_4) value and hence further improve the flicker noise and thermal noise performance. Equation (1) highlights the importance of the parasitic capacitance at the differential input of the OTA. While using large transistors at the differential input of the OTA reduces the flicker noise corner frequency, it can degrade the overall input-referred noise of the amplifier. Therefore, in this design, a proper sizing for the transistors was implemented to address this trade-off.

The design considerations mentioned above and the biasing technique approach allow us to considerably lower the noise corner frequency, as well as reduce the thermal noise level, and to implement a low-power low input-referred noise instrumentation amplifier at the ECG signal frequency level.

4. Low-Pass Filter and VGA Design

The tunable bandwidth low-pass filter controls the upper corner frequency of the AFE and adjusts the input voltage swing at the input of the VGA to prevent any distortion or clipping of the AFE's output signal. A multiple feedback topology is employed for the differential second-order LPF, which offers an increased dynamic range in the output, as shown in Figure 6. The gain of the filter is set by the ratio of the pseudo-resistors R_1 and R_3, and the upper cutoff frequency is tuned by the variable pseudo-resistors R_2 with fixed capacitors C_1 and C_2. The employed architecture has the advantage of having separate controls over bandwidth and gain. A 5b voltage mode resistive DAC is used to program the cutoff frequency of the LPF. The use of variable pseudo-resistors for gain and bandwidth tuning, instead of capacitor arrays, has the advantage of minimizing the area, which is one of the key factors in energy-harvesting signal acquisition devices.

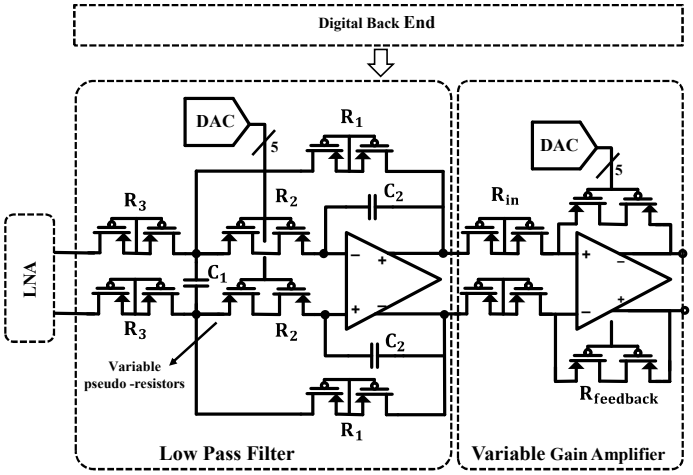


Figure 6. Circuit implementation of the low-pass filter (LPF) and variable gain amplifier (VGA).

As the last stage of the amplifier, the VGA provides sufficient gain for the maximum voltage swing. Similar to the LPF, the gain of the VGA is defined by the ratio of resistors $R_{feedback}$ and R_{in} and is tuned by varying the value of the pseudo-resistors in the feedback path by adjusting the control voltage values applied to the gate of the transistors. The variable pseudo-resistors are controlled by a 5b voltage DAC that is programmed by the digital back-end. The circuit implementation of the VGA is shown in Figure 6.

5. Experimental Results

5.1. AFE Performance Measurements

The prototype was fabricated in a 130 nm CMOS process, and the AFE core blocks, not including the I/O pads, occupy an area of 0.24 mm^2. Figure 7 shows the die micrograph of the AFE chip.

The LNA–VGA chain consumes 53 nW of power and delivers a variable gain of 31–52 dB. The measured gain and bandwidth of the AFE are presented in Figure 8. All the measurements were done at room temperature with a measured ±2 dB gain variation in the 0–40 °C range. The AFE offers a digitally tunable bandwidth control, where the lower corner frequency is set by the LNA and varies from 0.5 to 5 Hz. The upper corner frequency is adjusted to meet the ECG signal monitoring requirements. Most of the diagnostic information in ECG signals is contained below 100 Hz [22], and the AFE is designed to satisfy this requirement with a tunable bandwidth up to 155 Hz at the maximum gain. For applications with higher frequency contents, such as ECG signals for infants, the bandwidth can further be increased by sacrificing the gain of the VGA stage with a constant gain–bandwidth product. For example, for a tunable bandwidth of up to 250 Hz, the AFE can provide a gain of 39 dB.

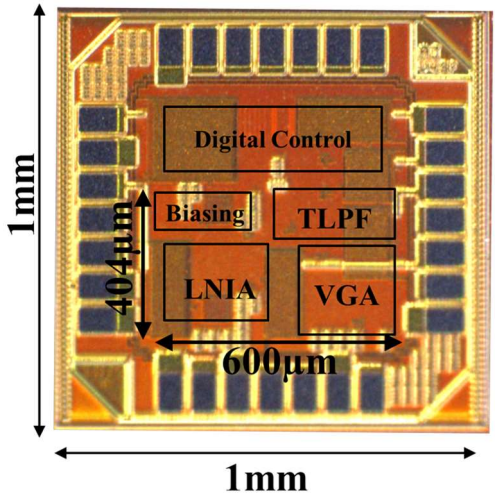
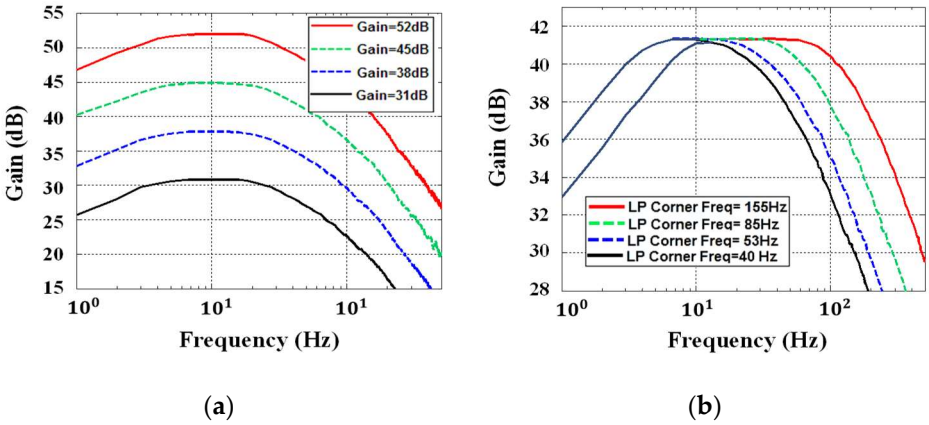


Figure 7. Chip die micrograph.



(**a**) (**b**)

Figure 8. Measured frequency response of the AFE. (**a**) gain tuning, (**b**) bandwidth tuning.

Figure 9 shows the measured input-referred noise density of the amplifier. The measurements show a good matching to the expected performance, confirming the power-efficient low-noise design techniques of the AFE. The AFE has a measured RMS input-referred noise of 2.8 µV over a 155 Hz bandwidth and has an input-referred noise density of 200nV/$\sqrt{}$Hz at 155 Hz. The circuit exhibits a noise efficiency factor (NEF) of 2.78, which is well in range with other state-of-the-art AFEs. This work realized a PEF (NEF^2xV_{DD}) of 3.9, while maintaining a balanced power consumption–input-referred noise trade-off. As shown in Figure 1, the proposed AFE has the lowest input-referred noise per square root of bandwidth compared to the sub-100nW state-of-the-art AFEs. The measured CMRR and PSRR exceed 60 dB and 70 dB over the bandwidth of the AFE. Total harmonic distortion (THD) is measured in the low-gain setting of the AFE. The THD stays below 1% for inputs less than 2.5 mV peak–peak. Table 1 summarizes the measured performance of the AFE and presents a comparison between this work and the state-of-the-art AFEs [6–8,10,18].

Table 1. Performance summary and comparison with the state-of-the-art biopotential AFEs.

	This Work	[6]	[7]	[8]	[10]	[18]
Technology (nm)	130	65	180	180	130	350
V_{DD} (V)	0.5	0.5	1	1.8	1.2	2.5
Area (mm^2)	0.24	0.013	0.25	-	0.4	0.17
Blocks in comparison	AFE	AFE, ADC	AFE	AFE	AFE	AFE
Power (nW)	68	5040	266	8250 *	5300	82.5
Gain (dB)	31–52	32	42–51	52–80	45–71	40.7
HP corner Freq. (Hz)	0.5	1	1	0.07	1	0.05
LP corner Freq. (Hz)	40–250	300–10,000	500	30–100	100	100
Input Referred Noise (μV_{rm})	2.8 [1.5–155 Hz]	4.9 [300 Hz–10 kHz]	1.54 [1–500 Hz]	0.91 [0.5–100 Hz]	0.45 [1–100 Hz]	2.8 [0.05–100 Hz]
Input Impedance (MΩ)	115	N/A	N/A	>500	>100	N/A
NEF	2.78	5.99	1.38	5.12	3.7	1.96
PEF	3.9	17.96	1.9	47*	16.4	9.6
CMRR (dB)	62	75	89	>90	>95	>70

* This value is calculated based on the reported performance.

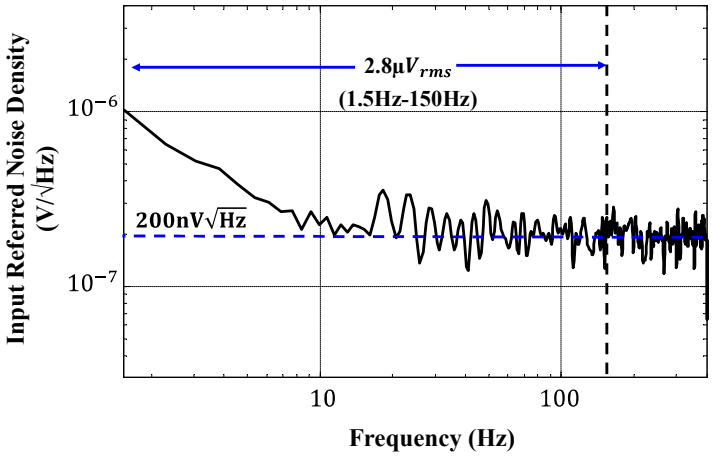


Figure 9. Measurement input-referred noise density of the analog front-end.

5.2. Arrhythmia Diagnosis

The AFE is also integrated on an energy-harvesting continuous monitoring SoC [2], and the SoC is used to perform human ECG signal acquisition in a real-world scenario. In the SoC, the AFE is directly coupled to an integrated single-ended 12-bit SAR ADC. When enabled, the ADC uses the clock generated on the SoC to provide 12-bit parallel output every 16 clock cycles. The combined power consumption of the integrated AFE and ADC is 301 nW at 0.5 V. The input impedance of the AFE is measured at 115 MΩ, which is sufficient for our measurements of ECG signal acquisition. In this measurement setup, we have used the commercial, 3M 2560 Red Dot, electrodes to successfully capture ECG data from a human subject. The performance of the AFE with dry electrodes, where the input impedance imbalance from electrodes can cause large DC drifts, has not been evaluated.

The digitized ECG signals were processed and analyzed off-chip using heart rate extraction algorithms. The R-R extraction algorithm is based on the popular Pan–Tomkins algorithm [23]. The algorithm uses an initial 4 s time frame to estimate the DC baseline value for the ECG waveform, and through thresholding and time windowing, extracts the ECG R-peaks. Desired accuracy can be achieved by adjusting the sampling rate in the algorithm. Figure 10 shows the measured R-R interval for the ECG signal calculated by the R-R extraction algorithm, with a sampling rate of 200 Hz. The annotated numbers represent the number of samples between consecutive peaks.

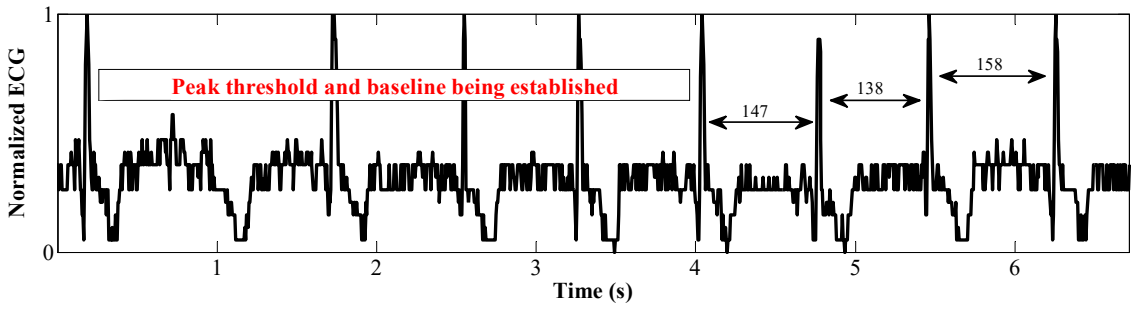


Figure 10. Measured electrocardiogram (ECG) results for an R-R extraction algorithm. The measured results are for the acquired ECG data through the AFE integrated on the System on Chip (SoC).

6. Conclusions

An ultralow power ECG AFE with a balanced noise and power performance is presented in this paper. The AFE provides bio-signal monitoring with programmable gain and bandwidth, amplifying ECG signals as low as a few microvolts while consuming <100 nW. To realize a high-noise and -power efficiency, a weak inversion biasing technique was used together with other low-noise design techniques. The proposed AFE has a power consumption of only 68 nW operating at 0.5 V supply voltage. The AFE provides a variable gain of 31–52 dB with NEF and PEF of 2.78 and 3.9, respectively. It was fabricated in a 130 nm CMOS technology and occupies an area of 0.24 mm^2. Arrhythmia diagnosis algorithms were implemented and the feasibility of the AFE performance for energy-harvesting applications was validated by integrating it on a battery-less SoC and successfully performing human ECG signal acquisition with an R-R extraction algorithm.

Author Contributions: In this research work, author A.K. contributed to the literature search, design of the AFE, power-noise analysis, and the measurements for the AFE standalone chip. She was also responsible for writing the paper. Author J.B. was responsible for implementing the arrhythmia algorithms and performing the measurements associated with the ECG data acquisition on the SoC. Author N.L. contributed to the design of the ADC and integration of the AFE block with the ADC on the SoC. Author B.H.C. and Author D.D.W. guided the first three authors in the research, implementation and documentation of this work.

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