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A Performance of the Soft-Charging Operation in Series of Step-Up Power Switched-Capacitor Converters

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Abstract: Due to their high power density and appropriateness for small circuits integration, switched-capacitor (SC) converters have gotten more interests. Applying the soft-charging technique effectively eliminates the current transient that results in a higher power density and a higher fundamental efficiency. Achieving the complete soft-charging operation is impossible by using the conventional control diagram for any SC converter topology. In this paper, we proposed a split-phase control to achieve the complete soft-charging operation in a power switched-capacitor (PSC) converter. The proposed control diagram was designed for a 1-to-4 PSC converter (two-level of the PSC converter). The implemented split-phase diagram successfully controls eight switches to exhibit eight modes of operation. In addition to the current transient elimination, the complete soft-charging allows us to reduce capacitor sizes. However, reducing capacitor size negatively increases the output voltage ripple; hence, an output LC filter is needed. The complete soft-charging achievement accomplishes a 96% efficiency due to the lower output impedance and the dead time switching. LT-Spice software has been used to verify the proposed control and the results were compared with hard-charging and incomplete soft-charging operations.

Keywords: the PSC converter; the complete soft-charging; switched-capacitors converters; LT spice

1. Introduction

DC-to-DC converters are commonly designed with magnetic elements for energy storing purposes. Designing a DC-to-DC converter with magnetic components such as an inductor leads to low power density due to the inductor bulky size. An increase in the power density of DC-to-DC converters requires a higher switching frequency (f_{sw}) since the inductor size is inversely proportionate to the switching frequency. Increasing the f_{sw} can solve the problem partially; however, it will cause a switching loss produced by semiconductor elements. A growth in switching loss is conversely proportional to the converter efficiency [1,2]. High power density and high efficiency are two significant requirements for designing a DC-to-DC converter functional for tiny electronic circuit integration.

To satisfy these desires, the DC-to-DC switched-capacitors (SC) converters are widespread for on-chip integration. Because the DC-to-DC SC converters contain only capacitors and switches, they have a high-power density. Charging and discharging the capacitors allow the electric charge to flow from the input to the output to accomplish voltage regulation by alternating the switches states. In addition to the high-power density, the SC converters tend to maintain the efficiency at a high voltage gain. Because of their numerous topologies, analysis of the SC converters has been considered a challenging task. The SC analysis has been generalized in [3]. Two operation states occur in most types of SC converter, which are charging and discharging modes. The total charge of the charging mode is assumed to equal the total charge in the discharging mode [3]. By studying the charge flow, the SC converter voltage gain, the slow switching limit (SSL), and the fast switching limit (FSL) can be obtained. The output impedance at the SSL limit is proportional to the switching frequency, and the capacitors' sizes while the output impedance at the FSL limit depends on the switches resistance R_{ds_on} [4].

However, the SC converters are not ideal or without drawbacks. For instance, providing a higher voltage gain is unlikely to be achieved with SC converters. Furthermore, the SC converters cannot normalize the output voltage in a lossless approach due to the R_{ds_on} resistors [5–8]. The proposed step-up PSC converter has demonstrated a higher gain voltage at a smaller number of elements compared to other SC topologies. The PSC converter has a gain voltage $V_{out} = 2^n V_{in}$ where n is the number of stages. Each added stage requires two additional capacitors and four more switches [7]. Unlike the other SC converters' topologies, the number of operation modes increase with the number of levels. Each level of the PSC converter has two operation modes. For instance, the 1-to-4 PSC converter (two-levels) as in Figure 1 operates in four operation modes, where three-levels operate in six operation modes. To achieve a superior efficiency achievement purpose, it is recommended that SC converters are designed with resonant soft-switching techniques. However, designing resonant SC converters requires additional components, and hence a reduction in the power density is possible [9–17].

The work in [18–24] proposed an alternative way of soft switching which is called a soft-charging operation. The main advantage of applying the soft-charging technique instead of soft-switching is it is not essential to add more components to optimize the fundamental efficiency [18]. Eliminating the current transient to increase the fundamental efficiency and the power density are the major functions of the soft-charging technique. In conventional operation (hard-charging), there are two ways to reduce the current transient, either by large capacitors selection or a higher f_{sw}. However, these two implementations reduce the power density and the fundamental efficiency respectively. To overcome the current transient issue, the complete soft-charging techniques are proposed to achieve that with a lower f_{sw} and smaller capacitors [22]. Resizing the capacitors in soft-charging techniques can be done theoretically by analyzing the voltage change and charge flow for each capacitor. In addition to resizing the capacitors, the output capacitor is eliminated in the soft-charging technique. Incomplete soft-charging and complete soft-charging are the two types of soft-charging. One significant difference between them is the complete soft-charging operation operates in a split-phase control diagram. The proposed control for Dickson SC converter [23] splits each operation mode into two modes, which are the conventional modes besides the transition modes.

In this paper, the complete soft-charging operation has been applied to the proposed PSC converter in [7]. A control diagram has been proposed to achieve a complete soft-charging in a 1-to-4 PSC converter. Achieving the complete soft-charging shows an output impedance reduction and a superior efficiency achievement to the 1-to-4 PSC converter. In addition, the split-phase successfully recovered the current transient. The reason for that is due to the dead time of the control diagram. However, reducing the capacitor size caused a high output voltage ripple. To overcome the ripple issues, an output LC filter has been inserted into the 1-to-4 PSC converter. The rest of the paper will be organized as follows: Section 2 will contain series of PSC converters, topology, and operation, and then the incomplete soft-charging operation of the second order PSC converter comes in Section 3. In Section 4, the complete soft-charging operation of the second order PSC converter is described. The result and discussion come in Section 5 before the conclusion.

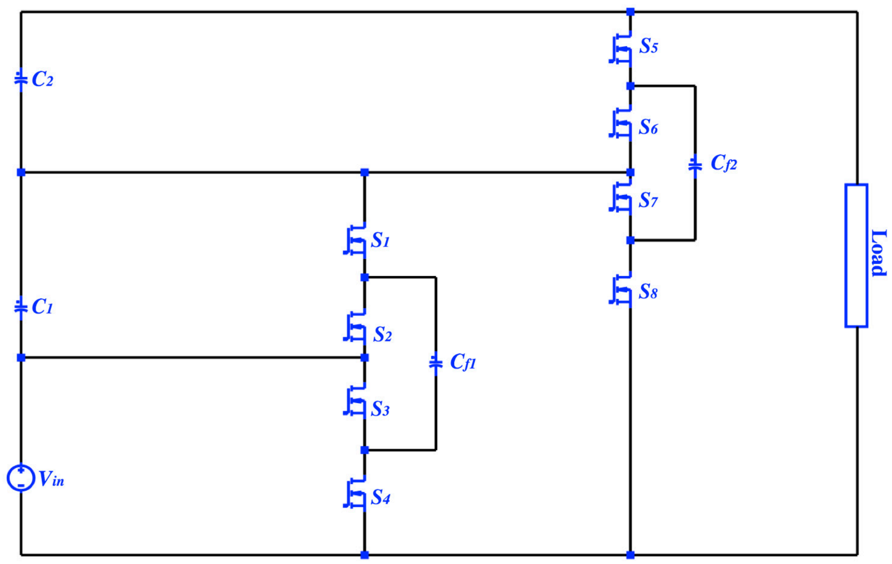


Figure 1. A 1-to-4 PSC topology (two-stage).

2. A Series of PSC Converters

2.1. A Second-Order PSC Converter; Topology and Operation

Figure 1 shows the topology of the 1-to-4 PSC converter and its control signals [7]. The control diagram in Figure 2a shows how four modes of operation are possible. The operation modes come in the following sequence: Mode-1, Mode-2, Mode-3, Mode-4, and Mode-1. In each mode, the capacitors are connected differently for voltage regulation purposes. In Mode-1 the flying capacitor C_{f1} is charging; however, flying capacitor C_{f2} is discharging. In Mode-2, both flying capacitors C_{f1} and C_{f2} are discharging, whereas they are both charging in Mode-4. In Mode-3 C_{f1} is discharging whereas C_{f2} is charging. To find the voltage gain of the proposed converter, each mode has a total charge that can be derived from the following equations.

$$QT_i = V_{C_1}C_1 + V_{C_2}C_2 + V_{C_{f1}}C_{f1} + V_{f2}C_{f2} \tag{1}$$

where i is the number of modes 1, 2, 3 and 4. From Mode-1 Figure 2

$$V_{C_{f1}} = V_{C_1} \tag{2}$$

$$V_{C_2} = V_{C_{f2}} \tag{3}$$

$$V_{C_{f1}} = V_o - V_{in} - V_{C_{f2}} \tag{4}$$

by substituting (2), (3) and (4) in (1) we get the total charge of Mode-1 (5)

$$QT_1 = V_{in}\left(-C_{f1} - C_1\right) + V_{f2}(C_2 + C_{f2} - C_1 - C_{f1}) + V_o\left(C_1 + C_{f1}\right) \tag{5}$$

To find the total charge of the rest of the modes, the same steps can be repeated

$$QT_2 = V_{in}\left(C_{f1} - C_1\right) + V_{f2}(C_1 + C_{f2} - C_2) + V_{out}C_2 \tag{6}$$

$$QT_3 = V_{in}\left(-C_{f1} - C_1\right) + V_{f2}(C_1 + C_{f1} + C_{f2} - C_2) + V_{out}C_2 \tag{7}$$

$$QT_4 = V_{in}\left(C_{f1} - C_1\right) + V_{f2}(-C_1 + C_{f2} + C_2) + V_{out}C_1 \tag{8}$$

In the steady state operation, the total charge of any two modes is assumed to be equal. In this work, we assumed that

$$QT_1 = QT_4 \tag{9}$$

$$QT_2 = QT_3 \tag{10}$$

By simplifying (9) and (10) we get

$$2V_{in}C_{f1} + V_{f2}C_{f1} - V_{out}C_{f1} = 0 \tag{11}$$

$$2V_{in}C_{f1} - V_{f2}C_{f1} = 0 \tag{12}$$

By combining (11) and (12), the 1-to-4 PSC converter's voltage gain can be calculated (13)

$$V_{out} = 4V_{in} \tag{13}$$

The general form of the proposed converter is

$$V_{out} = 2^n V_{in} \tag{14}$$

where n is the number of the stage. The output voltages of the one and two stages of PSC converter are presented in Figure 3.

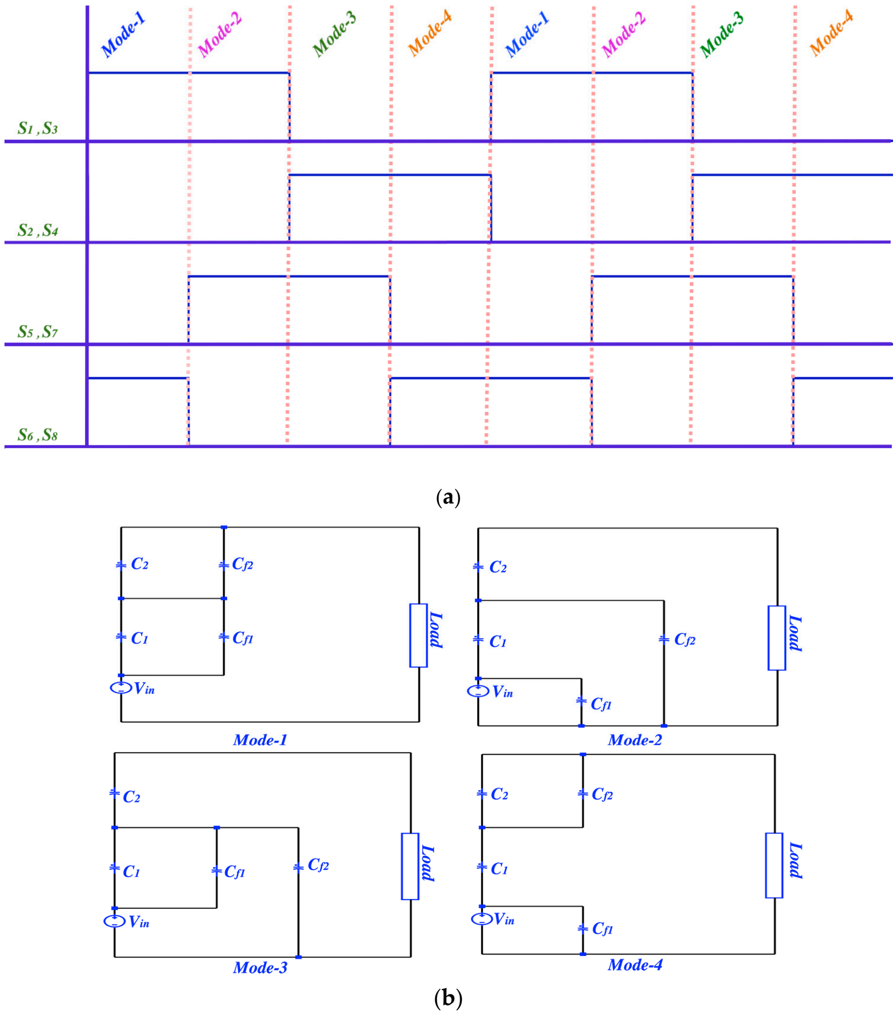


Figure 2. (**a**) Timing diagram of a 1-to-4 PSC topology; (**b**) four-mode operation of a 1-to-4 PSC converter.

For each added stage, two capacitors and four switches are needed. Figure 4 presents three stages of the proposed converter with 1-to-8 conversion ratio.

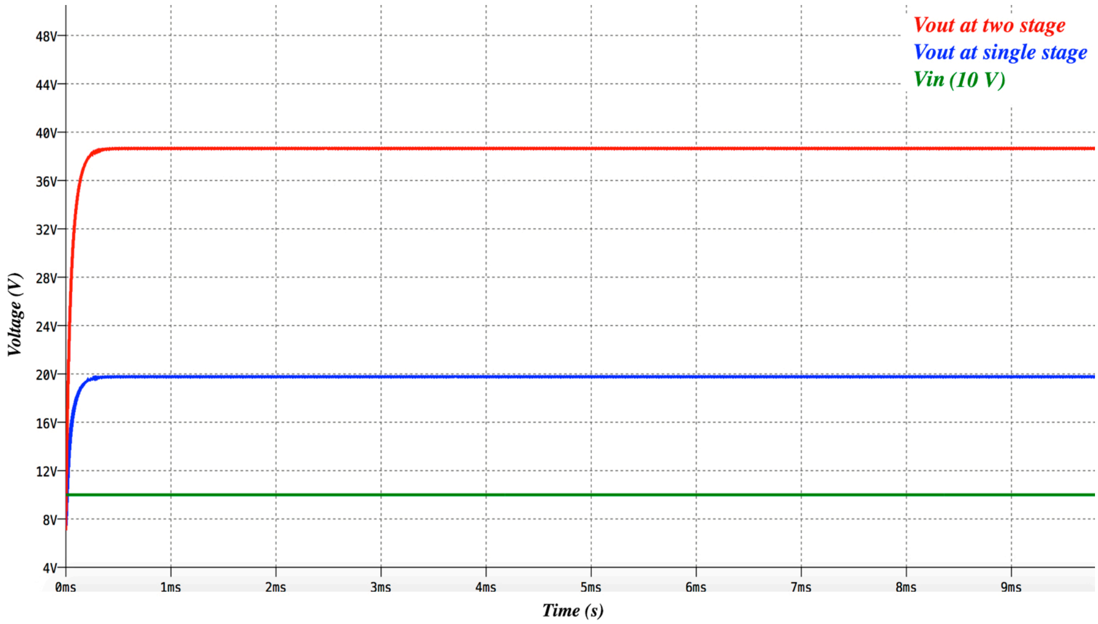


Figure 3. The input and output voltages of a 1-to-4 and 1-to-2 of the proposed PSC converter.

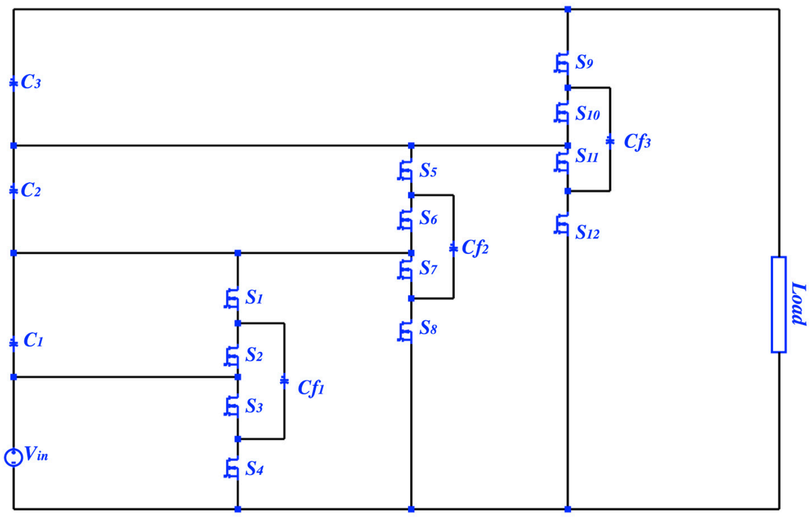


Figure 4. A 1-to-8 PSC topology (three-stage).

2.2. Slow-Switching Limit Impedance (R_{ssl})

The SC converters suffer from losses related to the switches and the capacitors' charging or discharging process. This capacitors' loss can be characterized as an output impedance that is called a slow switching limit impedance, R_{ssl}. The charge flow analysis of the four modes has been applied to find the charge multiplier of the four capacitors a_c^i

$$q_c^i = a_c^i \, q_{out} \tag{15}$$

$$q_c = [q_{C_1} q_{C_2} q_{C_{f1}} q_{C_{f2}}]^T \tag{16}$$

In [18–22] a useful technique was used to find the charge flow vectors of all the operation modes. For the ith mode, KCL can be derived by (17)

$$B_i q^i = 0 \tag{17}$$

where B_i is reduced incidence matrices of the four modes of 1-to-4 PSC converter. Each row in B_i corresponds to an independent KCL equation. The number of independent KCL equations can be derived by the number of nodes. Each element in the circuit has two nodes related to its positive and negative terminals as in Figure 5 [24,25].

$$\begin{gathered}
B_1 = \begin{bmatrix} -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & -1 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 0 & -1 & 1 \\ 1 & 0 & 0 & 0 & 0 & -1 \end{bmatrix} \\
B_{2,a} = \begin{bmatrix} -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & -1 & -1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & -1 & -1 & 1 \end{bmatrix} \\
B_{3,a} = \begin{bmatrix} -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & -1 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & -1 & -1 \end{bmatrix} \\
B_{4,a} = \begin{bmatrix} -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & -1 & -1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & -1 & 1 \\ 1 & 0 & 0 & -1 & 0 & -1 \end{bmatrix}
\end{gathered} \tag{18}$$

To find the charge flow's vectors, (17) can be solved for q^i.

$$\begin{gathered}
q^1_{Flow} = \begin{bmatrix} 3 \\ 1 \\ 1 \\ 2 \\ 2 \\ 3 \end{bmatrix} \quad q^2_{Flow} = \begin{bmatrix} -3 \\ -1 \\ -1 \\ -2 \\ -2 \\ -1 \end{bmatrix} \\
q^3_{Flow} = \begin{bmatrix} 3 \\ 1 \\ 1 \\ 2 \\ 2 \\ 1 \end{bmatrix} \quad q^4_{Flow} = \begin{bmatrix} -3 \\ -1 \\ -1 \\ -2 \\ -2 \\ -1 \end{bmatrix}
\end{gathered} \tag{19}$$

The total output charge with respect to the output charge can be found in (18)

$$q_{out} = q^1_{out} + q^2_{out} + q^3_{out} + q^4_{out} \tag{20}$$

The total output charge with respect to the input charge is

$$q_{out,total} = q_{in} + \frac{q_{in}}{3} + \frac{q_{in}}{3} + \frac{q_{in}}{3} = 2q_{in} \tag{21}$$

By using (21), (19) can be rewritten with respect to the output charge (22)

$$q_c^1 = \begin{bmatrix} \frac{q_{out}}{2} \\ \frac{q_{out}}{2} \\ q_{out} \\ q_{out} \\ \frac{3q_{out}}{2} \end{bmatrix} q_c^2 = \begin{bmatrix} \frac{-q_{out}}{2} \\ \frac{-q_{out}}{2} \\ -q_{out} \\ -q_{out} \\ \frac{-q_{out}}{2} \end{bmatrix} q_c^3 = \begin{bmatrix} \frac{q_{out}}{2} \\ \frac{q_{out}}{2} \\ q_{out} \\ q_{out} \\ \frac{q_{out}}{2} \end{bmatrix} q_c^4 = \begin{bmatrix} \frac{-q_{out}}{2} \\ \frac{-q_{out}}{2} \\ -q_{out} \\ -q_{out} \\ \frac{-q_{out}}{2} \end{bmatrix} \tag{22}$$

By applying (15), the charge multipliers are presented in (23)

$$a_c^1 = \begin{bmatrix} \frac{1}{2} \\ \frac{1}{2} \\ 1 \\ 1 \\ \frac{3}{2} \end{bmatrix} a_c^2 = \begin{bmatrix} \frac{-1}{2} \\ \frac{-1}{2} \\ -1 \\ -1 \\ \frac{-1}{2} \end{bmatrix} a_c^3 = \begin{bmatrix} \frac{1}{2} \\ \frac{1}{2} \\ 1 \\ 1 \\ \frac{1}{2} \end{bmatrix} a_c^4 = \begin{bmatrix} \frac{-1}{2} \\ \frac{-1}{2} \\ -1 \\ -1 \\ \frac{-1}{2} \end{bmatrix} \tag{23}$$

Then by using Tellegen's theorem, R_{ssl} can be found for our proposed design (24).

$$\frac{3V_{out}}{q_{out}} + \sum_{i=1}^{number\ of\ C} \frac{(a_{c,i})^2}{2C_i fsw} = 0 \tag{24}$$

where $\frac{V_{out}}{q_{out} fsw} = R_{ssl}$

$$R_{ssl} = \frac{1}{6} \sum_{i=1}^{number\ of\ C} \frac{(a_{c,i})^2}{C_i fsw} \tag{25}$$

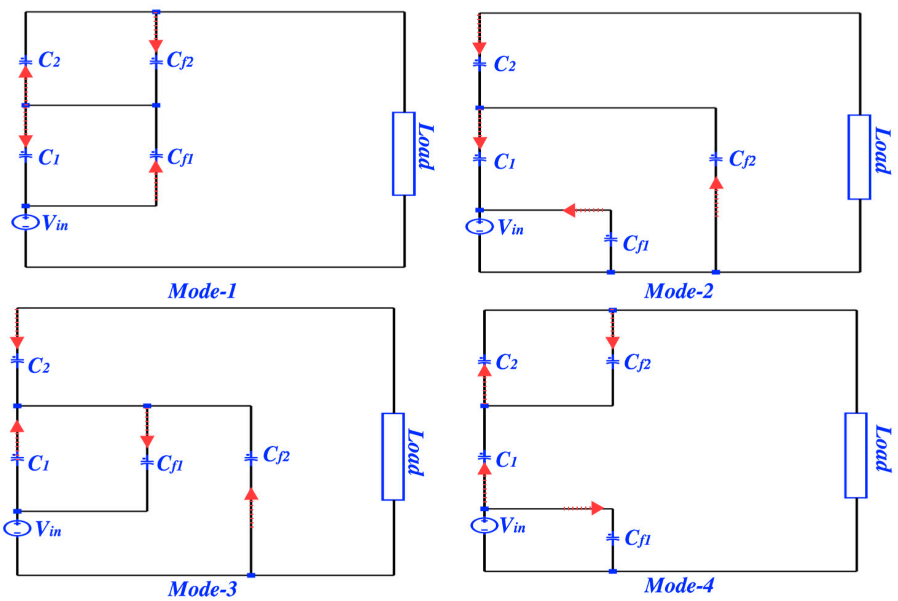


Figure 5. The charge flow for the operation modes in the 1-to-4 PSC converter.

2.3. Fast-Switching Limit Impedance

Another important parameter can be determined by analyzing the SC converter to find the fast switching limit (R_{Fsl}). In the SC converter, two parameters are responsible for increasing the efficiency, which are a high switching frequency and a large capacitor size. The R_{Fsl} depends on the switches' R_{ds_on} as in the following equation

$$R_{Fsl} = 4\sum_{i=1}^{number\ of\ S} R_{ds\_on}(a_{r,i})^2 \tag{26}$$

where $(a_{r,i})$ is the charge multiplier of eight switches in the 1-to-4 PSC converter.

3. An Incomplete Soft-Charging Operation of the Second Order PSC Converter

For more convenience, a constant output current source is used as an output load in the soft-charging analysis [18–21]. In addition, the PSC converter is designed with a lossless output capacitor to recover the voltage differences. The current transient and the voltage mismatch dispersions are the essential benefits of the soft-charging technique. However in the hard-charging operation, requirements of a higher switching frequency or a larger capacitor selection are needed to eliminate the current transient. To determine the flowing charge and the changing capacitors' voltage for the 1-to-4 PSC converter, we applied a KCL. Corresponding to the timing diagram in Figure 2a, four operation modes are presented in Figure 2b. The elements of each circuit in Figure 2b, which are V_{in}, V_{C_1}, V_{C_2}, $V_{C_{f1}}$, $V_{C_{f2}}$ and V_{out}, can be written in a voltage vector form.

$$V = [V_{in}\ V_{C_1}\ V_{C_2}\ V_{C_{f1}}\ V_{C_{f2}}\ V_{out}]^T \tag{27}$$

Each phase in Figure 2b has four possible loops that can be expressed in a reduced matrix loop (29) [24]

$$A_i V^i = 0 \tag{28}$$

the reduced matrix's loops for the four modes can be written as in (29),

$$\begin{aligned}
A_1 &= \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ -1 & -1 & 0 & 0 & -1 & 1 \\ -1 & 0 & 0 & -1 & -1 & 1 \\ -1 & 0 & -1 & -1 & 0 & 1 \end{bmatrix} \\
A_2 &= \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ -1 & -1 & 0 & 0 & 1 & 0 \\ 0 & -1 & -1 & -1 & 0 & 1 \\ 0 & 0 & -1 & 0 & -1 & 1 \end{bmatrix} \\
A_3 &= \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ -1 & 0 & 0 & -1 & 1 & 0 \\ -1 & 0 & -1 & -1 & 0 & 1 \\ -1 & -1 & 0 & 0 & 1 & 0 \end{bmatrix} \\
A_4 &= \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ 0 & -1 & -1 & -1 & 0 & 1 \\ 0 & -1 & 0 & -1 & -1 & 1 \\ -1 & -1 & 0 & 0 & -1 & 1 \end{bmatrix}
\end{aligned} \tag{29}$$

At the end of each mode, the voltage vectors become $\Delta V^i + V^i$

$$A_i\left(\Delta V^i + V^i\right) = 0 \tag{30}$$

where ΔV^i is the voltage change related to the load received charge. From (28) and (30), we have

$$A_i \Delta V^i = 0 \tag{31}$$

In the steady state assumption, the total voltages changes for the four operation modes equal zero.

$$\Delta V^1 + \Delta V^2 + \Delta V^3 + \Delta V^4 = 0 \tag{32}$$

since V_{in} is a constant DC source, then $\Delta V_{in} = 0$. To satisfy $\Delta V_{in} = 0$ a row with $\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$ is added to A_i

$$\Delta V^1 = a_1 W_1 + a_2 W_2$$

$$
\begin{aligned}
\Delta V^2 &= b_1 U_1 + b_2 U_2 \\
\Delta V^3 &= c_1 H_1 + c_2 H_2 \\
\Delta V^4 &= d_1 X_1 + d_2 X_2
\end{aligned} \tag{33}
$$

where $W_1,\ W_2\ U_1,\ U_2\ H_1,\ H_2,\ X_1,\ X_2$ are null spaces of the modified A_i matrices (after adding $\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$).

$$
W = \left\{ \begin{bmatrix} 0 \\ 0.3541 \\ -0.5891 \\ 0.3541 \\ -0.5891 \\ -0.235 \end{bmatrix}, \begin{bmatrix} 0 \\ 0.4996 \\ 0.1673 \\ 0.4996 \\ 0.1673 \\ 0.6669 \end{bmatrix} \right\}
$$

$$
U = \left\{ \begin{bmatrix} 0 \\ 0.6295 \\ -0.3832 \\ 0 \\ 0.6295 \\ 0.2463 \end{bmatrix}, \begin{bmatrix} 0 \\ 0.0612 \\ 0.6732 \\ 0 \\ 0.0612 \\ 0.7344 \end{bmatrix} \right\}
$$

$$
H = \left\{ \begin{bmatrix} 0 \\ -0.1035 \\ -0.642 \\ -0.1035 \\ -0.1035 \\ -0.7455 \end{bmatrix}, \begin{bmatrix} 0 \\ 0.5244 \\ -0.3991 \\ 0.5244 \\ 0.5244 \\ 0.1253 \end{bmatrix} \right\}
$$

$$
X = \left\{ \begin{bmatrix} 0 \\ 0.6136 \\ -0.5569 \\ 0 \\ -0.5569 \\ 0.0566 \end{bmatrix}, \begin{bmatrix} 0 \\ 0.4728 \\ 0.2997 \\ 0 \\ 0.2997 \\ 0.7725 \end{bmatrix} \right\} \tag{34}
$$

The voltage change ΔV^i can be calculated by

$$
\begin{aligned}
\Delta V^1 &= a_1 W_1 + a_2 W_2 \\
\Delta V^2 &= b_1 U_1 + b_2 U_2 \\
\Delta V^3 &= c_1 H_1 + c_2 H_2 \\
\Delta V^4 &= d_1 X_1 + d_2 X_2
\end{aligned} \tag{35}
$$

where $a_1, a_2, a_3, a_4, b_1, b_2, b_3$ and b_4 can be found by (36), and $\overline{W_1}\ \ \overline{W_2}\ \ \overline{U_1}\ \ \overline{U_2}\ \ \overline{H_1}\ \ \overline{H_2}\ \ \overline{X_1}\ \ \overline{X_2}$ are the reduced form of $W_1, W_2\ U_1,\ U_2\ H_1,\ H_2,\ X_1$ and X_2 (after eliminating the last row corresponding to ΔV_{out}). The ΔV_{out} is zero at an inductive load case.

$$
\begin{bmatrix} \overline{W_1} & \overline{W_2} & \overline{U_1} & \overline{U_2} & \overline{H_1} & \overline{H_2} & \overline{X_1} & \overline{X_2} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = 0 \tag{36}
$$

$$\begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} -0.6794 \\ 0.3024 \\ -0.3050 \\ -0.1486 \\ 0.0837 \\ 0.1872 \\ 0.4934 \\ -0.215 \end{bmatrix} \tag{37}$$

Now (35) can be solved to calculate ΔV^i.

$$\Delta V^1 = \begin{bmatrix} 0 \\ -0.0895 \\ 0.4508 \\ -0.0895 \\ 0.4508 \\ 0.3613 \end{bmatrix} \Delta V^2 = \begin{bmatrix} 0 \\ -0.2011 \\ 0.0168 \\ 0 \\ -0.2011 \\ -0.1843 \end{bmatrix}$$

$$\Delta V^3 = \begin{bmatrix} 0 \\ -0.0895 \\ -0.1284 \\ 0.0895 \\ 0.0895 \\ -0.0389 \end{bmatrix} \Delta V^4 = \begin{bmatrix} 0 \\ 0.2011 \\ -0.3392 \\ 0 \\ -0.3392 \\ -0.1382 \end{bmatrix} \tag{38}$$

From (19) and (38) the capacitor sizes can be found by (39)

$$C_j = q_j / \Delta V_{Cj} \tag{39}$$

4. A Complete Soft-Charging Operation of the Second Order PSC Converter

The complete soft-charging analysis can be satisfied if and only if the KVL exists at all operation modes including the four transitions modes. In this section, we proposed a split-phase control for the 1-to-4 PSC converter. The control diagram in Figure 6a allows eight modes of operation to exist as in Figure 6b. Four of those modes are the same as the four modes of the conventional PSC converter Figure 2b where the new four modes are basically the transition modes. The same procedures as applied for the incomplete soft-charging are repeated in this section. The A_i and B_i matrices Mode-1a, Mode-2a, Mode-3a and Mode-4a are the same matrices as in Section 2. Since the extra four transition modes have three capacitors then only two KVL loops are possible for A_i matrices, which are presented as in following reduced loop.

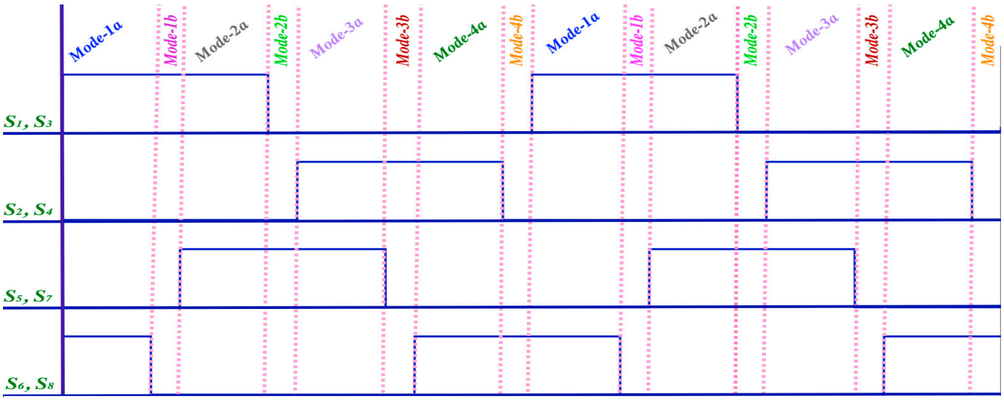
$$A_{1b} = \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ -1 & 0 & -1 & -1 & 0 & 1 \end{bmatrix}$$

$$A_{2b} = \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ 0 & -1 & -1 & -1 & 0 & 1 \end{bmatrix}$$

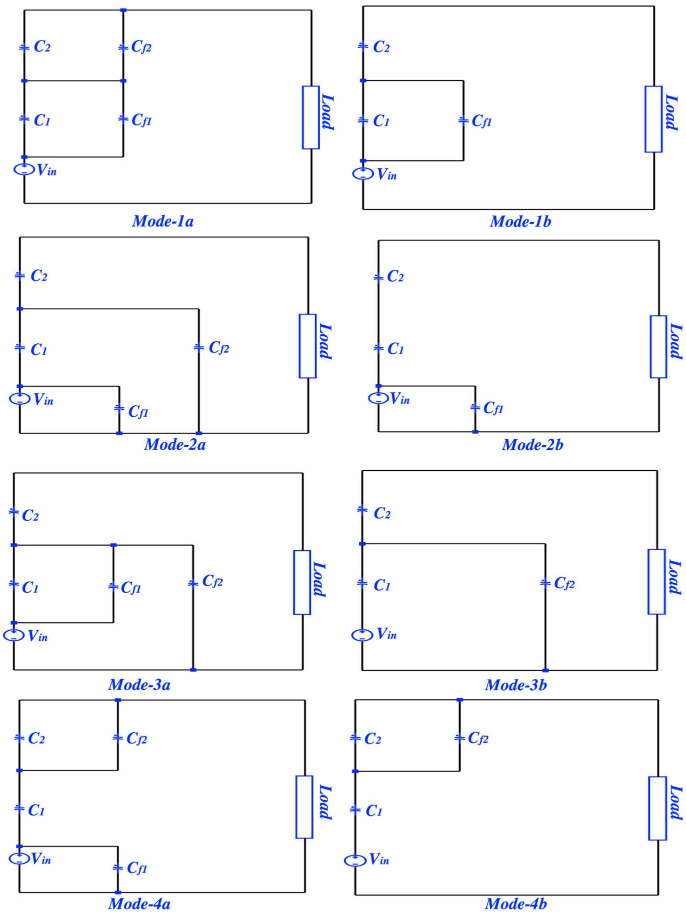
$$A_{3b} = \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ -1 & -1 & 0 & 0 & 1 & 0 \end{bmatrix}$$

$$A_{4b} = \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ -1 & -1 & 0 & 0 & -1 & 1 \end{bmatrix} \tag{40}$$

Although the transition modes contain three capacitors, their charge flow directions are the same as the charge flow direction of the basic modes as in Figure 5. However, the number of nodes in the transition modes is five instead of four due to the floating capacitor terminals. Since both terminals are floating, they are considered one node and expressed in an extra row in B_i. By using (17), the reduced matrices of the transition modes as in Figure 7 are presented as following (41).



(**a**)



(**b**)

Figure 6. (**a**) A proposed timing diagram to achieve a complete soft-charging in the 1-to-4 PSC converter; (**b**) eight operation modes of the 1-to-4 PSC converter in the complete soft-charging technique.

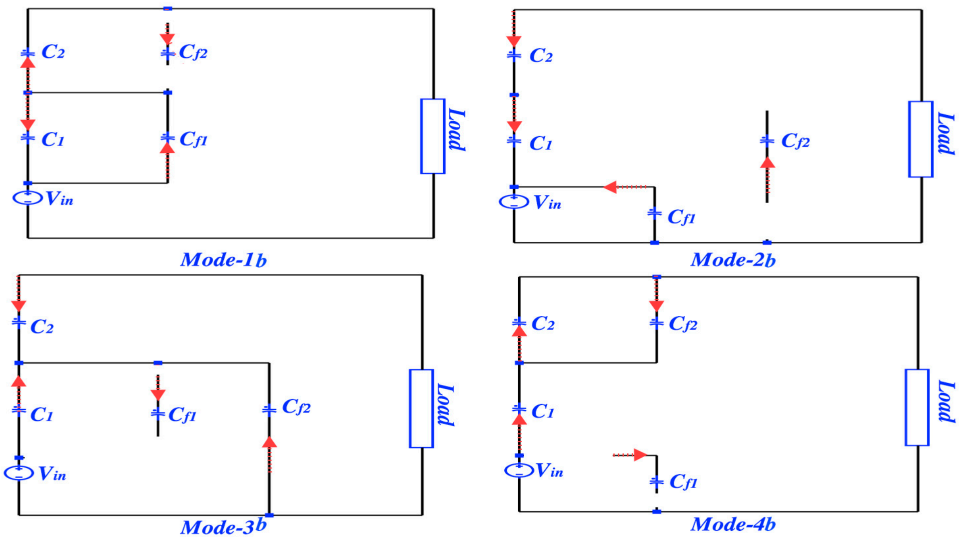


Figure 7. The charge flow for the operation modes in the 1-to-4 PSC converter.

$$B_{1b} = \begin{bmatrix} -1 & -1 & 0 & 1 & 0 & 0 \\ 0 & -1 & 1 & -1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}$$

$$B_{2b} = \begin{bmatrix} -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & -1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & -1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}$$

$$B_{3b} = \begin{bmatrix} -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix}$$

$$B_{4b} = \begin{bmatrix} -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & -1 & -1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & -1 & 1 \\ 1 & 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix} \tag{41}$$

By applying the (17) the charge flow of the eight modes are

$$q_c^{1,a} = \begin{bmatrix} 3 \\ 1 \\ 1 \\ 2 \\ 2 \\ 3 \end{bmatrix} q_c^{1,b} = \begin{bmatrix} 1 \\ -1 \\ 1 \\ 2 \\ 0 \\ 1 \end{bmatrix}$$

$$q_c^{2,a} = \begin{bmatrix} -3 \\ -1 \\ -1 \\ -2 \\ -2 \\ -1 \end{bmatrix} q_c^{2,b} = \begin{bmatrix} -1 \\ 1 \\ -1 \\ -2 \\ 0 \\ -1 \end{bmatrix}$$

$$q_c^{3,a} = \begin{bmatrix} 3 \\ 1 \\ 1 \\ 2 \\ 2 \\ 1 \end{bmatrix} q_c^{3,b} = \begin{bmatrix} 1 \\ 1 \\ 1 \\ 0 \\ 2 \\ 1 \end{bmatrix}$$

$$q_c^{4,a} = \begin{bmatrix} -3 \\ -1 \\ -1 \\ -2 \\ -2 \\ -1 \end{bmatrix} q_c^{4,b} = \begin{bmatrix} -1 \\ -1 \\ -1 \\ 0 \\ -2 \\ -1 \end{bmatrix} \tag{42}$$

from (42), the last rows represent the output delivered charge. The total input charge equals 16 which is the sum of the input charges for all eight modes (42). The duty cycle of each mode to achieve a complete soft-charging is calculated in (43). Each mode has a certain duty cycle where the sum of the modes' duty cycles completes one period of the proposed split-phase control in Figure 6a.

$$D_{1a} = D_{2a} = D_{3a} = D_{4a} = \frac{q_{input\_i}}{q_{input\_total}} = \frac{3}{16}$$

$$D_{1b} = D_{2b} = D_{3b} = D_{4b} = \frac{q_{input\_i}}{q_{input\_total}} = \frac{1}{16} \tag{43}$$

The complete soft-charging operation allows us to resize the capacitors; however, small capacitor selection can result in a higher voltage ripple. To overcome the voltage's ripple, an output LC filter can be added to the output stage of the PSC converter. Figure 8 shows a 1-to-4 PSC with an output LC filter.

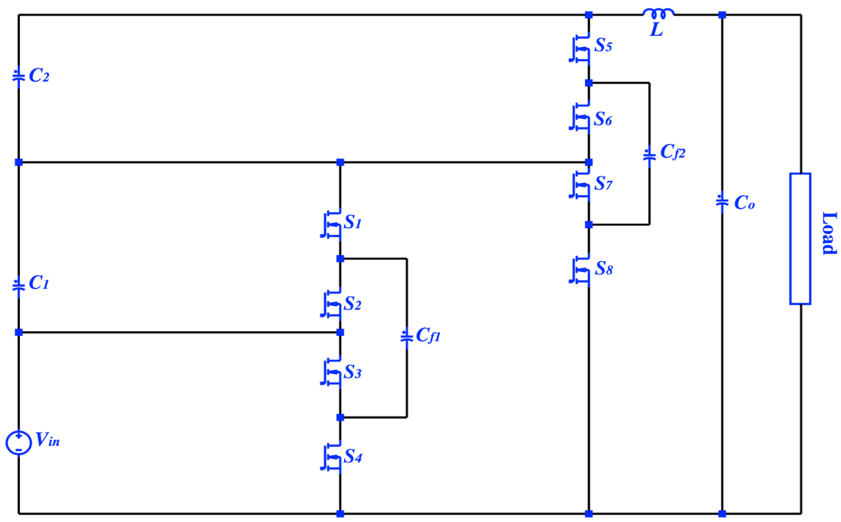


Figure 8. The 1-to-4 PSC topology with an output LC filter.

5. Results and Discussion

The simulation design has been completed to determine the proposed split-phase control for the 1-to-4 PSC converter. The proposed split-phase control successfully supports the 1-to-4 PSC converter to achieve its complete soft-charging operation. Eight operation modes are approached in the following sequences, Mode 1-a, Mode 1-b, Mode 2-a, Mode 2-b, Mode 3-a, Mode 3-b, Mode 4-a and Mode 4-b in the soft-charging operation. However, only four operation modes were possible by controlling them conventionally, Figure 2. The scheme needs eight switches and four capacitors to rate a 40 V nominal output voltage with a supplied voltage of 10 V. The voltage stresses across the switches either 0.25 V_{out} or 0.5 V_{out} as. Due to the switches' stresses and the rated output voltage, all eight switches are selected to rate 40 V. Direct comparisons among four operation techniques, which are hard-charging, incomplete soft-charging, complete soft-charging-I and complete soft-charging-II, are presented in this section. In the hard-charging approach, C_1, C_2, C_{f1} and C_{f2} are selected equally with a capacitance equal to 188 µF. Corresponding to (38), C_{f1} and C_{f2} have the lowest voltage change; C_1, and C_2 have the highest voltage change. Hence by using (39) C_1, C_2, C_{f1} and C_{f2} are selected differently (Sections 3 and 4). In the incomplete soft-charging and complete soft-charging-I operations, C_1 and C_2 have a size equals to half of the C_{f1} and C_{f2} as in Table 1 which are 90 µF and 188 µF respectively. Due to the switching dead time, the proposed split-phase control allows for more decrease of C_1, C_2, C_{f1} and C_{f2} sizes. The converter with reduced capacitors is referred to as a complete soft-charging-II in Table 2. Reducing the capacitors sizes outcomes in a lower output impedance. Figure 9 shows the output impedance versus the switching frequency at hard-charging, incomplete soft-charging and complete soft-charging-II. It can be clearly seen that the output impedance eventually decreases at a higher switching frequency selection. However, unlike the hard-charging operation, applying the complete soft-charging-II technique keeps the output impedance almost constant at varied switching frequencies. Having an almost constant output impedance means the 1-to-4 PSC converter participates the FSL limits at a lower f_{sw}. Moreover, the split-phase control helps to eliminate the voltage mismatch between any two parallel capacitors. The voltage mismatch between $V_{Cf2} - V_{C2}$ and $V_{Cf2} - V_{in}$ has been recovered by applying split-phase control as in Figures 10 and 11. In addition to eliminating the voltage mismatch, the complete soft-charging removes the current transient in the flying capacitors as in Figure 12. The decrease of the output impedance and the dead time switching should effectively recover the fundamental efficiency. However, reducing capacitor size causes an undesired higher output voltage ripple. To overcome the output voltage ripple, an output LC filter was added to the PSC converter as presented in Figure 9. (44), shows an equation to determine L where C is the equivalent capacitance in the 1-to-4 PSC converter [22].

$$f_{sw} \geq \frac{1}{2\pi\sqrt{LC}} \tag{44}$$

The general output impedance in the SC converters can be calculated by using (45) [22]

$$R_{out} = \frac{\frac{V_{in}}{N} - V_{out}}{I_{out}} \tag{45}$$

Figure 13 shows the 1-to-4 PSC efficiency against the I_{out} in four compared operations. The highest achieved efficiency occurs at the complete soft-charging-II with the LC filter insertion. Adding the LC filter could decrease the efficiency; however, this reduction is small compared to the high increase of the efficiency by using the soft-charging-II operation.

Table 1. Equation of the voltage stress on all semiconductor and capacitors.

Elements	Equation
S_1, S_2, S_3, S_4	V_{in}
S_5, S_6, S_7, S_8	$2V_{in}$
C_1, C_2, C_{f1}	V_{in}
C_{f2}	$2V_{in}$

Table 2. Simulation parameters.

Parameter	Value
V_{in}	10 V
f_{sw}	200 KHz
$C_1, C_2, C_{f1}C_{f2,hard-charging}$	188 µF
$C_{f1}, C_{f2complete\ soft-charging-I\ and\ incomplete\ soft-charging}$	94 µF
$C_{f1}, C_{f2complete\ soft-charging-I\ and\ incomplete\ soft-charging}$	188 µF
$C_1, C_{2-complete\ soft-charging-II}$	20 µF
$C_{f1}, C_{f2-complete\ soft-charging-II}$	40 µF
$C_{o-hard-charging}$	200 µF
L of LC filter	50 nH

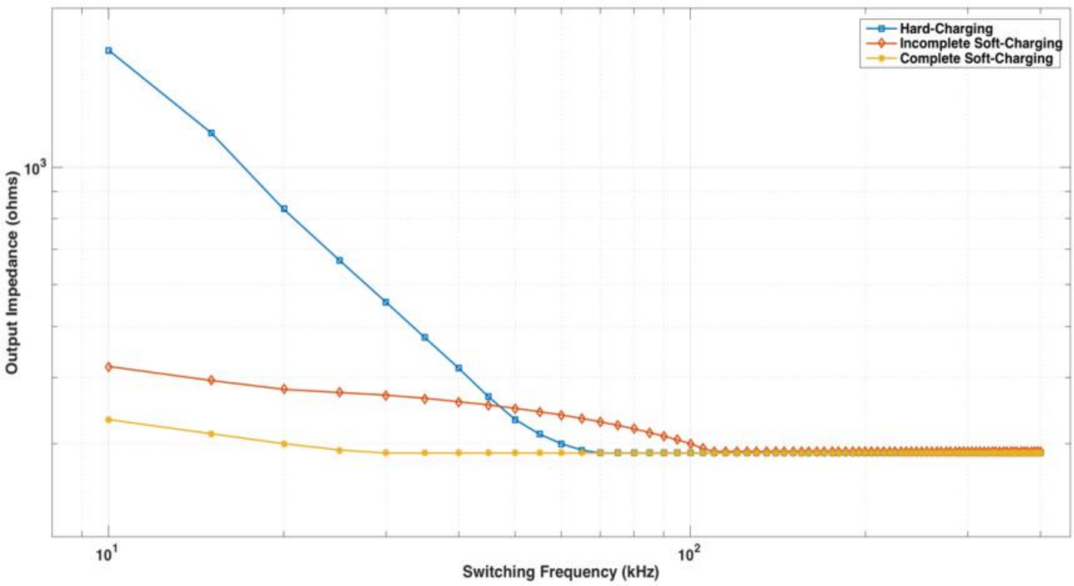


Figure 9. Simulation output impedance of the 1-to-4 PSC converter vs. the switching frequency at three charging methods: hard-charging, incomplete soft-charging, complete soft-charging II.

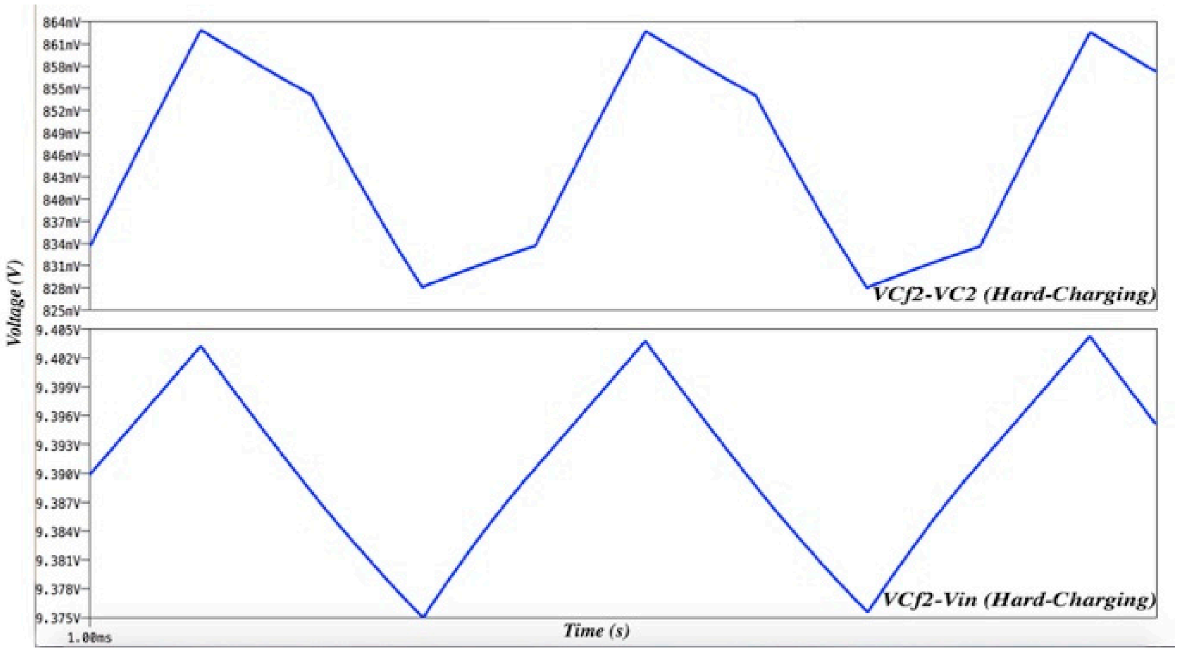


Figure 10. Capacitor voltage mismatch during hard-charging between $V_{Cf2} - V_{C2}$ and $V_{Cf2} - V_{in}$.

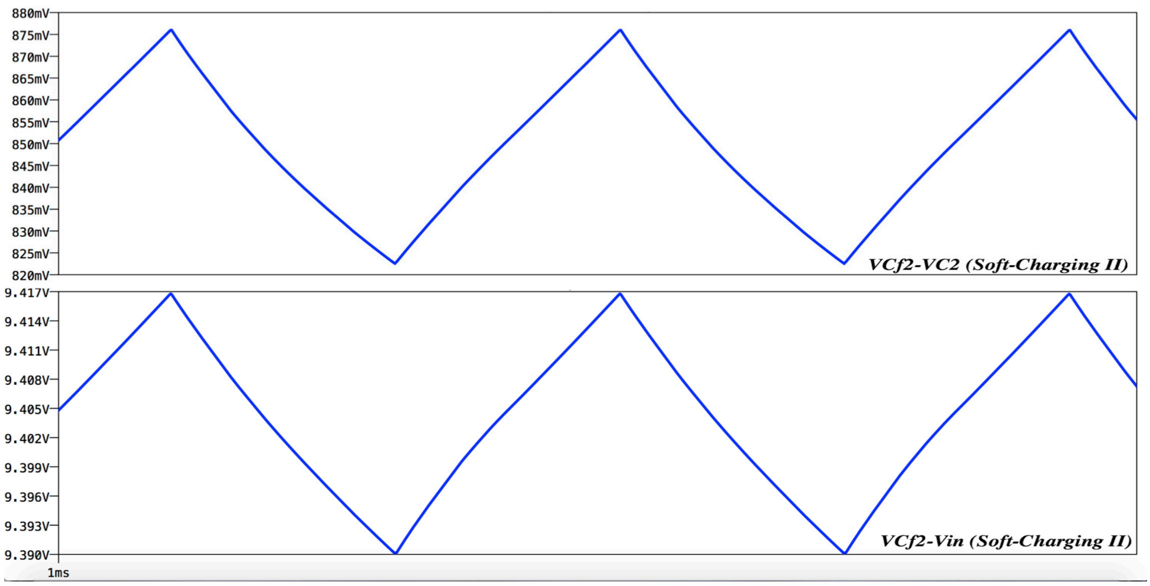


Figure 11. The elimination of the capacitor voltage mismatch during complete soft-charging II between $V_{Cf2} - V_{C2}$ and $V_{Cf2} - V_{in}$.

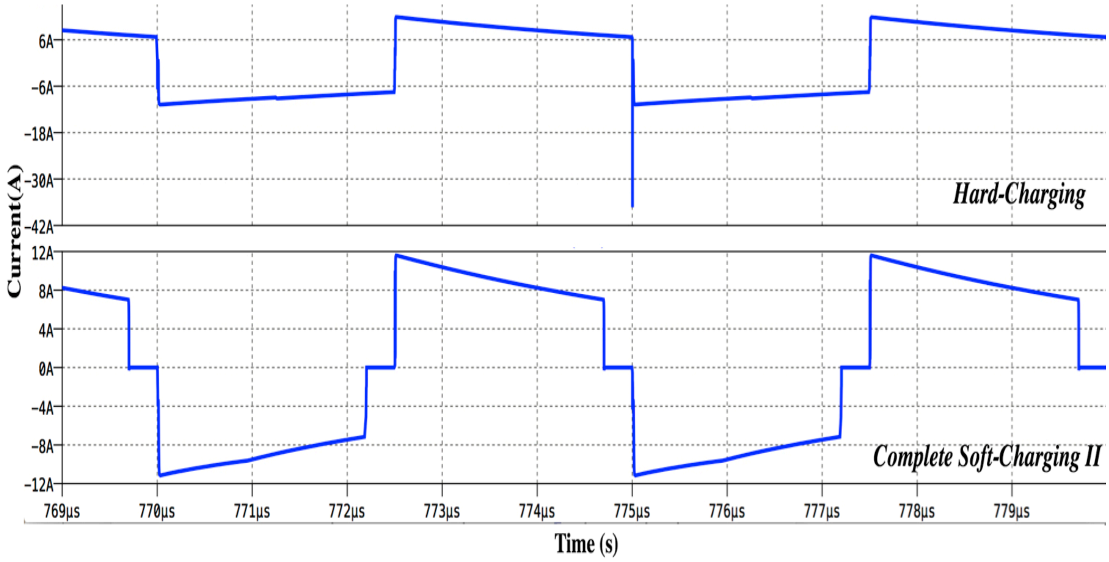


Figure 12. The current waveform of C_{f2} shows the transient in the hard-charging was eliminated by applying the complete soft-charging II.

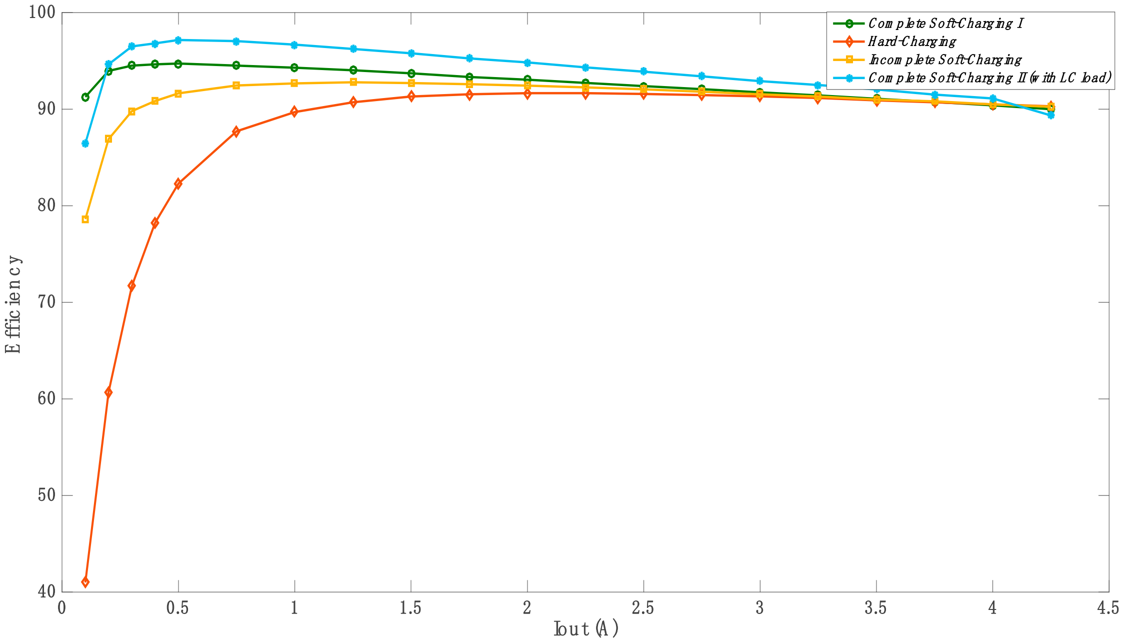


Figure 13. The PSC converter efficiency vs. the rated power at different operation techniques: hard-charging, incomplete soft-charging, complete soft-charging I and complete soft-charging II (with LC filter).

6. Conclusions

The proposed split-phase control allows the 1-to-4 PSC converter to operate in the complete soft-charging operation. The elimination of the current transient excellently increases both the efficiency and the power density. In addition to the output impedance reduction, the complete soft-charging operation leads to eliminating the voltage mismatch between any parallel capacitors. A theoretical analysis was successfully applied for resizing the capacitors in the soft-charging approach. Beyond the resizing approach, the theoretical analysis productively helps to calculate the duty cycles for each operation mode. The dead time of the proposed control diagram is the main reason behind achieving superior efficiency due to smaller switching losses and lower output impedance. However, a lower capacitor size causes a higher output voltage ripple. An output LC filter was added to the 1-to-4 PSC converter to reduce the output voltage ripple. Although adding the LC filter could cause a small loss; however, this loss is not effective to the efficiency which has been efficaciously increased by using the complete soft-charging-II technique.

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Conflicts of Interest: The authors declare no conflict of interest.

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