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# A Low-Power CMOS Piezoelectric Transducer Based Energy Harvesting Circuit for Wearable Sensors for Medical Applications

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Received: 20 September 2017; Accepted: 12 December 2017; Published: 18 December 2017

**Abstract:** Piezoelectric vibration based energy harvesting systems have been widely utilized and researched as powering modules for various types of sensor systems due to their ease of integration and relatively high energy density compared to RF, thermal, and electrostatic based energy harvesting systems. In this paper, a low-power CMOS full-bridge rectifier is presented as a potential solution for an efficient energy harvesting system for piezoelectric transducers. The energy harvesting circuit consists of two n-channel MOSFETs (NMOS) and two p-channel MOSFETs (PMOS) devices implementing a full-bridge rectifier coupled with a switch control circuit based on a PMOS device driven by a comparator. With a load of 45 k $\Omega$ , the output rectifier voltage and the input piezoelectric transducer voltage are 694 mV and 703 mV, respectively, while the  $V_{OUT}$  versus  $V_{IN}$  conversion ratio is 98.7% with a PCE of 52.2%. The energy harvesting circuit has been designed using 130 nm standard CMOS process.

**Keywords:** AC-DC power conversion; energy harvesting; piezoelectric transducer; active rectifier; switch based rectifier

## 1. Introduction

Technological advancements in low-power CMOS processes have driven rapid development of sensor electronics such as implantable and wearable sensor systems. The powering of such sensor systems has remained a major problem since the traditional batteries can leak resulting in serious health problems in patients. Moreover, in typical sensor systems, the available space for batteries is very limited thereby restricting the battery capacity. Energy harvesting has emerged as one of the potential solutions for powering the sensor electronics and has been widely studied in recent years. Energy can be harvested from various ambient energy sources such as electromagnetic, wind, mechanical vibration, RF, and thermal energy etc. There are three general energy sources that utilize vibration, namely electrostatic, electromagnetic, and piezoelectric. Among these sources, the piezoelectric vibration based energy harvesting system has received a great deal of attention because of its ease of integration with electronic systems and moderate power density. Several rectifier circuits based on piezoelectric transducers have been reported in [1–7]. The circuits reported in [4–6] aim to reduce the voltage drop across rectifier diodes while references [2–9] aim to reduce the wasted charges associated with the charging of the plate capacitance of the piezoelectric transducer to further increase the overall efficiency of the systems. In [1,8,10], the researchers have used techniques called bias-flip and synchronized switch harvesting on inductor (SSHI) to improve the extraction of energy. However, the major problems associated with the schemes involve the requirement of relatively large inductors to improve the overall efficiency while still requiring very complex control circuits.

## 2. Piezoelectric Energy Harvester

### 2.1. General Architecture of Energy Harvesting System

Figure 1 shows a general building block or system architecture of a piezoelectric energy harvesting system [1,11]. A piezoelectric transducer can convert vibrational energy into electrical energy or can be used as a vibrational device by application of an electrical source such as a battery. When a piezoelectric transducer is used as an electrical energy generator, an AC voltage is produced at the output. Therefore, an AC-to-DC rectifier or an AC-to-DC converter must be constructed to acquire a useful DC output voltage. Since the energy generated by an AC-to-DC rectifier or a converter is not sufficient or stable enough to directly power up the system, the energy should be generally stored in a battery or a super capacitor followed by a regulator such as a DC-DC converter, LDO etc. In general, there are two types of conventional rectifiers: a voltage-doubler and a full-bridge rectifier [8]. The major drawbacks of these two conventional structures are usually low power extraction and low power conversion efficiencies. A low extraction efficiency is mainly attributed to charging and discharging of the internal parasitic capacitances of a piezoelectric transducer whenever it changes its polarity and the large voltage drop occurs due the diode turn-on voltage [8]. To overcome this drawback, a number of different schemes have been proposed such as synchronized switch harvesting on inductor, switch-only harvester, etc. In order to improve the conversion efficiency of a rectifier, a diode can be replaced by a CMOS circuit. A CMOS based rectifier has lower voltage drop compared to a conventional off-chip diode rectifier. In this paper, a CMOS synchronous switch based energy harvesting circuit is reported which offers several advantages over the schemes reported in literature due to its simplicity of design, moderate energy harvesting, and the requirement of no off-chip components except the output capacitor.

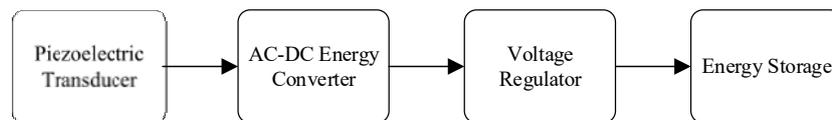


Figure 1. A general building block of a piezoelectric energy harvester.

### 2.2. Transducer Modeling

A piezoelectric device can be modeled in both mechanical and electrical domains that are coupled through a magnetic coil [12], as illustrated in Figure 2a [10,12,13]. In the mechanical domain model of a piezoelectric transducer,  $R_M$  represents the mechanical damping,  $C_M$  is the reciprocal mechanical stiffness, and  $L_M$  is the effective mass. In the electrical domain, the vibrational excitation can be modeled as a current source with a parasitic capacitance,  $C_P$  and a parasitic resistance,  $R_P$ . In the proposed CMOS active rectifier with a switch, a typical model of a piezoelectric device has been used. The parameter values for the piezoelectric transducer are chosen such that  $C_P$  is 25 nF,  $R_P$  is 1 M $\Omega$ , and  $I_P$  is 45  $\mu$ A.

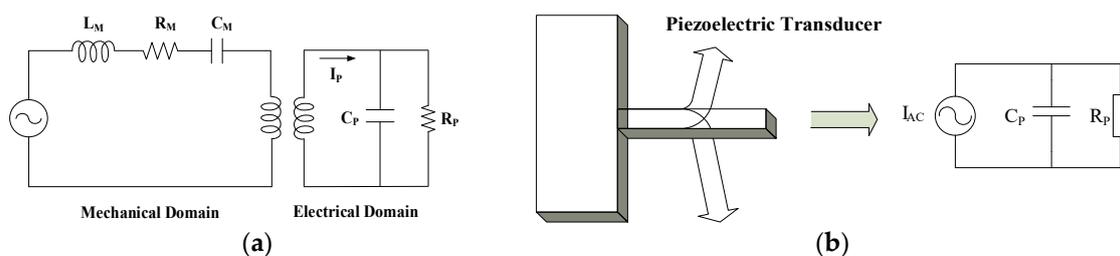


Figure 2. (a) Modeling of a piezoelectric transducer showing mechanical to electrical domain; (b) simplified model of a piezoelectric transducer [12].

### 3. CMOS Full-Wave Rectifier

#### 3.1. Operating Principle

As shown in Figure 2 [8], a piezoelectric transducer can be modeled as a sinusoidal current source  $i_p(t) = I_p \sin(2\pi f_p t)$ , in parallel with a parasitic plate capacitor,  $C_p$  and a parasitic resistor,  $R_p$ . The amplitude of a piezoelectric transducer current,  $I_p$  varies with the mechanical excitation level of the piezoelectric transducer while  $f_p$  represents the excitation frequency of the piezoelectric transducer.

A typical full-wave bridge rectifier consists of four diodes. The major problem of using an off-chip diode in a conventional rectifier circuit is that it results in a substantial voltage drop due to the diode turn-on voltage ( $V_d$ ), which is typically 0.5~0.7 V. This large turn-on voltage causes a significant loss in a conventional full-bridge rectifier. In addition, charging and discharging of the plate capacitance of a piezoelectric transducer results in a loss of available charges from the transducer. To overcome these problems, a CMOS based full-bridge rectifier with a switch-only circuit in parallel with a piezoelectric transducer is proposed in [8]. In the switch-only (SO) rectifier scheme, a switch is turned on whenever the transducer current crosses a zero which helps discharge the capacitor,  $C_p$ . Unlike a conventional rectifier, this process allows the SO rectifier not to discharge from  $(V_{RECT} + 2V_d)$ . Figure 3a,b show a conventional full-bridge rectifier and a rectifier with switch-only scheme, respectively. To reduce the voltage-drop across a diode which affects the conversion efficiency, a CMOS based full-wave bridge rectifier with a switch is presented in this paper. The advantages of this proposed design include the ability to power the proposed circuit to operate without requiring any off-chip components even though the power generated by the SO rectifier is less than that of the bias-flip or other power enhanced structures. This allows more flexibility to integrate the circuits with an integrated system. In addition, by using a separate control signal for the PMOS switch in a SO rectifier, the current for charging and discharging of  $C_{sg}$  of the PMOS device can be effectively reduced, which increases the available energy transfer time to the output load. In addition, a switch can be added in between  $V_N$  and  $V_P$  inputs of a piezoelectric transducer to reduce the wasted charges which is used to charge or to discharge the parasitic capacitance of a piezoelectric device. Figure 4 shows the circuit diagram of the proposed circuit as well as the system reported in [1,3,8].

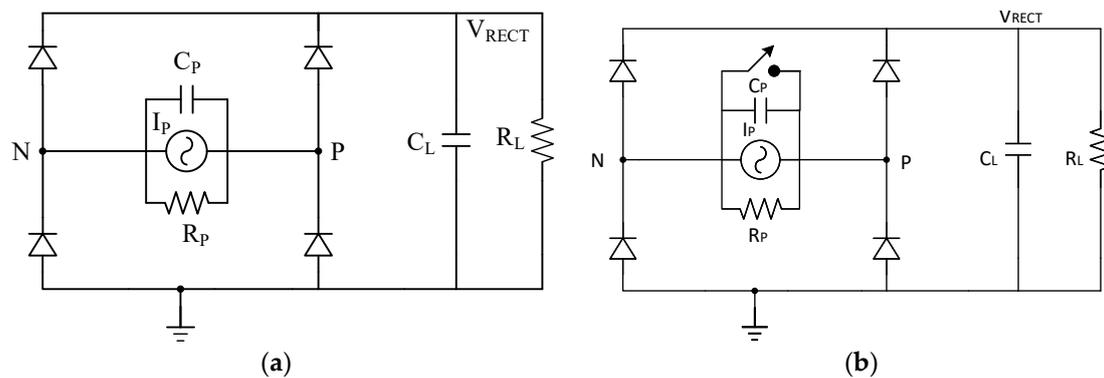


Figure 3. Circuit schematics of: (a) a full-wave rectifier, (b) a conventional diode full-bridge rectifier.

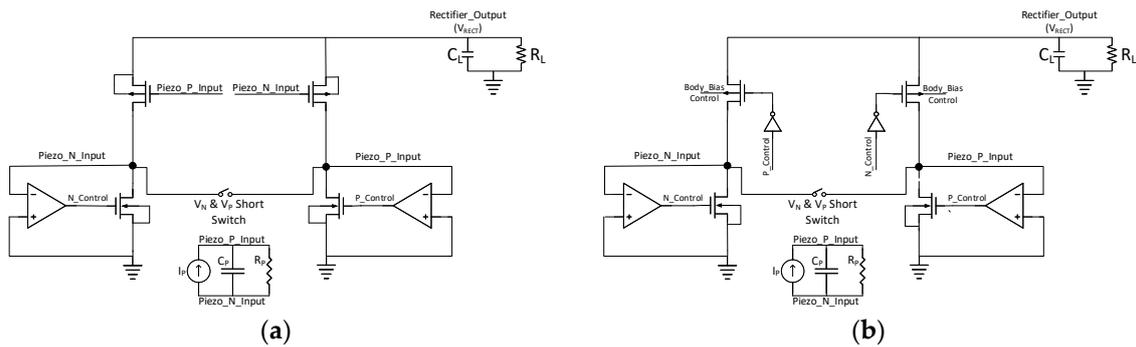


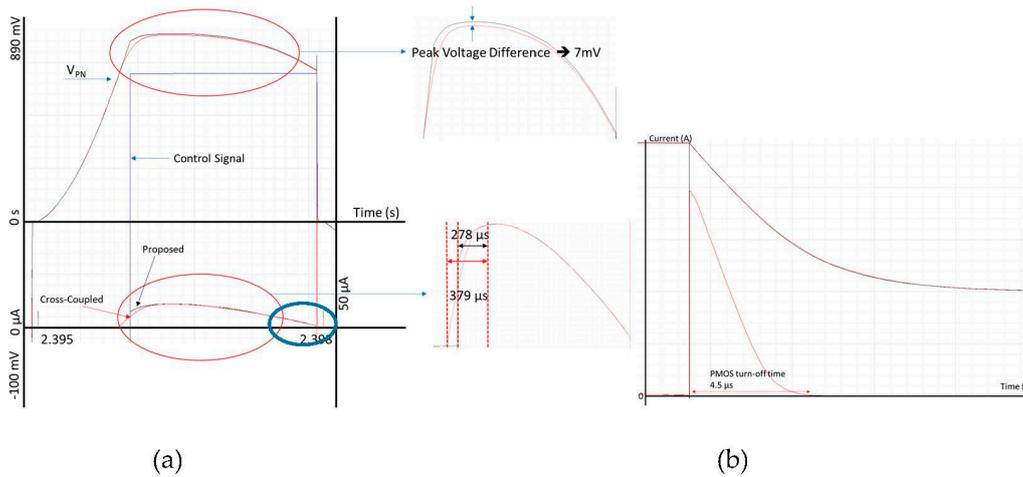
Figure 4. (a) Full-wave rectifier circuits presented in [1,3,8] and (b) the proposed architecture.

### 3.2. Proposed Active Full-Wave Rectifier

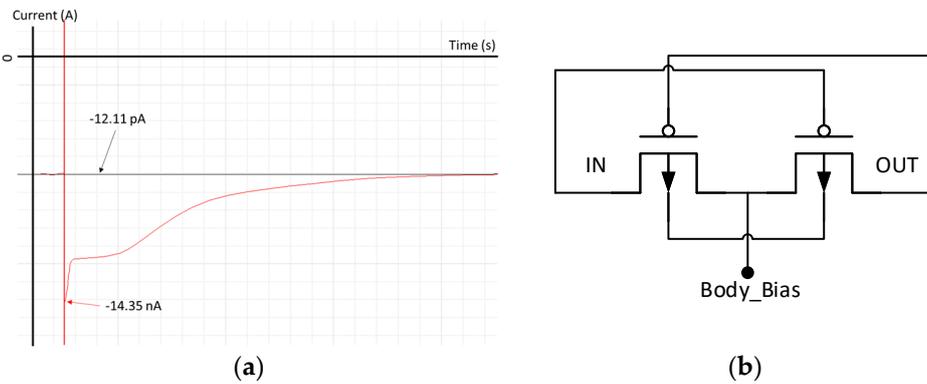
Figure 4a shows the full-wave rectifier structure reported in [1,3,8]. Due to the cross-coupled nature of the circuit, it requires a current and time to charge and discharge  $C_{sg}$  of the PMOS switch charged by a piezoelectric transducer directly prior to being turned on and off. Therefore, to turn on the PMOS switch in order to charge  $C_{sg}$  the input voltage from a piezoelectric transducer,  $V_{PN}$  should be greater than  $|V_{thp}|$ . Therefore, the available transfer time of energy from a piezoelectric transducer will be reduced because of the time required to charge  $C_{sg}$ .

However, in the proposed active rectifier circuit as shown in Figure 4b, the PMOS on/off are controlled by the NMOS turning on/off signal and are driven by output voltage powered buffer. Therefore, the proposed system does not pose problems associated with the design reported in [1,3,8]. As shown in Figure 5, the time required to charge  $C_{sg}$  is about 100  $\mu$ s (about 39% less time to reach the peak current from a piezoelectric transducer) less than cross-coupled system presented in [1,2,8]. The PMOS off-time also has been reduced as shown in Figure 5b. The proposed system instantly discharges  $C_{sg}$ , and as a result, the off time is in the nano-second range even though the off-time of the cross-coupled system is 4.5  $\mu$ s. Therefore, more energy from a piezoelectric transducer can be transferred to the output resulting in the  $V_{PN}$  voltage ( $[V_P - V_N]$  of a piezoelectric input voltage) being about 0.7% higher than that of a cross-coupled based active rectifier with the same load and piezo input. Although 0.7% can be considered as a small improvement in a system, for low input power systems such as the one proposed in this paper, every available energy should be squeezed so that more available energy can be transferred to the output. In addition, if the excitation frequency as well the force applied to a piezoelectric transducer are lowered, then, charging time will be increased because of less available charges from a piezoelectric transducer. As a result, the voltage amplitude of  $V_{PN}$  will be lowered so as  $V_{RECT}$ . In addition, since the proposed energy harvesting system can handle more energy than a cross-coupled rectifier, the output voltage,  $V_{RECT}$ , is higher than that of the cross-coupled circuit. Figure 6a,b show the body leakage current and the body bias control circuit utilizing the leakage current, respectively. With the help of simple implementation of body-bias control circuit, the proposed system can achieve lower body leakage current compared with cross-coupled system reported in [1,3,8].

Figure 6 shows the body leakage current of the circuit that has been used to control the body bias. In Figure 6b,  $I_N$  is connected to the  $V_{RECT}$ ,  $I_P$  is connected either  $V_P$  or  $V_N$ , and the body-bias port is connected to the body of the PMOS switch. As shown in Figure 6a, the leakage current in the proposed system is  $-12.11$  pA (black line) while the leakage current in cross-coupled system is  $-14.35$  nA (red line), which is a huge improvement. With the help of all the above improvements, the output voltage from a proposed active rectifier is 698 mV while that of the rectifier with cross-coupled based is 694 mV.

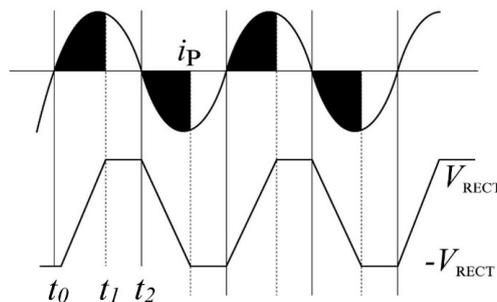


**Figure 5.** Comparison between cross-coupled full-wave rectifier circuit reported in [1,3,8] and the proposed architecture (Simulated): (a) on-time; (b) off-time of PMOS (blue circle magnified).



**Figure 6.** (a) Body bias circuit of the PMOS switch based active rectifier circuit, (b) simulated body leakage current of the body bias circuit of the PMOS switch.

The proposed switch-only active rectifier as well as the cross-coupled active rectifier with switch-only are simulated with the same MOSFET sizes as well as the same input piezo current. The only difference between the two schemes is the top PMOS gate control methods. Figure 7 shows the waveform of the piezoelectric transducer current,  $i_P$  versus  $V_{RECT}$  of a conventional full-wave rectifier. The shaded regions show the wasted energy due to charging and discharging of a parasitic capacitor,  $C_P$ .



**Figure 7.** Waveform of a piezoelectric transducer.

It is evident from the figure that a significant amount of energy is lost due to the charging and discharging actions of  $C_P$ . In Figure 7, the difference between  $t_0$  to  $t_1$  represents the wasted energy when  $i_p$  is used to charge  $C_P$ . The total charge available in full-bridge rectifier can be written as,

$$Q_{total/cycle} = \int_0^{2\pi/\omega_p} i_p dt = \frac{4I_p}{\omega_p} = 4C_P V_p \quad (1)$$

where  $V_p$  is the amplitude of the open circuit voltage of the piezoelectric transducer.

The piezoelectric transducer current,  $i_p$ , has to charge  $C_P$  from  $V_{RECT}$  to  $-V_{RECT}$  in every cycle before turning on a diode in a conventional full bridge diode. Therefore, charge lost in every cycle can be written as [8],

$$Q_{\frac{lost}{cycle}} = 2C_P(V_{RECT} - (-V_{RECT})) = 4C_P V_{RECT} \quad (2)$$

From Equations (1) and (2), the actual charge that used to charge  $C_L$  in Figure 3 can be written as [8],

$$Q_{\frac{RECT}{cycle}} = Q_{\frac{total}{cycle}} - Q_{\frac{lost}{cycle}} = 4C_P V_p - 4C_P V_{RECT} \quad (3)$$

Multiplying Equation (3) by the output voltage of the piezoelectric transducer,  $V_{RECT}$  provides the total energy delivered to  $C_L$ . Therefore, the total energy can be written as [8],

$$Energy_{\frac{RECT}{cycle}} = Q_{\frac{RECT}{cycle}} \times V_{RECT} = 4C_P V_{RECT} (V_p - V_{RECT}) \quad (4)$$

Since the piezoelectric transducer operates at a frequency,  $f_p$  the total power delivered to the output capacitor,  $C_L$  by the conventional full-bridge rectifier can be expressed as [8],

$$Power_{RECT} = Energy_{\frac{RECT}{cycle}} \times f_p = 4C_P V_{RECT} f_p (V_p - V_{RECT}) \quad (5)$$

Using Equation (5), the maximum available power is obtained when  $V_{RECT} = V_p/2$ , and can be expressed as

$$P_{RECT}(MAX) = C_P (V_p)^2 f_p \quad (6)$$

To reduce this unwanted energy loss or to increase the energy transfer from a piezoelectric transducer, one effective scheme involves inserting a switch in between the inputs of the piezoelectric transducer,  $V_P$  and  $V_N$  as shown in Figure 4.

Figure 8 shows the steady-state operation of the proposed full-wave rectifier. It can be seen from Figure 8 that the operation of the proposed full-wave rectifier can be divided into three phases. In phase 1 between  $t_0$  to  $t_1$ , a sinusoidal current,  $i_p$  from a piezoelectric transducer starts charging a parasitic capacitor,  $C_P$ . Unlike a conventional piezoelectric transducer as shown in Figure 3, time for charging of  $C_P$  has been reduced significantly because of the inclusion of a switch in between  $V_P$  and  $V_N$ . In Figure 9, it can be seen that as the one-shot turns on, the  $V_P$  and  $V_N$  terminals are shorted instantly and therefore it does not have to charge from its previous value, rather it starts from zero. In a conventional rectifier, when  $i_p$  is changing its polarity from positive to negative,  $C_P$  should be discharged from  $(V_{RECT} + 2V_d)$  to zero and charged from zero to  $-(V_{RECT} + 2V_d)$ . In phases 2 and 3, since the charging of a parasitic capacitor  $C_P$  has been completed, the energy can be transferred to the output capacitor,  $C_L$  through the full-wave rectifier.

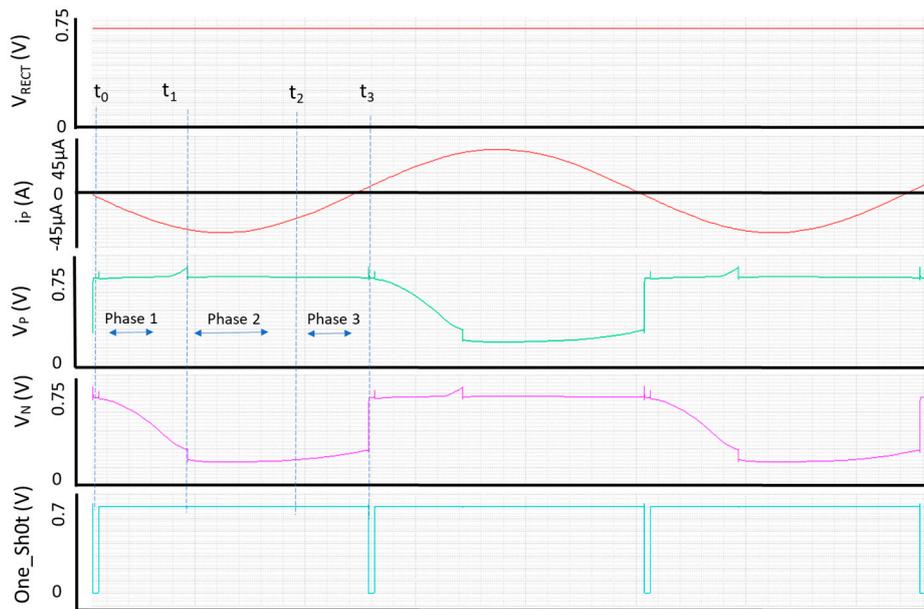


Figure 8. Simulated waveform of a piezoelectric transducer output.

Figure 9 shows the switch inserted in between  $V_P$  and  $V_N$  of a piezoelectric transducer which allows the capacitor to discharge to zero. The working principle for the one-shot signal switch is very simple.

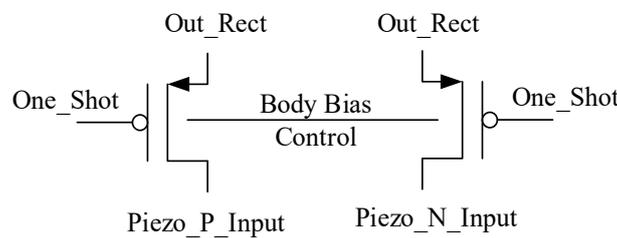


Figure 9. Schematic of the piezoelectric transducer switch.

Whenever a piezoelectric transducer crosses the zero point, the one-shot control circuit as shown in Figure 10 is designed to provide a short pulse which shorts the input ports of a piezoelectric transducer to reset the voltages  $V_P$  and  $V_N$ . This shorting action will help improve the efficiency of the piezoelectric energy harvesting circuit by reducing a waste charge. Therefore,  $i_p$  does not have to charge or discharge  $C_P$  from  $\pm(V_{RECT} + 2V_d)$  but rather from zero to  $(V_{RECT} + 2V_d)$ . The bottom two NMOS switches are controlled by a low-power comparator while the top two PMOS switches are controlled by  $P\_Control$  and  $N\_Control$  bar signals. All the control circuits as well as the comparator are powered by the harvested supply voltage,  $V_{RECT}$ .

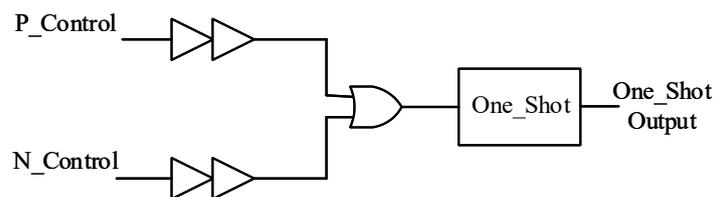


Figure 10. Schematic of the one-shot digital control circuit.

In the proposed full wave rectifier, the charge lost in every cycle can be denoted by [8],

$$Q_{lost/cycle} = 2C_P V_{RECT} \tag{7}$$

The charge available can be calculated as [8],

$$Q_{cycle}^{RECT} = Q_{cycle}^{total} - Q_{cycle}^{lost} = 4C_P V_{open} - 2C_P V_{RECT} \tag{8}$$

Therefore, the total power delivered to the output load  $C_L$  can be expressed as follow [8].

$$Power_{RECT} = Energy_{cycle}^{RECT} \times f_P = 2C_P V_{RECT} f_P (2V_{open} - V_{RECT}) \tag{9}$$

Comparison of Equations (3) and (8) reveals that the charge lost is reduced by about 50%. Therefore, inserting a switch in between  $V_P$  and  $V_N$  of a piezoelectric transducer can save a substantial amount of energy. All the control circuits in this proposed active rectifier are powered by the output voltage,  $V_{RECT}$  derived from the harvested energy. Figure 11 illustrates the start-up operation of the circuit. For the start-up of the rectifier operation, all the control circuits including the comparators are not working until  $C_L$  is charged properly since no charge is accumulated in  $C_L$  initially. As shown in Figure 11, leakage current flows through both PMOS( $M_P$ ) and NMOS( $M_N$ ) as the input of a piezoelectric transducer starts increasing thereby slowly charging  $C_L$ . The initial charging current derived from this leakage current is in nano-ampere range. The time required to charge  $C_L$  is approximately 120  $\mu$ s and the resulting harvested supply power all the control circuits including the comparators. Proper working of all control signal starts at around 180  $\mu$ s.  $Comp_P$  and  $Comp_N$  are the output waveform of comparators, and  $One-Shot$  is the output waveform of the One-Shot control signal.  $Comp_P$  and  $Comp_N$  are represent  $P\_Control$  and  $N\_Control$  signals in Figure 4b.



Figure 11. Simulated start-up of the proposed active rectifier.

#### 4. Measurement Results

Figures 12 and 13a show the measured waveforms of the proposed full-wave rectifier. For the sake of simplicity and to validate the operation of the proposed circuits, the input signal was generated by a function generator with  $V_{pk-pk}$  voltage of 1.2 V (600 mV amplitude). The output was measured to be 580 mV with load resistor of 45 k $\Omega$ . The measurement data is slightly different from a simulated one because of the parasitic PCB board capacitance as well as the chip-package parasitics. Figure 12c,d

show the test set-up. Since the proposed circuit is tested with a signal generator, the model used in this test set-up is the Norton to Thevenin equivalent of the circuit shown in Figure 13b.  $V_1$  represents the voltage signal from the signal generator with an amplitude of 0.6 V ( $V_{PK-PK}$  is 1.2 V),  $R_1$  is 13.3 k $\Omega$ , and  $C_p$  is a parasitic capacitance of a piezoelectric transducer.

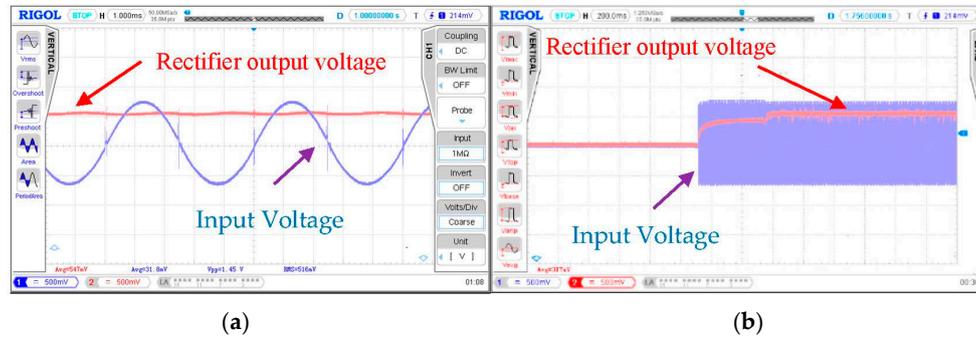


Figure 12. Measured input and output voltage waveforms of the rectifier (a) magnified; (b) full waveform.

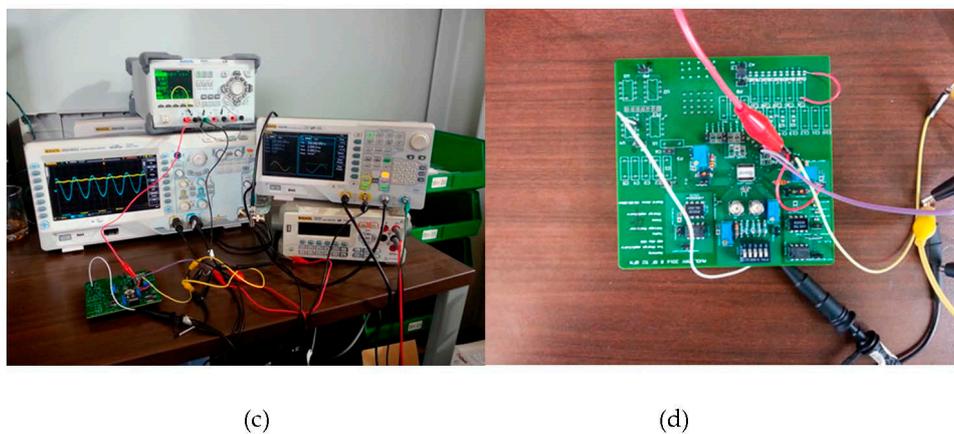
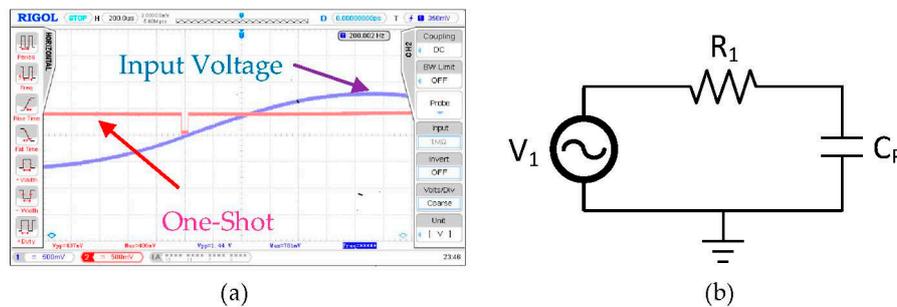


Figure 13. (a) One-shot and input voltage waveforms; (b) input equivalent circuit of a piezoelectric transducer; (c) test setup; and (d) printed circuit board (PCB) implementation of the test board.

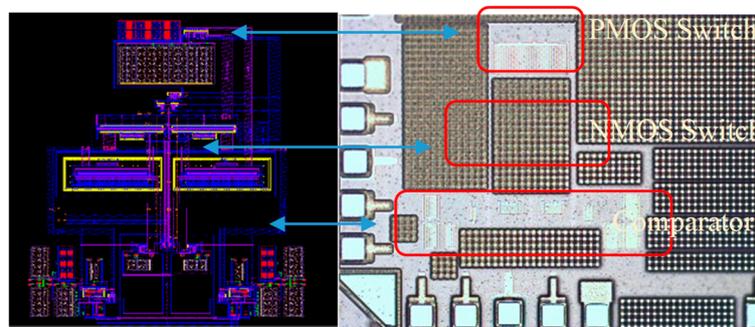
### 5. Conclusions

Figure 14 shows the layout of the proposed full-wave CMOS rectifier and the microphotograph of the fabricated IC and Table 1 shows the summary of the system performance. The amplitude of the output voltage is 0.694 V. The simulated conversion ratio of  $V_{OUT}$  versus  $V_{IN}$  is 98.7%. The output power,  $P_{OUT}$  of the proposed full-wave rectifier is 10.7  $\mu$ W, and the power conversion efficiency (PCE) of the system is 52.2%, and this PCE can be achieved at 45 K $\Omega$  (Max PCE). The main reason for the low PCE is due to the low available input power. The main idea of this proposed active rectifier is to reduce the off-chip components as much as possible so that this energy harvester can be easily integrated

with other complex systems. In addition, the performance of the proposed system demonstrates that by reducing the time for charging and discharging of  $C_{sg}$  of the PMOS switch, the input amplitude of a piezoelectric transducer will increase the output voltage. This process saves the wasted charges caused by  $C_p$ , and the output voltage can be increased even though the increment in the input voltage amplitude is small. As shown in Table 1, the PCE of the proposed circuit is comparable to other energy harvesting circuits reported in literature. Reference [8] used an external power source, which will decrease the harvested power. References [1,3] used high piezo current,  $i_p$  compared to this proposed design and high voltage amplitude to achieve higher output voltage. In addition, an inductor is used in reference [1] to further increase the PCE of the overall system. However, with such high piezoelectric current as well as with an additional inductor with a fairly big value, the PCE of their system is not far from the proposed simple but effectively controlled rectifier. The input of the proposed system was provided by a function generator instead of a piezoelectric transducer for proof of concept of the proposed rectifier circuit. The preliminary test results show that the overall system performs as expected. Figure 14 shows the proposed full-wave rectifier layout and full-chip micro-photograph.

**Table 1.** Performance Comparison.

Publications	[1]	[3]	SO [8]	This Work
Inductor and External Components	Yes	No	No	No
External Power	Yes	No	No	No
Amplitude of $I_p$ by PD or Applied force	2 mA	94 $\mu$ A	3.35 g	45 $\mu$ A
Parasitic Capacitance of PD (nF)	330	25	12	25
Vibration Frequency (Hz)	185	200	225	200
$V_{IN,Peak}$	3.5	3	2.4	0.704
$V_{OUT}$ (V)	3.34	2.9	2	0.694
$R_L$ (K $\Omega$ )	3.51	100	75	45
PCE (%)	160% higher than conventional rectifier. Converted PCE is 63%		53	52.2



**Figure 14.** Layout and chip microphotograph of the proposed full-wave rectifier (540  $\mu$ m  $\times$  540  $\mu$ m).

**Acknowledgments:** The chip has been manufactured through the MOSIS education support.

**Author Contributions:** Taeho Oh designed and tested the proposed novel works. Thanks to Syed K. Islam, Mohamad Mahfouz and Gary To for their support of the test equipment as well as valuable advice for the work.

**Conflicts of Interest:** The authors declare no conflict of interest.

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