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Review

Ultralow-Power SOTB CMOS Technology Operating Down to 0.4 V †

Nobuyuki Sugii [1,*], Yoshiki Yamamoto [1], Hideki Makiyama [1], Tomohiro Yamashita [1], Hidekazu Oda [1], Shiro Kamohara [1], Yasuo Yamaguchi [1], Koichiro Ishibashi [2], Tomoko Mizutani [3] and Toshiro Hiramoto [3]

[1] Low-Power Electronics Association & Project, Tsukuba, Ibaraki 305-8569, Japan; E-Mails: yoshiki.yamamoto.pc@renesas.com (Yo.Ya.); hideki.makiyama.wx@renesas.com (H.M.); tomohiro.yamashita.ue@renesas.com (T.Y.); hidekazu.oda.yf@renesas.com (H.O.); shiro.kamohara.uh@renesas.com (S.K.); yasuo.yamaguchi.uf@renesas.com (Ya.Ya.)

[2] Department of Engineering Science, Graduate School of Informatics and Engineering Departments, The University of Electro-Communications, Chofu, Tokyo 182-8585, Japan; E-Mail: ishibashi@ee.uec.ac.jp

[3] Institute of Industrial Science, The University of Tokyo, Meguro, Tokyo 153-8505, Japan; E-Mails: mizutani@nano.iis.u-tokyo.ac.jp (T.M.); hiramoto@nano.iis.u-tokyo.ac.jp (T.H.)

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* Author to whom correspondence should be addressed; E-Mail: n-sugii@ieee.org; Tel.: +81-29-879-8265; Fax: +81-29-856-2622.

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Abstract: Ultralow-voltage (ULV) CMOS will be a core building block of highly energy efficient electronics. Although the operation at the minimum energy point (MEP) is effective for ULP CMOS circuits, its slow operation speed often means that it is not used in many applications. The silicon-on-thin-buried-oxide (SOTB) CMOS is a strong candidate for the ultralow-power (ULP) electronics because of its small variability and back-bias control. Proper power and performance optimization with adaptive V_{th} control

taking advantage of SOTB's features can achieve the ULP operation with acceptably high speed and low leakage. This paper describes our results on the ULV operation of logic circuits (CPU, SRAM, ring oscillator and other logic circuits) and shows that the operation speed is now sufficiently high for many ULP applications. The "Perpetuum-Mobile" micro-controllers operating down to 0.4 V or lower are expected to be implemented in a huge number of electronic devices in the internet-of-things (IoT) era.

Keywords: ultralow power; ultralow voltage; CMOS; minimum energy point; variability; back bias; FDSOI; silicon-on-thin-buried-oxide (SOTB); thin BOX

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1. Introduction: Issues for ULV Operation Possibly Staying on MEP Point

A huge number of small electronic devices composing big data are expected to be used across the globe as the "internet of things" (IoT). The CMOS integrated circuit is a core part of these devices. The energy efficiency of the CMOS circuits should therefore be greatly improved. It is well known that the operating voltage (V_{dd}) is a primarily important parameter for reducing the energy per operation cycle in the CMOS circuits. As shown in Figure 1, the energy is a sum of active (E_{ac}) and leakage (E_{leak}) energy as shown in Equation (1) in the simplified form.

$$E = E_{ac} + E_{leak} = C_{load}V_{dd}^2 + I_{leak}V_{dd}/af \quad (1)$$

where C_{load}, I_{leak}, a, and f denote load capacitance, leakage current, activity, and frequency, respectively. With decreasing V_{dd}, E_{ac} decreases since it is proportional to $C_{load}V_{dd}^2$. However, E_{leak} relatively increases as f decreases with decreasing V_{dd}. These two terms determine the minimum energy point (MEP). The energy efficiency of CMOS circuits has been greatly improved by the miniaturization of CMOS transistors. This improvement is mainly accomplished by E_{ac} reduction due to C_{load} reduction with the transistor scaling. However, most of the circuits do not operate at MEP and the improvement in terms of the efficiency has not been perfect so far. In recent generations, the scaling has increased the V_{dd} at MEP, as shown in Figure 2 [1,2]. This is because E_{leak} tends to increase with the miniaturization that has been seen in recent generations, especially for the performance-oriented applications. In the energy-efficiency conscious design like [1], the E_{min} has already an increasing trend (minimum point of E_{min} at 90-nm node), as shown in Figure 2.

The near- or sub-V_{th} operation is attractive to improve the energy efficiency. The operating speed of these circuits, however, is not high. The maximum frequency rapidly drops with decreasing V_{dd} in the conventional CMOS [3]. In the device design for ULP circuits, it is important to optimize both V_{dd} and V_{th}. With decreasing V_{dd}, V_{th} should increase to minimize the energy [4]. This drastically decreases the frequency and in many cases the MEP operation is a sub-V_{th} operation and its frequency is less than MHz. The variable V_{th} approach with adaptive back-bias control can mitigate the situation: optimizing frequency and decreasing energy as low as possible down to the MEP value. Both V_{dd} and V_{th} are controlled to minimize the energy, while satisfying the required workload: required frequency. In the dynamic voltage and frequency scaling (DVFS), only V_{dd} is controlled. In order to achieve higher energy efficiency, the control of V_{th} should be accompanied.

Figure 1. Schematic relationship between energy per operation E *versus* operating voltage V_{dd}.

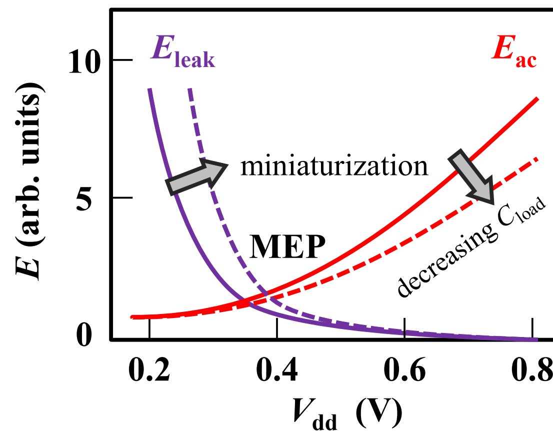
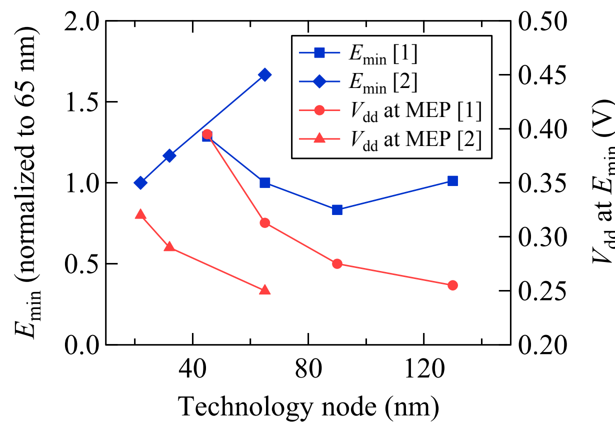


Figure 2. Minimum energy E_{min} and V_{dd} at MEP as a function of technology node number after [1,2].



It is well known that the characteristic variability of transistors is recognized as a major obstacle for the performance/power tradeoff, especially at low V_{dd}. The increasing variability also increases V_{dd} at MEP [5] simply because of the increase in leakage current in a circuit that is a sum of transistor leakages [6]. Moreover, increasing the transistor variation causes delay variation, especially at low V_{dd} and causes a significant performance drop [7]. Design to cope with the increasing variability at low V_{dd} becomes more complex. The variability tolerant design prefers to increase the transistor width W; however, this directly increases the power [8,9]. Another variability tolerant logic design prefers a smaller number of pipeline stages and longer logic depth. However, these design strategies decrease the frequency [10,11] and increase E_{min}.

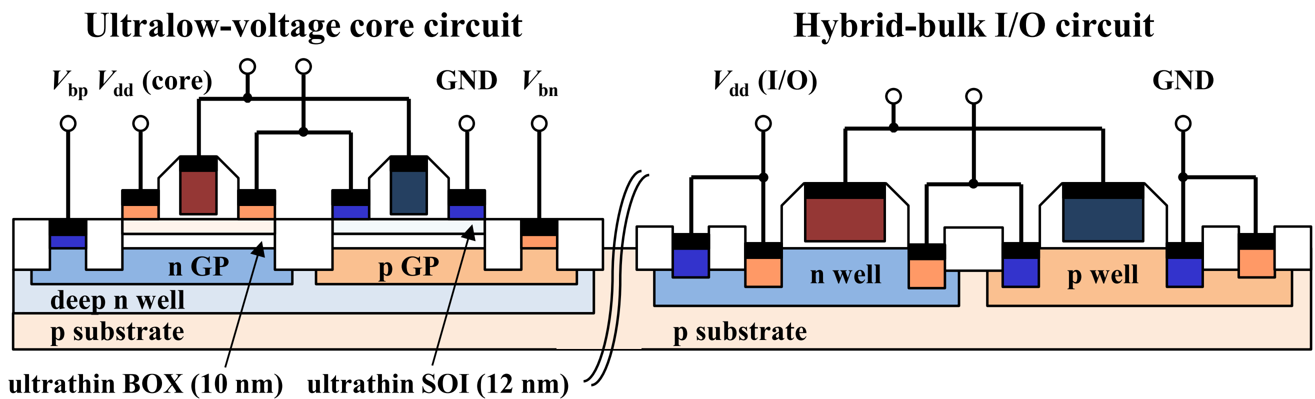
We hypothesize the main issues for the highly energy efficient CMOS circuits are adaptive V_{th} control and small variability, as described in this section. In order to solve these issues, we are developing the silicon on thin buried oxide (SOTB) [12–16]. In this article, we show SOTB's low voltage capability, including small variability and back-bias control through device and circuit results.

2. SOTB Device Technology

Schematic cross section of the SOTB is shown in Figure 3. There are four major factors: (i) small local variability due to low-impurity fully depleted SOI channel; (ii) high back-bias coefficient due to

thin BOX layer and doped ground plane (n GP and p GP) just below the BOX layer; (iii) flexible V_{th} tuning by impurity density control of the ground plane and (iv) high design compatibility with the conventional CMOS due to mostly identical planar layout to the bulk and a hybrid bulk integration for I/O. Details of the SOTB fabrication process are reported elsewhere [15,16].

Figure 3. Schematic cross section of silicon on thin buried oxide (SOTB) and hybrid bulk transistors. V_{bp} and V_{bn} denote back-bias terminal for p- and n-type SOTB, respectively.



V_{th} control optimized for the ULV operation has been an important process issue. In this optimization, we controlled the V_{th} values at around 0.2 V, which is by about 0.2 V lower than that for the low-standby-power (LSTP) application, with the multiple V_{th} option utilizing a poly-silicon and high-k gate-stack technology and a proper doping profile control of the ground plane [15]. As shown in Figure 4, we utilize a small amount of high-k (Hf and Al) oxide mixed with the conventional SiON gate dielectric and control proper effective work function (EWF) both for NMOS and PMOS. Typical I_d-V_g characteristics of triple V_{th} option are shown in Figure 5. LVT, SVT, and HVT denote low, standard, and high V_{th} option, respectively. Two-orders-of-magnitude off-leakage-current variation can be done only by changing the doping density below the BOX layer with the same gate stack.

Figure 4. Effective work function (EWF) control with high-k/SiON gate stack [15]. Circles and diamonds represent EMF of P-type and N-type gate stacks for PMOS and NMOS, respectively.

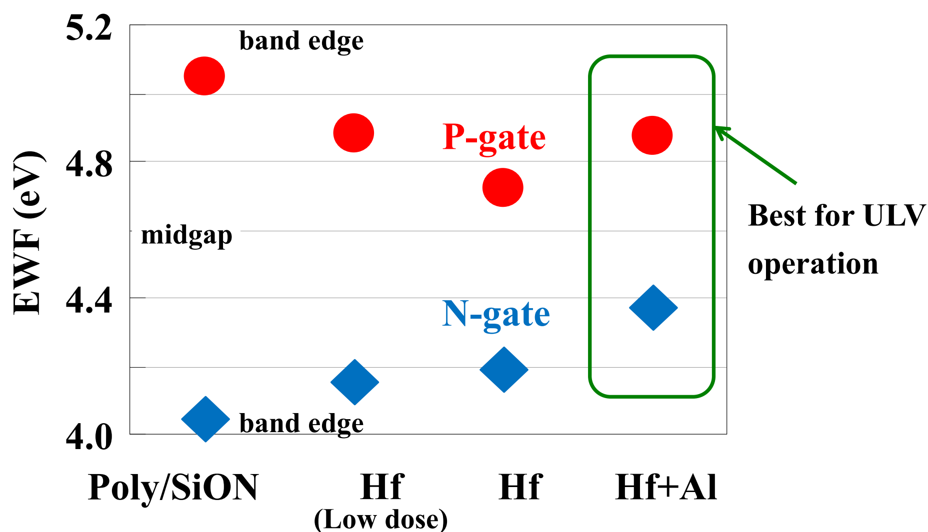
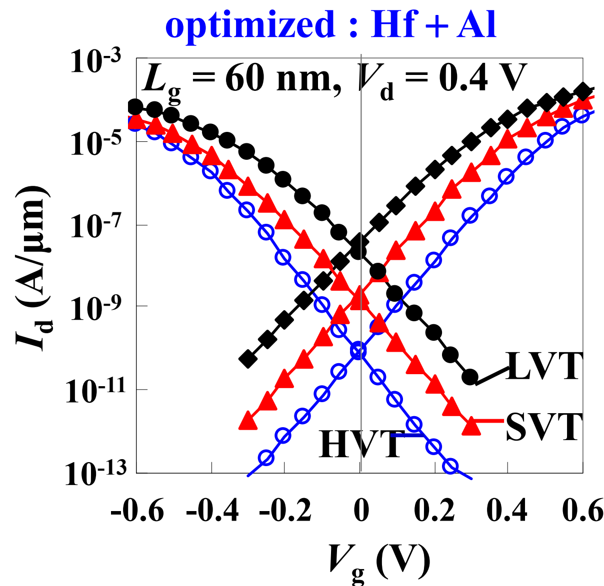


Figure 5. I_d-V_g characteristics of triple V_{th} option controlled by ground plane doping [15].



We have demonstrated significant reduction of the V_{th} variability. The Pelgrom coefficient (A_{VT}) of the SOTB was about 1.2–1.3 mVμm [16], which is less than half of the bulk. Moreover, we measured the V_{th} variation of one-million transistors (gate length and width: 0.06 and 0.14 μm, respectively) [16] as shown in Figure 6 and confirmed regular distribution without dropout transistors. Variation of on-state current I_{on} is important and must be decreased since this directly affects the delay variation of circuits. The I_{on} variation was demonstrated to be less than half of bulk [17] and we confirmed a significant reduction of the I_{on} variability for one-million transistors as shown in Figure 7 [16]. The lowest V_{th} values of SOTB and bulk are the same as shown in Figure 6. This means the highest leakage current among one-million transistors is the same. Besides, the highest V_{th} transistor determines the delay. As shown in Figure 7, the smallest I_{on} value for SOTB is about twice as high as the bulk's worst value. This is a strong advantage of SOTB's small variability in terms of the circuit performance.

Figure 6. V_{th} distribution of 1 M transistors. [16] Vertical-axis value shows deviation from V_{th} median value. Positive or negative σ values indicate that the corresponding V_{th} value is upper or below median, respectively.

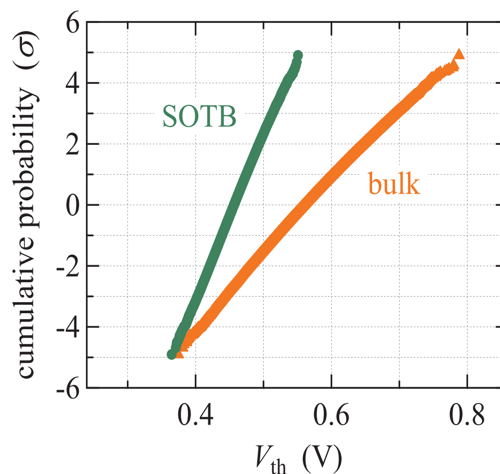
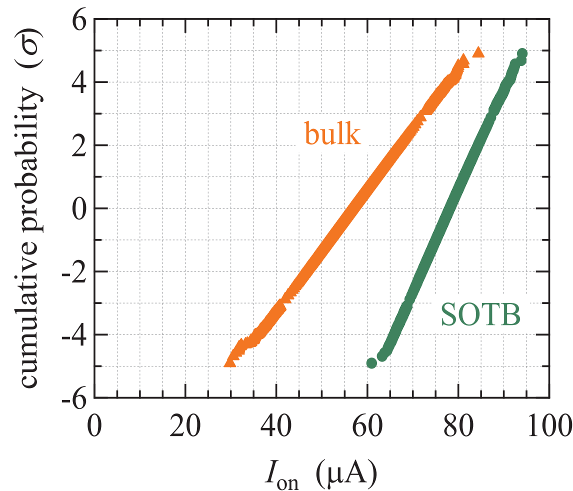


Figure 7. I_{on} distribution of 1 M transistors [16].



3. ULV Operation of SOTB Circuits

3.1. V_{min} Reduction of 6T-SRAM and Leakage Control by Back-Bias

Thanks to the significant reduction of the variability, as shown in Figures 6 and 7, we successfully demonstrated 2-Mbit SRAM operation at V_{min} = 0.37 V [16] of the standard six-transistor (6T) layout and without assist circuits as shown in Figure 8. Due to the V_{th} optimization mentioned in the previous section, very small access time (5.5 ps at V_{dd} = 0.4 V) was demonstrated. This enables a circuit operation with SRAM at several tens of MHz. The standby leakage decreased more than two orders of magnitude by a reverse back biasing and achieved 1.2 pA/cell without destroying the data. Moreover, the above V_{min} value can be kept at lower at elevated temperatures with a proper back-bias control. In Figure 9, the V_{min} value at room temperature was the same as the value shown in Figure 8. At 80 °C, the V_{min} value increased to 0.46 V. This is because the V_{th} values of NMOS and PMOS transistors differently shifted from the room-temperature values. Although these V_{th} values were smaller than the room-temperature values (this increased the leakage current about two orders of magnitude higher than that at room temperature), balance of V_{th}s (current drivabilities) between the NMOS and PMOS transistors untuned. This deteriorated the SRAM cell stability and increased the V_{min}. By applying proper back-bias voltages for both transistors, the V_{min} value again reduced to less than 0.4 V as shown in Figure 9. Leakage current also can be minimized by the back-bias control regardless of temperature, which is roughly the same as the room-temperature value.

3.2. Ring Oscillator Circuit Results

We have developed a standard logic cell library of the SOTB technology with a hybrid bulk I/O library. The delay characteristics of the cells were evaluated through the RO measurements [18]. Figure 10 shows propagation delay t_{pd} of a 101-stage inverter RO for SOTB and bulk. The delay of SOTB was by 42% smaller than bulk at V_{dd} = 0.4 V. Note that V_{th}s of SOTB and bulk were the same at V_{dd} = 0.4 V. The speed gain of SOTB was higher at lower V_{dd} because of better I_{eff}/I_{off} and smaller DIBL. The delay variability was then investigated. The standard deviation of t_{pd} for SOTB exhibited a

very weak $1/\sqrt{N}$ dependence. The result means that the local delay variability of SOTB is very small. We also succeeded in the significant reduction of die-to-die delay variability by a proper back-biasing [19]. The logic circuits contain various types of logic cells such as inverter, NAND, NOR, *etc.* We found that back-biasing considering a drivability balance of NMOS and PMOS transistors is essential for an effective suppression of die-to-die delay variability for various types of the cells.

Figure 8. Fail-bit count of 2-M bit SRAM array as a function of V_{dd} [16].

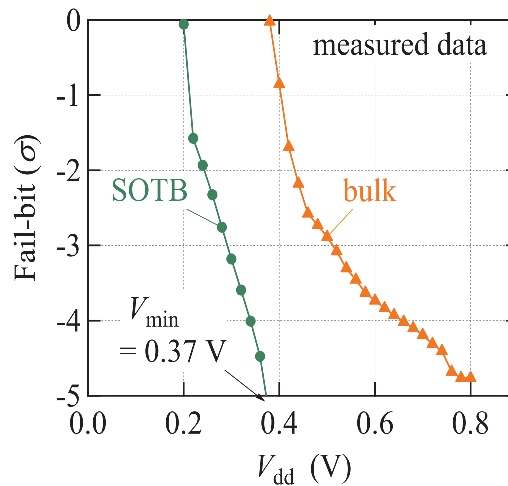
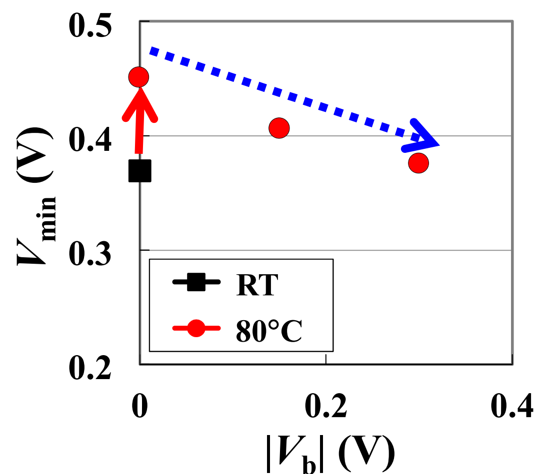
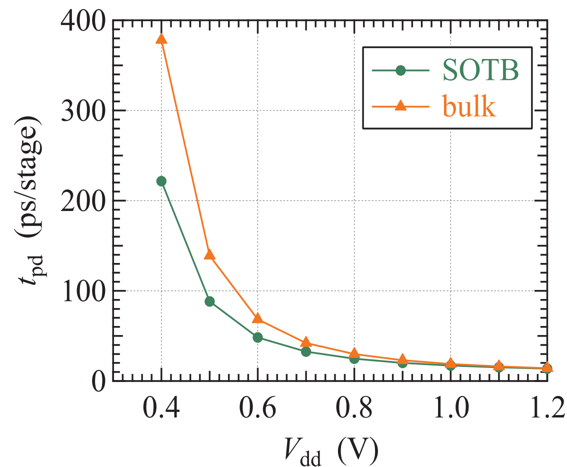


Figure 9. V_{min} of 2-M bit SRAM array as a function of back-bias voltage $|V_b|$: absolute values of back-bias voltage for NMOS and PMOS, $|V_b| = |V_{bn}| = |V_{bp}|$.



The minimum energy consumption of SOTB logic circuits of 50 kgates was estimated based on the RO results by optimizing the back-bias voltage [20]. At the same energy per operation, SOTB operates about ×10 higher than bulk. The power consumption of 44 µW at 10 MHz (4.4 pJ/cycle) is expected at V_{dd} = 0.33 V whereas bulk operates at 1 MHz with the same energy per cycle as SOTB.

Figure 10. Inverter delay t_{pd} as a function of V_{dd} [18].



3.3. Demonstration of ULV and ULP Operation of Logic Circuits

The design flow for the SOTB integrated circuits is basically the same as the conventional one. Using our newly developed design flow with the SOTB/bulk hybrid library, several ULV circuits were designed. Significant power reduction was demonstrated by the post-layout timing and power analysis. The reconfigurable accelerator named cool mega array (CMA) was designed and silicon results were obtained [21]. The bulk CMA operates at 0.8–1.2 V (with dynamic voltage scaling) and 210 MHz, and the SOTB version operates at 0.4 V (with back-biasing) and 65 MHz. The energy efficiency executing the Alpha blender test program was 38 and 65 MOPS/mW for bulk and SOTB, respectively.

The back-bias control offers a strong advantage for the FPGA circuits. The flex-power FPGA of the SOTB version was firstly implemented and silicon results were obtained [22]. After the FPGA configuration, the back-bias control enables that the only critical-path logic elements are set to low V_{th}. This significantly reduces the leakage power with no operation speed penalty.

High-efficiency generator of back-bias voltage is important for the SOTB technology since standby leakage current is kept low by applying reverse back-bias voltage. A superior point of the SOTB technology is that current load of the back-bias generator is very small because back-gate region of the SOTB transistor is electrically isolated by the BOX layer. This leads to a significant reduction of current consumption of the back-bias generator itself. We designed the generator circuit using the standard Dickson's charge pump for the SOTB and bulk hybrid platform and silicon results were obtained [23]. The generator operates at V_{dd} = 0.1 V and higher, and generates sufficient back-bias voltages for NMOS and PMOS of 0.85 and −1.5 V, respectively, at V_{dd} = 0.4 V with a current consumption of only 13 μA. By applying these back-bias voltages, leakage current of a 500 kgate logic circuit reduced to 2 μA corresponding to 4 pA/gate. There are still several points of the optimization and the generator current consumption is still higher than our target specification. The optimization is now under way.

We have confirmed a successful operation [24] of the proto-type ULV micro-controller chip as shown in Figure 11. This chip is composed of 32-bit RISC CPU with five-stage pipeline, 144 kByte SRAM, and interfaces (ROM, UART, SPI, and GP) and can be connected with sensors and rf modules

for the sensor-network node. The micro-controller chip operates at V_{dd} = 0.35 V and consumes only E = 13.4 pJ (f = 14 MHz) as shown in Figure 12. Note that the E values for SOTB and bulk at $V_{dd} \geq 0.8$ V are identical because it is determined by E_{ac} (same C_{load} of the same 65-nm technology) in this region. Sleep current is only 0.14 μA. By taking advantage of the ULP capability of our SOTB micro-controller chip, named "Perpetuum-Mobile", the sensor node is expected to operate with a sufficient frequency (>10 MHz) for a long period with a single battery or further longer operation with an energy harvester.

Figure 11. Block diagram of "Perpetuum-Mobile" micro-controller chip for a sensor-node application. (PLL: phase locked loop; ADC: analog to digital converter; SPI: serial peripheral interface; UART: universal asynchronous receiver transmitter; GP: general purpose).

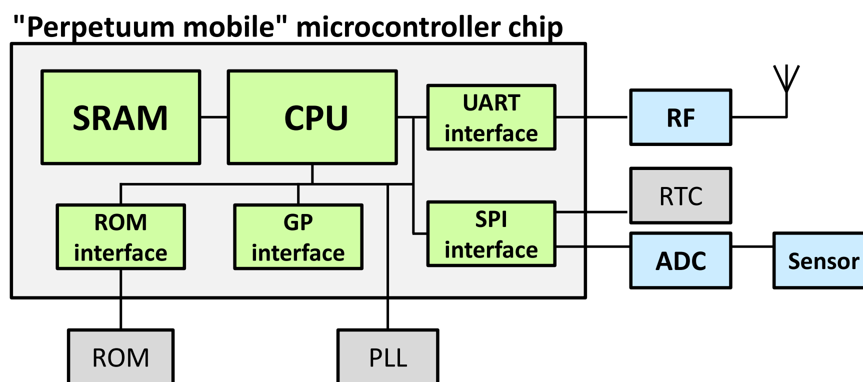
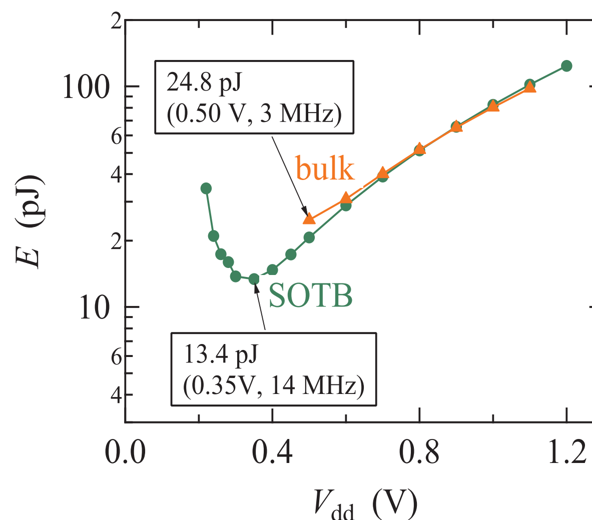


Figure 12. Energy per cycle E as a function of operating voltage V_{dd} for the "Perpetuum-Mobile" micro-controller chip [24].



4. Conclusions

Silicon on thin buried oxide (SOTB) is suitable for the ULV operation thanks to its small variability and back-gate bias controllability. We have demonstrated significant variability reduction, 0.4-V operation of SRAM, and reducing power consumption of logic circuits including a micro-controller

chip with a significant speed gain even at ULV. Many ULP applications are expected with SOTB chips. The "Perpetuum-Mobile" micro-controller chips will work as a core electronics parts in various types of electronic apparatuses of the "internet of things".

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Author Contributions

Nobuyuki Sugii coordinated and discussed the overall research and prepared the manuscript. Yoshiki Yamamoto and Hideki Makiyama designed the wafer fabrication process, prepared the device wafer, and measured their electrical characteristics. Tomohiro Yamashita, Hidekazu Oda, and Yasuo Yamaguchi designed the fabrication process and discussed the electrical characteristics. Shiro Kamohara and Koichiro Ishibashi designed and characterized the test chips. Tomoko Mizutani and Toshiro Hiramoto measured the electrical characteristics of the device wafers and discussed the results.

Conflicts of Interest

The authors declare no conflict of interest.

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