

Article

## Mechanisms of Low-Energy Operation of XCT-SOI CMOS Devices—Prospect of Sub-20-nm Regime

Yasuhisa Omura <sup>1,2,\*</sup> and Daiki Sato <sup>2</sup>

<sup>1</sup> Organization for Research and Development of Innovative Science and Technology (ORDIST), Kansai University, Yamate-cho, Suita 564-8680, Japan

<sup>2</sup> Graduate School of Science and Engineering, Kansai University, Yamate-cho, Suita 564-8680, Japan; E-Mail: k561544@kansai-u.ac.jp

\* Author to whom correspondence should be addressed; E-Mail: omuray@kansai-u.ac.jp; Tel.: +81-6-6368-1121; Fax: +81-6-6388-8843.

Received: 30 September 2013; in revised form: 18 December 2013 / Accepted: 3 January 2014 / Published: 10 January 2014

---

**Abstract:** This paper describes the performance prospect of scaled cross-current tetrode (XCT) CMOS devices and demonstrates the outstanding low-energy aspects of sub-30-nm-long gate XCT-SOI CMOS by analyzing device operations. The energy efficiency improvement of such scaled XCT CMOS circuits (two orders higher) stems from the “*source potential floating effect*”, which offers the dynamic reduction of effective gate capacitance. It is expected that this feature will be very important in many medical implant applications that demand a long device lifetime without recharging the battery.

**Keywords:** XCT-SOI MOSFET; quasi-static body floating effect; source potential floating effect; low energy; medical applications

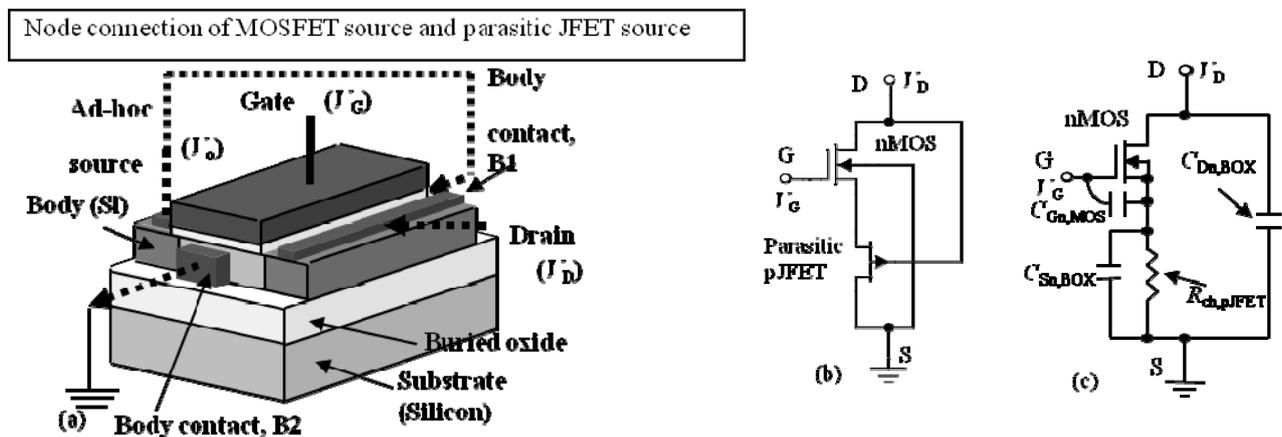
---

### 1. Introduction

Since the 1990s, various families of fully-depleted SOI MOSFET have been proposed and extensively studied [1,2] due to their various merits in terms of device scaling (high drivability, steep swing, less short-channel effects, smaller foot print, *etc.*). One of the authors (Omura) proposed the cross-current tetrode SOI MOSFET (XCT-SOI MOSFET) for analog applications (see Figure 1),

in 1986, on the basis of partially-depleted SOI MOSFET technology [3], and conducted experiments to evaluate the fundamental aspects of the device. While the scaling feasibility of XCT-like devices has been studied recently [4,5], we expect that XCT-SOI devices will yield new applications, such as medical implants, which demand low-energy operation with high noise margin. In order to discuss those applications in detail, device models have already been proposed to perform circuit simulations [6,7]. However, modeling an XCT-SOI device is not so easy due to the three-dimensionality of its operations [3,5]. Recently, our laboratory group examined the device model proposed in [6], and its usefulness was comprehensively revealed [8]. In addition, a mechanism analysis demonstrated the potential of scaled XCT CMOS devices for extremely-low-energy operation [9].

**Figure 1.** XCT-SOI MOSFET (bird’s eye view and equivalent circuit models): (a) Bird’s eye view of XCT-SOI device with parameter definitions and current flow. Broken arrows reveal the current flow; (b) Basic equivalent circuit model of n-XCT-SOI MOSFET [3]; and (c) AC circuit model of n-XCT-SOI MOSFET [9].



This paper considers the dynamic and standby power dissipation characteristics of the sub-30-nm-long gate XCT-SOI MOSFET. We start by analyzing the low-energy operation of XCT-SOI CMOS circuits; the model proposed here strongly suggests that the “*source potential floating effect (SPFE)*” substantially reduces the operation power consumption. The great advantages of the design methodology are also elucidated. In addition, this study addresses the reality of sub-20-nm-long gate XCT-SOI devices and a scaling scheme to suppress the standby power consumption for future low-energy applications.

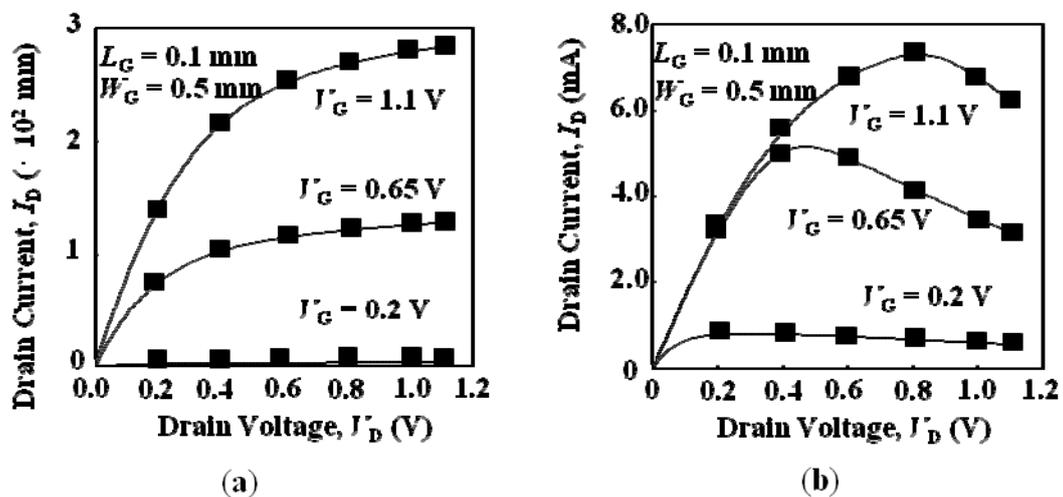
## 2. Device Structure and Assumptions for Modeling

The schematic device structure is shown in Figure 1a. In an n-channel XCT-SOI device, the n-channel SOI MOSFET and p-channel JFET are self-merged and the electron current of nMOSFET is relayed to the hole current of pJFET in series; the broken arrows reveal the current flow by the node connection of the MOSFET source and the JFET source.

As an example, we show the fundamental  $I_D$ - $V_D$  characteristics of a 0.1- $\mu\text{m}$ -long gate partially-depleted nMOSFET without the parasitic pJFET, see Figure 2a, following 3-D device simulations [10]. Device parameters are summarized in Table 1. As the XCT-SOI device has two active

body contacts (B1 and B2) of the SOI MOSFET, the conventional “quasi-static body-floating effect” [1] is eliminated automatically. Details of the device operation are described in a previous paper [8]. The nMOSFET shows slight short-channel effects due to channel length modulation. Figure 2b shows the  $I_D$ - $V_D$  characteristics of an n-channel XCT-SOI MOSFET as determined from 3-D device simulations. It is seen that the XCT-SOI device has lower  $I_D$  than the MOSFET because of the series resistance of the parasitic pJFET. In addition, the XCT-SOI device shows the negative-differential conductance (NDC) in the saturation region of drain current [3,6,7]. On the other hand, the short-channel effects (SCEs) of the original MOSFET are sufficiently suppressed in the XCT device [8]; subthreshold swing is 76 mV/dec at  $V_D = 1$  V. This is one of great advantages of XCT devices.

**Figure 2.** Simulated  $I_D$ - $V_D$  characteristics. (a) Original 0.1- $\mu$ m-gate SOI MOSFET without parasitic JFET; (b) nXCT-SOI MOSFET.



**Table 1.** Scaling scheme and device parameters for sub-100-nm-long gate XCT-SOI MOSFET.

Parameters	$N_A$ ( $\text{cm}^{-3}$ )	$L_G$ (nm)	$EOT$ (nm)	$t_{SOI}$ (nm)	$t_{BOX}$ (nm)	$V_D$ (V)	$V_{TH}^{(*)}$ (V)
Scaling scheme	$k^{4/3}$	$1/k$	$4/3k$	$1/k^{1/3}$	$1/k^{1/3}$	$1/k^{1/2}$	-
$L_G = 100$ nm	$2.0 \times 10^{18}$	100	2.0	129	111	1.00	0.20
$L_G = 75$ nm	$4.0 \times 10^{18}$	75	1.5	117	100	0.97	0.16
$L_G = 20$ nm	$2.3 \times 10^{19}$	20	0.4	75	65	0.50	-0.06
$L_G = 15$ nm	$3.4 \times 10^{19}$	15	0.3	69	59	0.43	-0.10

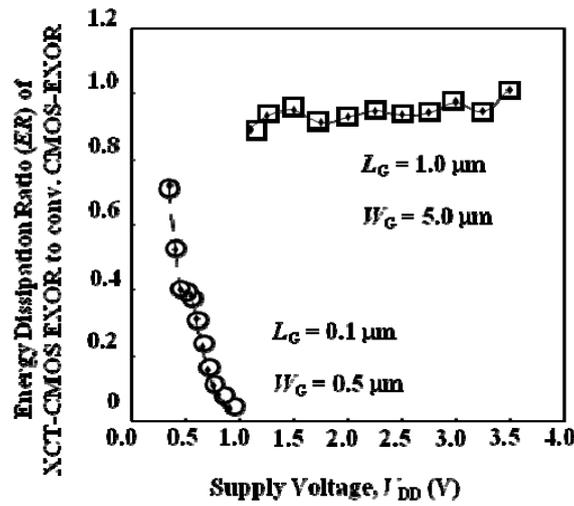
(\*)  $n^+$ -poly-Si gate is assumed.

In support of XCT-SOI MOSFET modeling, we have already proposed the equivalent circuit (for quasi-static analysis), shown in Figure 1b. The basic feasibility of this model has been examined by circuit simulations [5,7]. In addition, mechanisms of the low-energy operation were examined by a simplified analysis, based on the model shown in Figure 1c [9], where  $C_{Gn,MOS}$ ,  $C_{Sn,BOX}$ ,  $C_{Dn,BOX}$  and  $R_{ch,pJFET}$  denote the gate-to-source capacitance of SOI MOSFET, the source-to-substrate capacitance of SOI MOSFET, the drain-to-substrate capacitance of SOI MOSFET, and the source-to-drain resistance of the parasitic pJFET, respectively. In the case of p-channel XCT-SOI MOSFET, we label them as  $C_{Gp,MOS}$ ,  $C_{Sp,BOX}$ ,  $C_{Dp,BOX}$ , and  $R_{ch,nJFET}$ , respectively.

### 3. Circuit Simulation Results of SOI CMOS and XCT-SOI CMOS

Here, we advance the discussion to better understand XCT-CMOS EXOR circuit features. We assume the OR-NAND type EXOR circuit that consists of four CMOS inverters (standard layout). We concentrate the discussion on the energy ratio of CMOS-EXOR circuits, where energy ratio (*ER*) is defined as the energy dissipated by the XCT-CMOS EXOR over that of the comparable conventional SOI-CMOS EXOR. Calculation results, based on HSPICE [11] simulation results, are shown in Figure 3.

**Figure 3.** Simulation results of energy ratio (*ER*) of the energy dissipation of 1.0- $\mu\text{m}$ -long gate CMOS EXOR and 100-nm-long gate CMOS EXOR. The energy ratio is defined by the energy dissipated by the XCT-EXOR divided by that of the conventional CMOS EXOR.



First, it is seen that the *ER* value of 1- $\mu\text{m}$ -long gate devices is almost unity regardless of the  $V_{DD}$  value. This behavior is reasonable for the following reasons. The energy dissipation of conventional devices, evaluated by the  $P_d \cdot t_d$  product, is not a function of  $V_{DD}$  due to the simple recognition of the MOS gate capacitor's charging and discharging operations. It is anticipated that the XCT-CMOS, with a 1- $\mu\text{m}$ -long gate, follows this principle. In the case of 0.1- $\mu\text{m}$ -long gate devices, on the other hand, it is seen that the *ER* value rapidly falls as  $V_{DD}$  rises. As this is a very interesting result and somewhat mysterious, we discuss below a possible mechanism based on physics.

Frequency-dependent energy ratio (*ER*) is defined by [9]:

$$ER(\omega) = \frac{C_{Gn,XCT} + C_{Gp,XCT} + C_{Dn,BOX} + C_{Dp,BOX}}{C_{Gn,MOS} + C_{Gp,MOS} + C_{Dn,BOX} + C_{Dp,BOX}} \quad (1)$$

where  $C_{Gn,XCT}$  and  $C_{Gp,XCT}$  denote the effective gate capacitance of *n*-XCT-SOI MOSFET and *p*-XCT-SOI MOSFET, respectively. Here, for simplicity, we do not take account of the depletion layer beneath the buried oxide layer. These capacitances are calculated using the equivalent circuit model shown in Figure 1c as:

$$C_{Gn,XCT} = \frac{C_{Gn,MOS} (1 + \omega^2 C_{Sn,BOX}^2 R_{ch,nJFET}^2)}{1 + \omega^2 C_{Sn,BOX} R_{ch,nJFET}^2 (C_{Gn,MOS} + C_{Sn,BOX})} \quad (2a)$$

$$C_{Gp,XCT} = \frac{C_{Gp,MOS} (1 + \omega^2 C_{Sp,BOX}^2 R_{ch,pJFET}^2)}{1 + \omega^2 C_{Sp,BOX} R_{ch,pJFET}^2 (C_{Gp,MOS} + C_{Sp,BOX})} \quad (2b)$$

At the low-frequency limit ( $\omega \rightarrow 0$ ),  $C_{Gn,XCT}$  and  $C_{Gp,XCT}$  are reduced to  $C_{Gn,MOS}$  and  $C_{Gp,MOS}$ , respectively, as expected. At the high-frequency limit, however, we have:

$$C_{Gn,XCT} = \frac{C_{Gn,MOS} C_{Sn,BOX}}{C_{Gn,MOS} + C_{Sn,BOX}} \tag{3a}$$

$$C_{Gp,XCT} = \frac{C_{Gp,MOS} C_{Sp,BOX}}{C_{Gp,MOS} + C_{Sp,BOX}} \tag{3b}$$

Generally speaking, reducing the gate length ( $L_G$ ) raises the operation frequency at the same supply voltage. The  $ER$  rises when the scaling is enhanced; the scaling scheme assumed here [5,8] slightly reduces  $C_{Sn,BOX}R_{ch,pJFET}$  and  $C_{Sp,BOX}R_{ch,nJFET}$  as the scaling is advanced. For  $f < 1/(C_{Sn,BOX}R_{ch,pJFET})$  and  $f < 1/(C_{Sp,BOX}R_{ch,nJFET})$ , the roles of  $C_{Sn,BOX}$  and  $C_{Sp,BOX}$  are lost; *i.e.*, we have  $C_{Gn,XCT} \sim C_{Gn,MOS}$  and  $C_{Gp,XCT} \sim C_{Gp,MOS}$ . This is equivalent to the low-frequency limit. As a result, the  $ER$  value approaches unity; the intrinsic advantage of the XCT-SOI CMOS is lost. For  $f > 1/(C_{Sn,BOX}R_{ch,pJFET})$  and  $f > 1/(C_{Sp,BOX}R_{ch,nJFET})$ , on the other hand, we have  $C_{Gn,XCT} < C_{Gn,MOS}$  and  $C_{Gp,XCT} < C_{Gp,MOS}$ . Device operation approaches the high-frequency limit. In this case, the  $ER$  value decreases as the frequency rises. The  $ER$  value approaches zero as the supply voltage rises, shown in Figure 3. It is anticipated that the depletion layer beneath the buried oxide layer reduces the parasitic capacitance of source diffusion. In order to achieve a small  $ER$  value, therefore, we have to increase the effective channel resistance of the parasitic JFET when scaling is advanced.

Calculation results of the energy ratio ( $ER$ ), defined by Equations (1) and (2), are shown in Figure 4. The model clearly predicts that high-frequency drive will drastically reduce XCT-SOI CMOS power consumption. This stems from the “*source potential floating effect (SPFE)*” obtained by the model shown in Figure 1c. Consequently, we can conclude that the SPFE of the source diffusion of the SOI MOSFET plays an important role in reducing the energy dissipated by XCT-SOI CMOS devices.

**Figure 4.** Dissipated energy ratio as a function of the scaling factor. It is assumed that the energy dissipation consists only of the charging and discharging processes of the gate capacitor. Scaling scheme is described in [5]. The dotted arrows reveal the lowest-to-highest range of supply voltage applicable to 1- $\mu$ m-long gate CMOS (for  $k = 1$ ) and 0.1- $\mu$ m-long gate CMOS ( $k = 20$ ).

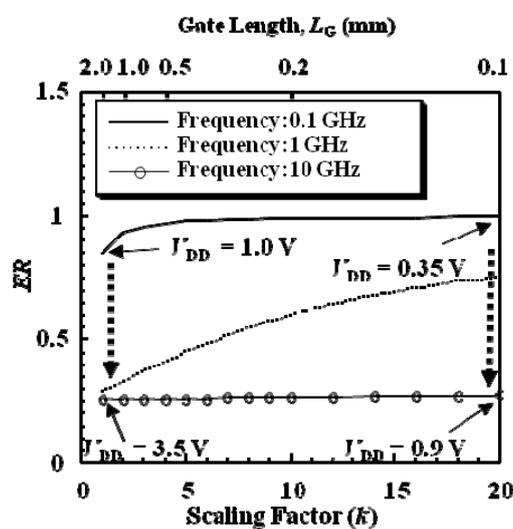
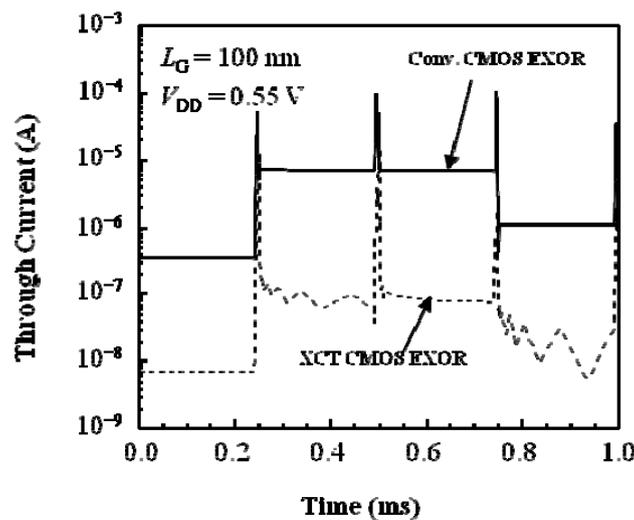


Figure 5 shows simulation results of the time-dependent through-current of the conventional SOI CMOS EXOR chain circuit and the XCT-SOI CMOS EXOR chain circuit, both under dynamic operation. It is seen that the standby power of the XCT-SOI CMOS EXOR chain circuit is about two orders lower than that of the conventional SOI CMOS EXOR chain circuit. This suggests that logic circuits composed of XCT-SOI CMOS can offer drastically lower standby-energy dissipation as well as lower switching-energy dissipation.

**Figure 5.** Simulation results of through-current of CMOS EXOR for  $L_G = 100$  nm. Arrows show standby power reduction.



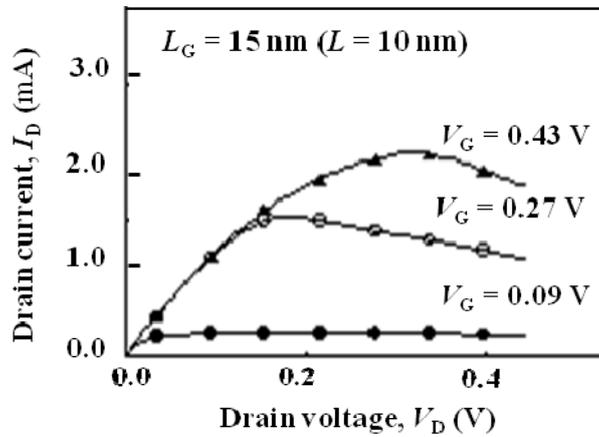
#### 4. Further Scaling Potential of XCT-SOI MOSFET

We now investigate the scaling potential of the XCT-SOI CMOS. The fundamental scaling scheme of the XCT-SOI MOSFET has been already studied in [5,8] and a 100-nm-long gate XCT-SOI CMOS has been realized. However, body doping is apt to rise to  $10^{19}$   $\text{cm}^{-3}$  as the XCT-SOI MOSFET is inherently a partially-depleted SOI device. We investigated how well the XCT-SOI MOSFET can be scaled down to realize a 15-nm-long gate. Using 3D device simulations [10], we simulated the performance of 20-nm-long gate and 15-nm-long gate XCT-SOI MOSFETs under the scaled bias condition, where we assumed abrupt source and drain junctions, for simplicity, in the scaling scheme proposed recently [12]. As the previous scheme [5,8] cannot be applied to the sub-100-nm regime, we restructured the scheme (see Table 1) so that devices work well [12].

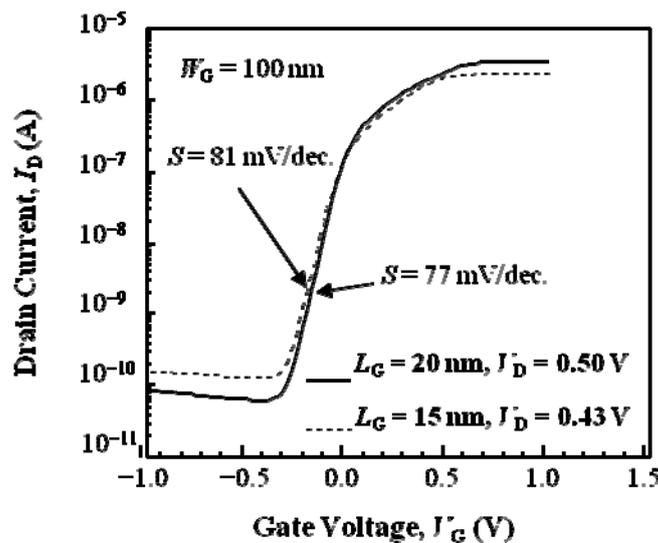
Here, simulated  $I_D$ - $V_D$  characteristics of the 15-nm-long gate XCT-SOI MOSFET, with device parameters, shown in Table 1, shown in Figure 6; the device has the abrupt source and drain junctions. The device shows the negative differential conductance in the saturation region, as is expected.

Simulated subthreshold characteristics of the 15-nm-long gate XCT-SOI MOSFET and the 20-nm-long gate XCT-SOIMOSFET are compared in Figure 7; both devices have the abrupt junctions. It is seen in Figure 7 that the subthreshold swing ( $S$ ) is 77 mV/dec, for the 20-nm-long gate device, and 81 mV/dec, for the 15-nm-long gate device. Short-channel effects are well suppressed. However, the gate-induced drain-leakage (GIDL) current level of the 15-nm-long gate XCT-SOI device is somewhat high ( $\sim 10^{-9}$  A/ $\mu\text{m}$ ) as the device simulation assumes the abrupt junction for simplicity.

**Figure 6.** Simulation results of  $I_D$ - $V_D$  characteristics of 15-nm-long gate XCT-SOI MOSFET.  $L$  denotes the effective channel length.

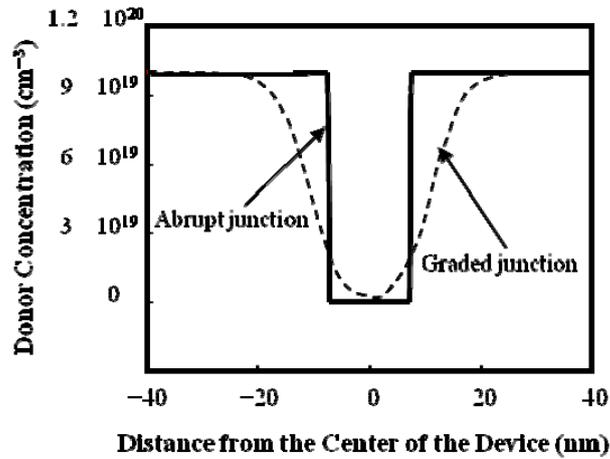


**Figure 7.** Simulation results of  $I_D$ - $V_G$  characteristics of 20-nm-long and 15-nm-long gate XCT-SOI MOSFET. It is assumed that the devices have abrupt source and drain junctions.

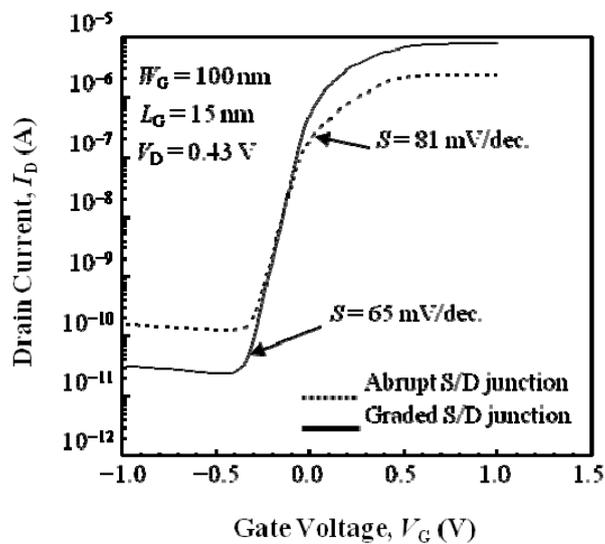


In response, we introduced a 10-nm-long graded doping region for source and drain junctions as a “new” scaling scheme, as shown in Figure 8. Simulated  $I_D$ - $V_G$  characteristics of the 15-nm-long gate XCT-SOI MOSFET are shown in Figure 9. Drain current characteristics of 15-nm-long gate XCT-SOI devices with the abrupt and the graded junctions are compared. It should be noted that the subthreshold swing is 65 mV/dec for the 15-nm-long gate device with the graded junction. Short-channel effects are well suppressed in the 15-nm-long gate XCT-SOI MOSFET. The GIDL current level is lowered to 200 pA/ $\mu$ m. The most noticeable result is the improved drivability of the device with the graded junction; this is due to the remarkable improvement in carrier velocity over the whole device region, as shown in Figure 10 [13], and the reduction of the channel resistance of the parasitic pJFET [12].

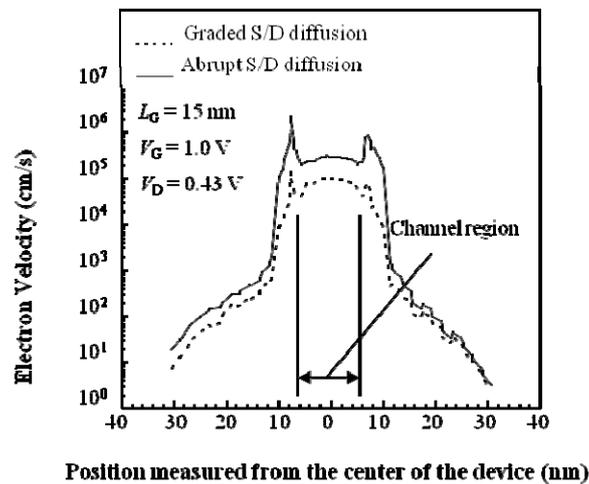
**Figure 8.** Doping profiles from the source to drain. The doping profile with a graded junction is compared to that with an abrupt junction.



**Figure 9.** Simulation results of  $I_D$ - $V_G$  characteristics of 15-nm-long gate XCT-SOI MOSFET. Impact of doping profile on  $I_D$ - $V_G$  characteristics is compared.



**Figure 10.** Simulation results of carrier velocity along the channel for the 15-nm-long gate XCT-SOI MOSFET. Impact of doping profile on velocity profile is compared.



**5. Performance Expected from the Scaled XCT-SOI MOSFET**

This section comprehensively examines the potential of the scaled XCT-SOI MOSFET. Calculated values of the on-current ( $I_{on}$ ), the off-current ( $I_{off}$ ), the intrinsic switching time ( $C_G V_D / I_{on}$ ), the switching energy ( $E_{sw}$ ), and the standby power ( $P_{stby}$ ), are summarized in Table 2, where it is assumed that the threshold voltage ( $V_{TH}$ ) is 0.2 V and  $W_G / L_G = 5$ , regardless of scale. Here, we assume that  $C_{G,XCT} = C_{G,MOS}$ ; in other words, SPFE is not assumed in Table 2. From Table 2, we can identify the following.

- (i) The graded source/drain junction improves the drivability;
- (ii) The graded source/drain junction does not always reduce the off-current;
- (iii) The intrinsic switching time is degraded as the scaling is advanced if an abrupt junction is assumed. However, it can be drastically improved by using a graded junction due to the improved drivability;
- (iv) The switching energy will be further reduced when SPFE is taken into account.

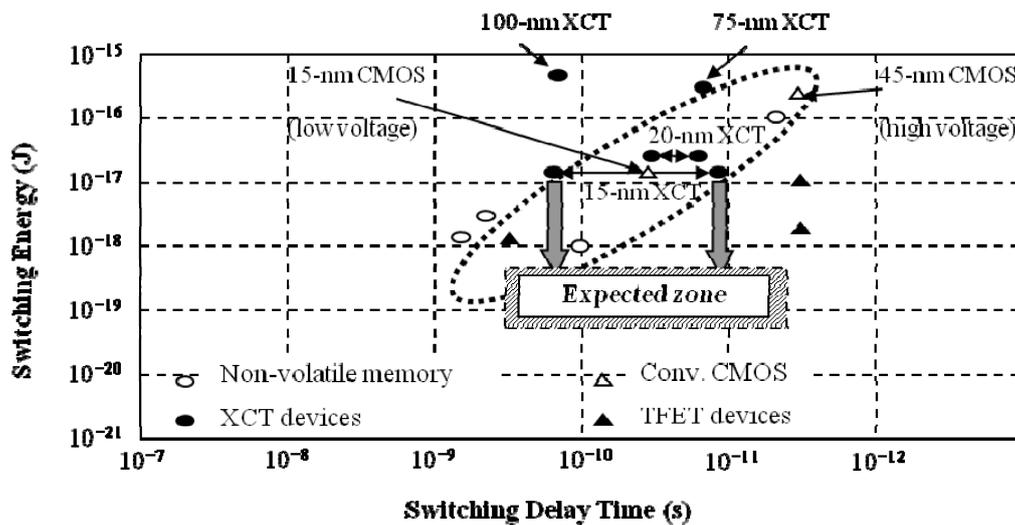
**Table 2.** Performance perspectives of scaled XCT-SOI MOSFET.

$L_G$ (nm)/ $W_G$ (nm)	$I_{on}$ (A)	$I_{off}$ (A)	$C_G V_D / I_{on}$ (s)*	$E_{sw}$ (J)*	$P_{stby}$ (W)*	
100/500	$5.4 \times 10^{-6}$	$2.5 \times 10^{-9}$	$1.7 \times 10^{-10}$	$5.1 \times 10^{-16}$	$2.8 \times 10^{-9}$	
75/375	$1.0 \times 10^{-5}$	$1.3 \times 10^{-9}$	$1.6 \times 10^{-11}$	$3.0 \times 10^{-16}$	$1.3 \times 10^{-9}$	
20/100	abrupt S/D	$1.7 \times 10^{-6}$	$7.6 \times 10^{-9}$	$4.9 \times 10^{-11}$	$2.1 \times 10^{-17}$	$3.8 \times 10^{-9}$
	graded S/D	$2.2 \times 10^{-6}$	$2.4 \times 10^{-9}$	$3.8 \times 10^{-11}$	$2.1 \times 10^{-17}$	$1.9 \times 10^{-9}$
15/75	abrupt S/D	$5.2 \times 10^{-7}$	$2.1 \times 10^{-10}$	$1.4 \times 10^{-10}$	$1.2 \times 10^{-17}$	$9.0 \times 10^{-11}$
	graded S/D	$4.4 \times 10^{-6}$	$1.9 \times 10^{-9}$	$1.6 \times 10^{-11}$	$1.2 \times 10^{-17}$	$8.2 \times 10^{-10}$

\*It is assumed that  $C_{G,XCT} = C_{G,MOS}$ .

In order to evaluate the above aspects of the scaled XCT-SOI MOSFET, we start by referring to the ITRS roadmap 2011 [14]. Figure 10 shows the projected switching performance suggested by the ITRS roadmap 2011; the calculation results of various XCT-SOI devices are also plotted. Simple calculation results reveal that 15-nm-long gate XCT-SOI devices without SPFE are identical to the non-volatile memory device group. However, it is worthwhile to note that the 15-nm-long gate XCT-SOI device is expected to lie in the zone below the non-volatile memory zone; SPFE should provide XCT-SOI devices with much better performance (“expected zone”) than that shown in Figure 11.

**Figure 11.** Comprehensive examination of scaled XCT-SOI MOSFET based on the ITRS roadmap 2011. Expected zone is estimated by assuming the SPFE, based on the model shown in Figure 1c.



**6. Conclusions**

We demonstrated the low-energy operation of XCT-SOI CMOS devices scaled down to 15 nm and analyzed the key underlying mechanism. It was shown that the source-follower like operation of the XCT-SOI MOSFET dynamically reduces the effective input capacitance, and, thus, the energy dissipated by XCT-SOI devices. This operation should be called the “*source potential floating effect (SPFE)*”. It is predicted, based on a physics-based model, that realizing SPFE in XCT-CMOS circuits will significantly suppress standby power dissipation.

It was also suggested that such aspects are still available in the sub-30-nm-long gate regime. Therefore, we can state that XCT-SOI CMOS devices are very promising for future extremely-low-energy circuits that suit medical implant applications.

**Acknowledgments**

A part of this study was supported by “Strategic Project to Support the Formation of Research Bases at Private Universities” in Japan: Matching Fund Subsidy from MEXT (Ministry of Education, Culture, Sports, Science and Technology) in Japan.

**Conflicts of Interest**

The authors declare no conflict of interest.

**References**

1. Colinge, J.P. *Silicon-On-Insulator Technology: Materials to VLSI*, 3rd ed.; Kluwer Academic Publishers: Dordrecht, the Netherlands, 2004; pp. 151–277.
2. *FinFETs and Other Multi-Gate Transistors*; Colinge, J.P., Ed.; Springer: New York, NY, USA, 2008; Chapter 1, pp. 4–28.

3. Omura, Y.; Izumi, K. High-Gain Cross-Current Tetrode MOSFET/SIMOX and Its Application. In Proceedings of the 18th International Conference of the Solid State Devices and Materials, Tokyo, Japan, 1986; pp. 715–716.
4. Blalock, B.J.; Cristoloveanu, S.; Dufrene, B.M.; Allibert, F.; Mojarradi, M. The multiple-gate MOSFET-JFET transistor. *Int. J. High Speed Electron. Syst.* **2002**, *12*, 511–520.
5. Omura, Y.; Fukuchi, K.; Ino, D.; Hayashi, O. Scaling scheme and performance perspective of cross-current tetrode (XCT) SOI MOSFET for future ultra-low power applications. *ECS Trans.* **2011**, *35*, 85–90.
6. Azuma, Y.; Yoshioka, Y.; Omura, Y. Cross-Current SOI MOSFET Model and Important Aspects of CMOS Operations. In Proceedings of the International Conference of the Solid State Devices and Materials, Tsukuba, Japan, 2007; pp. 460–461.
7. Omura, Y. Cross-current silicon-on-insulator metal-oxide semiconductor field-effect transistor and application to multiple voltage reference circuits. *Jpn. J. Appl. Phys.* **2009**, *48*, 04C07–04C11.
8. Omura, Y.; Azuma, Y.; Yoshioka, Y.; Fukuchi, K.; Ino, D. Proposal of preliminary device model and scaling scheme of cross-current tetrode silicon-on-insulator metal-oxide-semiconductor field-effect transistor aiming at low-energy circuit applications. *Solid-State Electron.* **2011**, *64*, 18–27.
9. Omura, Y.; Ino, D. Definite Feature of Low-Energy Operation of Scaled Cross-Current Tetrode (XCTY) SOI CMOS Circuit. In Proceedings of the 17th Workshop on Synthesis and System Integration of Mixed Information Technologies (SASIMI 2012), Beppu, Japan, 2012; pp. 355–360.
10. Synopsys Inc. *Sentaurus Operations Manual*; Synopsys: Mountain View, CA USA, 2008.
11. Synopsys Inc. *HSPICE Users Manual*; Synopsys: Mountain View, CA USA, 2008.
12. Sato, D.; Omura, Y. Scaling Scheme Prospect of XCT-SOI MOSFET Aiming at Medical Implant Applications Showing Long Lifetime with a Small Battery. In Proceedings of the IEEE International Meeting for Future of Electron Devices, Kansai (IMFEDK), Suita, Japan, 2013; pp. 38–39.
13. Omura, Y.; Nakano, S.; Hayashi, O. Gate-field engineering and source/drain diffusion engineering for high-performance Si wire GAA MOSFET and low-power strategy in sub-30-nm-channel regime. *IEEE Trans. Nanotechnol.* **2011**, *10*, 715–726.
14. ITRS Roadmap. <http://www.itrs.net/Links/2011ITRS/Home2011.htm> (accessed on 20 January 2012).