Journal of
Low Power Electronics and Applications

MDPI

Editorial

Ultra-Low-Power ICs for the Internet of Things

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The collection of research works in this Special Issue focuses on Ultra-Low-Power (ULP) Integrated Circuits (ICs) operating under a tight budget of power as a criterion to build electronic devices relying less and less on batteries. These enable the Internet of Things (IoT): a view of a world in which we are surrounded by devices that exchange data to enhance our quality of living. Thus, the goals of novel IC design strategies target both reducing the cost and the power consumption of any device. A method to reduce the cost is to minimize the use of a manual design process and maximize the use of a digital (automated) design flow so that the design is transferable across technological nodes. A digital-in-concept design also allows the scale of the supply voltage and offers a performance–power consumption trade-off [1–4]. In particular, a two-stage inverter-based operational transconductance amplifier (OTA) using rail-to-rail output operating with a supply voltage of 0.5 V is presented in [1]. Then, a novel implementation of a digital-based OTA consisting of only digital gates usually available in the standard cell libraries is the focus of [2]. In [3], a novel fully standard-cell-based common-mode feedback (CMFB) loop to improve the CMRR and to stabilize the DC output voltage of pseudo-differential standard-cell-based amplifiers is proposed. To further explore complexity, dynamic performance, and energy efficiency, a fully synthesizable digital–delta (Δ) modulator (ΔM) ADC with noise shaping using passive components (i.e., integrated capacitors and resistors) and standard-cell-based amplifiers is presented in [4].

The other research works exploit other methods, focusing on increasing the energy efficiency for a number of building blocks for general-purpose applications (i.e., amplifiers); more specifically, they target biomedical applications or at the system level. ULP/Ultra-Low-Voltage (ULV) ICs exploring bulk-drive solutions and operating with Sub-1V supply voltage down to 0.3 V were considered [5–8]. In [5], the authors proposed a new technique to improve the DC voltage gain, while keeping the high linearity in symmetrical bulk-driven (BD) OTA topology. A novel tree-based architecture that allows the implementation of a ULV OTA exploiting a body-driven input stage to guarantee a rail-to-rail input common mode range is also described in [6]. A bootstrapped BD Voltage Buffer is used to increase the intrinsic voltage gain of the Second-Order Gm-C Bandpass Filter in [7]. Moreover, a current-controlled CMOS ring oscillator topology, which exploits the bulk voltages of the inverter stages as control terminals to tune the oscillation frequency, is proposed and analyzed in [8]. Then, a fully differential (FD) instrumentation amplifier aimed at electrical impedance measurements in an IoT biomedical scenario is presented in [9].

To assist the ULP IC design flow, a compact and simplified approach that contains only four parameters and is based on the Advanced Compact MOSFET (ACM) model was implemented in Verilog-A and compared with the BSIM model in [10].

Sinusoidal oscillators based on second-generation voltage conveyors are investigated in [11], while a relaxation oscillator with valuable line sensitivity for Low Power Applications is shown in [12].

The last two studies in this Special Issue consider the IC as part of a ULP/ULV sensor system that needs to interact with the surrounding environment.

A wideband cascaded receiver including an inverter-based low-noise transconductance amplifier and a stacked receiver using an improved clock strategy with reduced mixer

Citation: Aiello, O. Ultra-Low-Power ICs for the Internet of Things. *J. Low Power Electron. Appl.* **2023**, *13*, 38. https://doi.org/10.3390/jlpea13020038

Received: 23 May 2023
Accepted: 24 May 2023
Published: 26 May 2023

switches is described in [13]. Hardware solutions for Low-Power Smart Edge Computing are presented in [14].

In summary, the published research works cover a wide area of the ULP/ULV IC field, offering the reader many ideas inspired by these innovative design approaches.

Acknowledgments: The Guest Editor of the Special Issue "Ultra-Low-Power ICs for the Internet of Things" thanks the Multidisciplinary Digital Publishing Institute (MDPI) for the invitation to write this Editorial as a presentation of the 14 papers published in this Special Issue which is freely available at https://www.mdpi.com/journal/jlpea/special_issues/low_power_iot. Moreover, based on the success of this Special Issue, a "Volume 2" has been launched at https://www.mdpi.com/journal/jlpea/special_issues/919Q5756T0.

Conflicts of Interest: The author declares no conflict of interest.

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