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A Time-Mode PWM 1st Order Low-Pass Filter †

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Abstract: In this work, a first-order low-pass filter is proposed as suitable for time-mode PWM signal processing. In time-mode PWM signal processing, the pulse width of a rectangular pulse is the processing variable. The filter is constructed using basic time-mode building blocks such as time registers and time adders and so it is characterized by low complexity which can lead to the modular and versatile design of higher-order filters. All the building blocks of the filter were designed and verified in a TSMC 65 nm technology process. The sampling frequency was 5 MHz, the gain of the filter at low frequencies was at −0.016 dB, the cut-off frequency was 1.2323 MHz, and the power consumption was around 59.1 μW.

Keywords: time-mode signal processing; time-mode filters; time registers; time adders; z^{-1} operators; CMOS

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1. Introduction

Analog circuits are continuously losing benefits through technology scaling. The reduction of the voltage headroom has resulted in limitations in the voltage swing of analog signals. In addition, the shrinkage of the channel length of transistors makes analog circuits vulnerable to non-linearities and current leakage. On the other hand, digital circuits are benefiting from the constant device scaling, improving their processing speed and resolution due to the superiority of time resolution to the voltage equivalent in these processes [1,2].

An interesting alternative to conventional analog circuits is time-mode circuits. The difference in this procedure is that the information is expressed in the field of time instead of voltage or current as it happens in the typical approaches. There are two types of time-mode processing with respect to the way that the information is represented. In the first, the information is expressed as the time interval between the positive edges of two pulse signals. In the second, the information is represented by different values of the pulse widths (PWM) of a pulse [3]. The advantages of time-mode circuits are that they are constructed by standard digital logic gates, which benefit from the device scaling due to the superiority of time resolution and are not affected by voltage supply reduction.

A block diagram of a time-mode system suitable for pulse-width modulation signal processing is presented in Figure 1. Firstly, a voltage-to-time converter (VTC) is employed to convert the analog continuous-time signal V_{in} into a time-mode signal T_{in} [4,5]. The VTC consists of a sample-and-hold circuit that samples the continuous voltage signal with a sampling period T_s and a pulse-width modulator that converts every voltage sample into a rectangular pulse. The input signal of the time-mode unit will actually be a pulse train in which every pulse will have the same frequency as the sampling signal, but the pulse width will be equal to a linear function of the corresponding voltage sample. After the conversion, the information is processed in the time mode. The time-mode processing unit could include many simple operations like a z^{-1} operation, addition,

subtraction, amplification [6], or multiplication [7,8]. Furthermore, a combination of these simple operations can be achieved if more complex processing is needed (e.g., time-mode filtering [9–11] and time-mode integrators [12–14]). Finally, the processed time-mode signal is converted back to the voltage mode via a time-to-voltage converter (TVC). It should be mentioned that the processed time-mode information can be quantized via a time-to-digital converter (TDC) if further processing is needed by a digital signal processing unit [15–17].

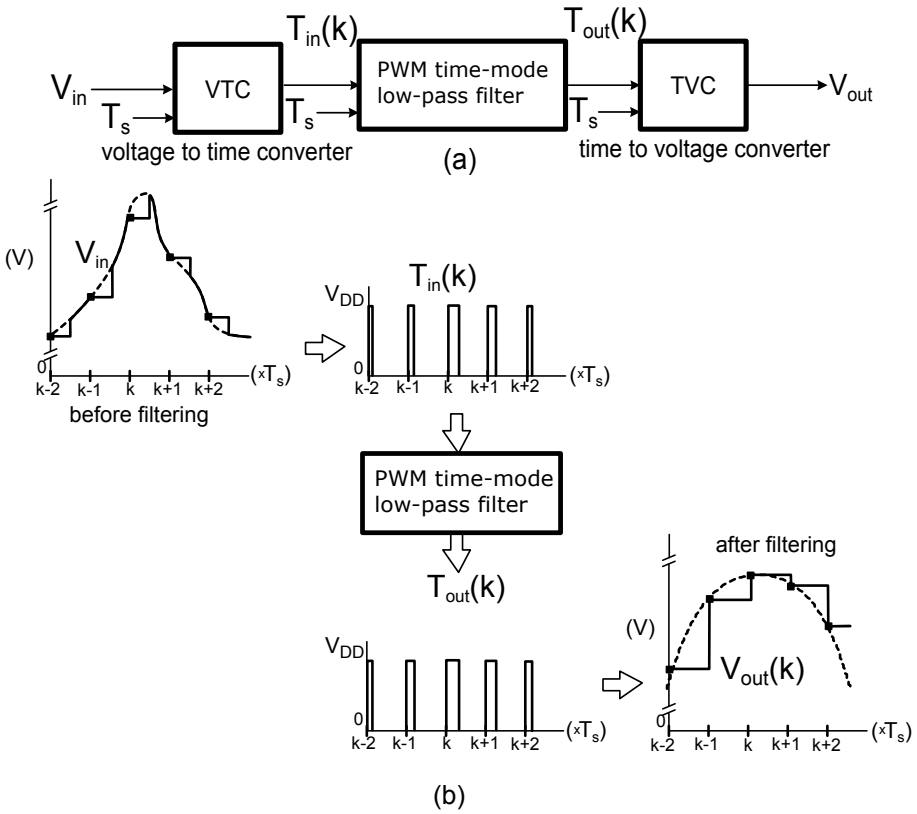

Figure 1. (**a**) Conceptual system block of the PWM time-mode low-pass filter, (**b**) Signal flow of the PWM time-mode filter.

Analog signal filtering is very important in many applications such as sensor interfaces, wireless transceivers, and signal/image processing. Low-order filters can be used in systems where the cut-off frequency is relaxed, offering low complexity and a small layout area. According to the author's best knowledge, there is no implementation of a first-order low-pass filter that operates in time mode, already published in the literature. This is the main contribution made in this work.

More specifically, this work presents a time-mode first-order low-pass filter as a design example suitable for time-mode signal processing (TMSP). The circuit consists of a time-mode z^{-1} operator and a z^{-1} weighted time-mode adder with gain $1/2$. All the building blocks of the z^{-1} operator and the weighted time adder are based on the time-register circuit. The low-pass filter is achieving the desired operation over process and temperature corners. Lastly, it is characterized by modular design, so it can be used as a building block for higher-order filters.

The paper is organized as follows. In Section 2, the top-level topology of the low-pass filter is presented as well as the time-mode building blocks that the filter consists of. In Section 3, a brief presentation of the digital calibration loop is presented which was used in order to achieve the desired frequency response, phase response, and cut-off frequency over process and temperature corners. Section 4 presents the simulation results to evaluate the filters' behavior with respect to their frequency response, phase response, cut-off frequency, and power consumption. Finally, the conclusions from this work are presented in Section 5.

2. Implementation of the Time-Mode PWM Low-Pass Filter

2.1. Top-Level Architecture

The proposed top-level topology of the time-mode PWM low-pass filter is presented in Figure 2a. The circuit architecture, which is presented in Figure 2b, consists of a z^{-1} operator and a z^{-1} time adder with a gain equal to 1/2. The operation principle is based on the application of z-transformation to the analog circuits and systems [18]. The timing diagram of the circuit is presented in Figure 2c. The first input of the time adder receives the input signal directly and so the $T_{int.1}(k)$ signal will be equal to the $T_{in}(k)$ signal. It is assumed that the input signal is basically a pulse train in which every pulse has the same frequency as the sampling signal and is synchronous with it. On the second input of the time adder, the input pulse train is first passed through a z^{-1} operator which delays every input pulse by one sampling clock and then it is connected on the second input of the time adder. Hence, the node $T_{int.2}(k)$ will be equal to:

$$T_{int.2}(k) = T_{in}(k-1) \tag{1}$$

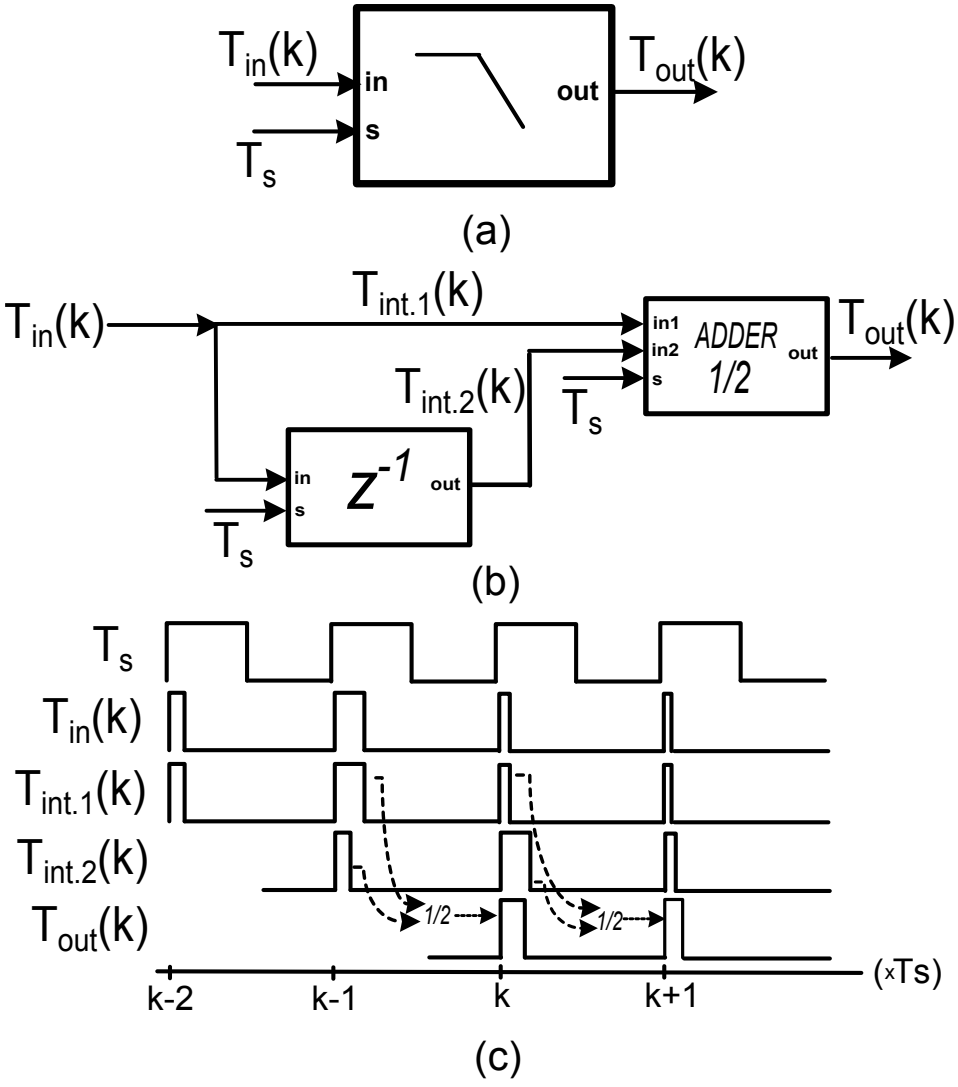

Figure 2. (**a**) Top-level topology, (**b**) circuit architecture, and (**c**) timing diagram.

Lastly, the time adder sums the two inputs and multiplies their product with a weight equal to 1/2. The time adder also adds one more time delay, which is equal to the sampling clock, to both input signals due to its inherent z^{-1} operation. As a result, the relationship between the output pulse width T_{out} and the input pulse width T_{in} of the low-pass filter is:

$$T_{out}(k) = \frac{1}{2}[T_{int.1}(k-1) + T_{int.2}(k-1)] = \frac{1}{2}[T_{in}(k-1) + T_{in}(k-2)] \quad (2)$$

where k is the time index. The z-domain transfer function of the above input–output equation is:

$$H(z) = \frac{z^{-1}}{2}(z^{-1} + 1) \quad (3)$$

At low frequencies, the signal time delay, which is always equal to one sampling clock due to the z^{-1} operation, is small compared to the period of the input signal. Hence, for those frequencies, the z^{-1} variable of Equation (3) is approximately equal to unity and therefore the gain of the impulse response that is described by Equation (3) will be approximately equal to 1. As the frequency increases, the time delay of the input signal becomes comparable to the sampling period. At the point where the frequency of the input signal becomes half the sampling frequency, the input signals of the time adder will have a 180° difference in phase. Therefore, their sum will be neglected and the gain of the transfer function will be zero. Therefore, the z-domain transfer function that was mentioned in Equation (3) describes a low-pass filter behavior in which, for frequencies sufficiently lower than the sampling frequency, the input signal will pass to the output and, for frequencies compared to the sampling frequency, the input signal will be attenuated [18]. It should be mentioned that for frequencies above half of the sampling frequency, the transfer function rebounds due to the aliasing effect as happens in many discrete-time systems. Thus, an anti-aliasing filter is needed during the reconstruction of the information to the voltage mode [18].

Finally, the transfer function of an ideal discrete time z-domain low-pass filter is given by $H(z) = (1/2)(z^{-1} + 1)$ because it is assumed that the time adder does not add a time delay. Comparing the aforementioned equation with Equation (3), an extra phase difference between the output and input signals will be expected due to the additional delay added by the time adder.

2.2. Time-Mode PWM Building Blocks

2.2.1. Time Register Based on Gate-Controlled Current Source

The time register that has been used is based on the gate-controlled approach that is presented in Figure 3 [19]. The behavior of the time register is based on the constant discharging slope of capacitor C. The T_{set} signal is equal to the sampling signal. During the time where T_{set} = '0' ('0' means asserted to the ground), the capacitor is connected to the supply via transistor M1 which acts as a switch. Hence, the capacitor is charged to the voltage supply V_{DD}. On the other hand, when T_{set} = '1' ('1' means asserted to the voltage supply), there are three distinct operations of the circuit. During the time interval of which T_{in} = '1', the capacitor is discharged via transistor M2 which acts as a current source, delivering constant discharging current equal to I_{ref}. The current I_{ref} that the current source delivers is controlled by its' gate voltage V_{CTRL}. The gate voltage of M2 is controlled through switches in order to be connected to V_{CTRL} or to the ground with respect to digital control signal TR_{in}, where $TR_{in} = T_{in} + T_{clk}$ due to the OR gate. The value of the discharging capacitors' slope is equal to:

$$slp = \frac{I_{ref}}{C} \quad (4)$$

At the time when both T_{in} = '0' and T_{clk} = '0' (they are both equal to zero voltage), the capacitor is floating and hence voltage V_{cap} remains constant. Finally, during the time interval of which T_{clk} = '1', the capacitor is also discharging with the constant slope described in Equation (4). During T_{clk} = '1' and when the voltage on the top plate of capacitor C crosses the reference voltage V_{tp} of the comparator, the latter changes state. The digital logic that follows the comparator results in an output pulse with a frequency equal to T_{set} while the phase between those two is equal to 180°. The pulse width of the output will be:

$$T_{out.reg}(k) = T_{clk} - T_{in}(k - 0.5) \quad (5)$$

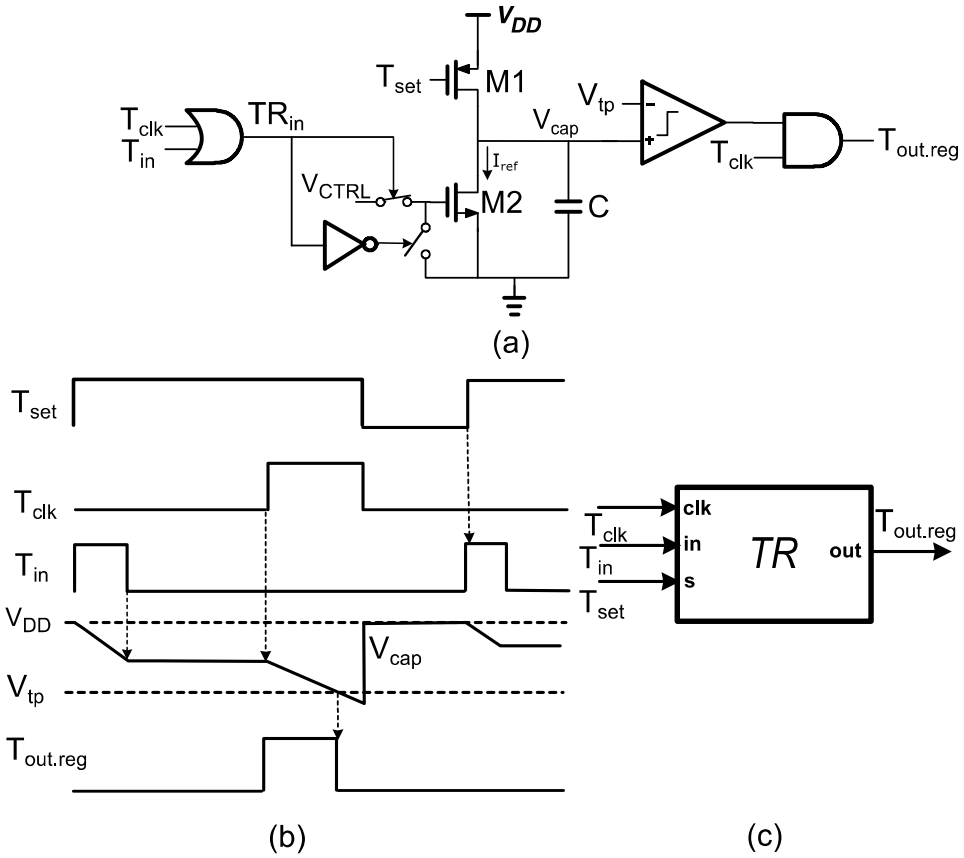

Figure 3. (**a**) Intuitive circuit schematic of the gate-controlled time register, (**b**) timing diagram, and (**c**) symbol.

2.2.2. Time-Adder Core Implementation with Gain 1/2

The time-adder core with gain 1/2 is presented in Figure 4. The operation principle of the circuit is based on the gate-controlled time register that is described earlier.

The difference here is that there are three discharging branches that deliver constant discharging currents with magnitudes equal to $I_{ref}/2$, I_{ref} /2, and I_{ref}, respectively. For this option, there are three different operations that affect the value of the discharging slope. At the time interval where T_{in1} = '1' and T_{in2} = '1', transistors M3 and M4 are both open and deliver constant discharging current. As a result, the total discharging current of the capacitor will be equal to I_{ref} and the value of the discharging slope will be given by Equation (4). When only one of the two inputs is connected to the supply, then the discharging current will drop to half and so will decrease the value of the discharging slope. Finally, during T_{clk} = '1', the circuit will have the same behavior as it had on the simple time register. Hence, every input signal will result in half of the voltage drop across the capacitor compared with the voltage drop from the T_{clk} signal. As a result, on the output of the time adder with gain 1/2, a pulse will be generated which will be delayed by half of a period of the T_{set} signal and with an output pulse width equal to:

$$T_{out.adder}(k) = T_{clk} + \frac{1}{2}[T_{in1}(k - 0.5) + T_{in2}(k - 0.5)] \quad (6)$$

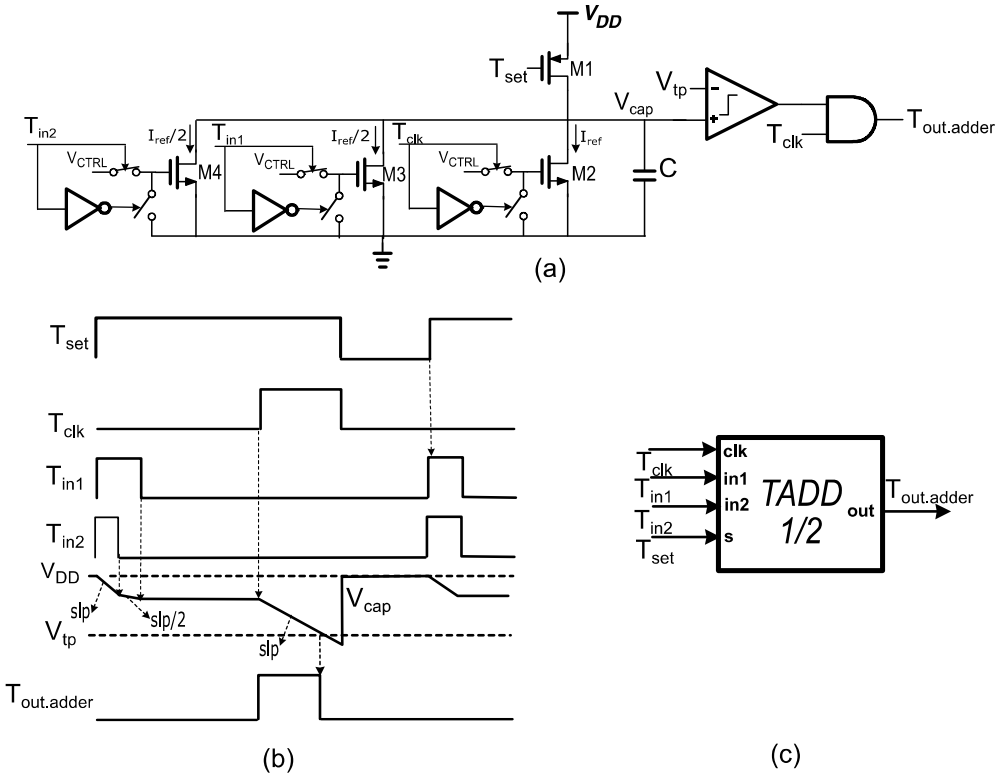

Figure 4. (**a**) Implementation of the time-adder core circuit with gain 1/2, (**b**) timing diagram, and (**c**) symbol.

2.2.3. Implementation of a z^{-1} Operator Using a Time Register

The z^{-1} operation is achieved by employing two cascaded time registers as presented in Figure 5. For the z^{-1} operation, the architecture which employs two cascaded time registers is selected instead of the architecture which uses four, in order to achieve less layout area, lower power consumption, and larger resolution [19].

The T_{set1} signal (sampling signal) and the T_{set2} signal have the same pulse width but with a phase difference equal to 180°. Furthermore, the T_{clk1} and T_{clk2} signals have the same pulse width but with phases equal to 180° and 0°, respectively, with respect to the sampling signal (T_{set1} signal).

The front-end time register receives an input pulse T_{in}, synchronous with the sampling signal, and produces an output pulse $T_{internal}$ delayed by half of a period of the T_{set1} signal and with a pulse width equal to the complementary value of T_{in} in respect to T_{clk}:

$$T_{internal}(k) = T_{clk} - T_{in}(k - 0.5) \quad (7)$$

The second time register receives $T_{internal}$ and produces output pulses delayed by half of a period of the T_{set2} signal and with a pulse width equal to the complementary value of $T_{internal}$ with respect to T_{clk}. As a result, the output pulse of the whole z^{-1} operator will be a pulse delayed by one T_{set1} clock and with a pulse width equal to the inputs' pulse width:

$$T_{out}(k) = T_{clk} - T_{internal}(k - 1) = T_{in}(k - 1) \quad (8)$$

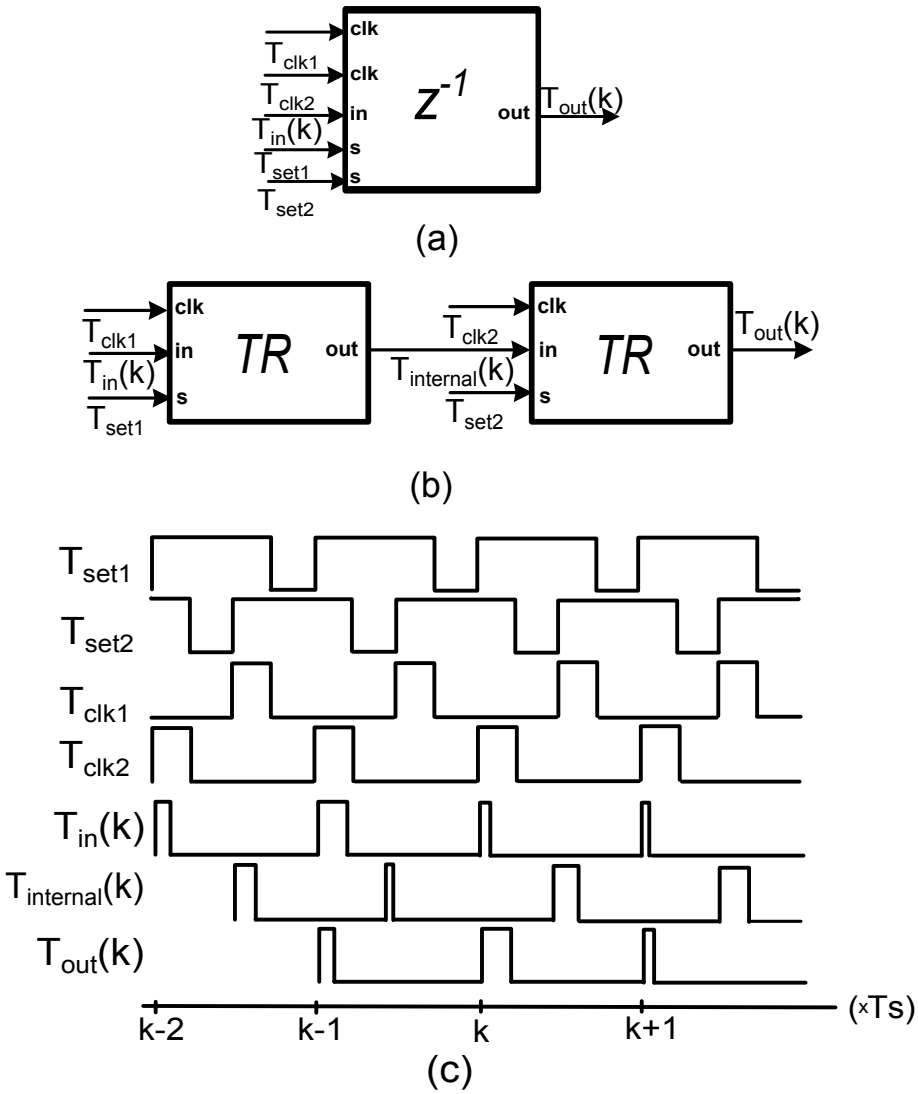

Figure 5. (**a**) Symbol of z^{-1} operator, (**b**) architecture with two cascaded time registers, and (**c**) timing diagram.

2.2.4. Implementation of the z^{-1} Time Adder with Gain 1/2

The implementation of the z^{-1} time adder with time gain 1/2 is illustrated in Figure 6. The T_{set1} signal is the sampling signal. In the implementation of the time adder, the time register is replaced by the time-adder core with gain 1/2 that was described earlier. As a result, the internal signal of the circuit will also be a pulse delayed by half of a period of the sampling signal but with a pulse width equal to the complementary value of half of the sum of the two inputs T_{in1} and T_{in2} of the time-adder core with respect to the T_{clk} signal:

$$T_{internal}(k) = T_{clk} + \frac{1}{2}[T_{in1}(k-0.5) + T_{in2}(k-0.5)] \quad (9)$$

The time register has the same behavior as it had on the z^{-1} operation, shifting the $T_{internal}$ signal by half of a period of the T_{set1} signal and producing an output pulse with a pulse width equal to:

$$T_{out}(k) = T_{clk} - T_{internal}(k-0.5) = \frac{1}{2}[T_{in1}(k-1) + T_{in2}(k-1)] \quad (10)$$

Hence the output of the circuit will be a pulse delayed by sampling signal and with a pulse width equal to half of the sum of the two inputs of the circuit.

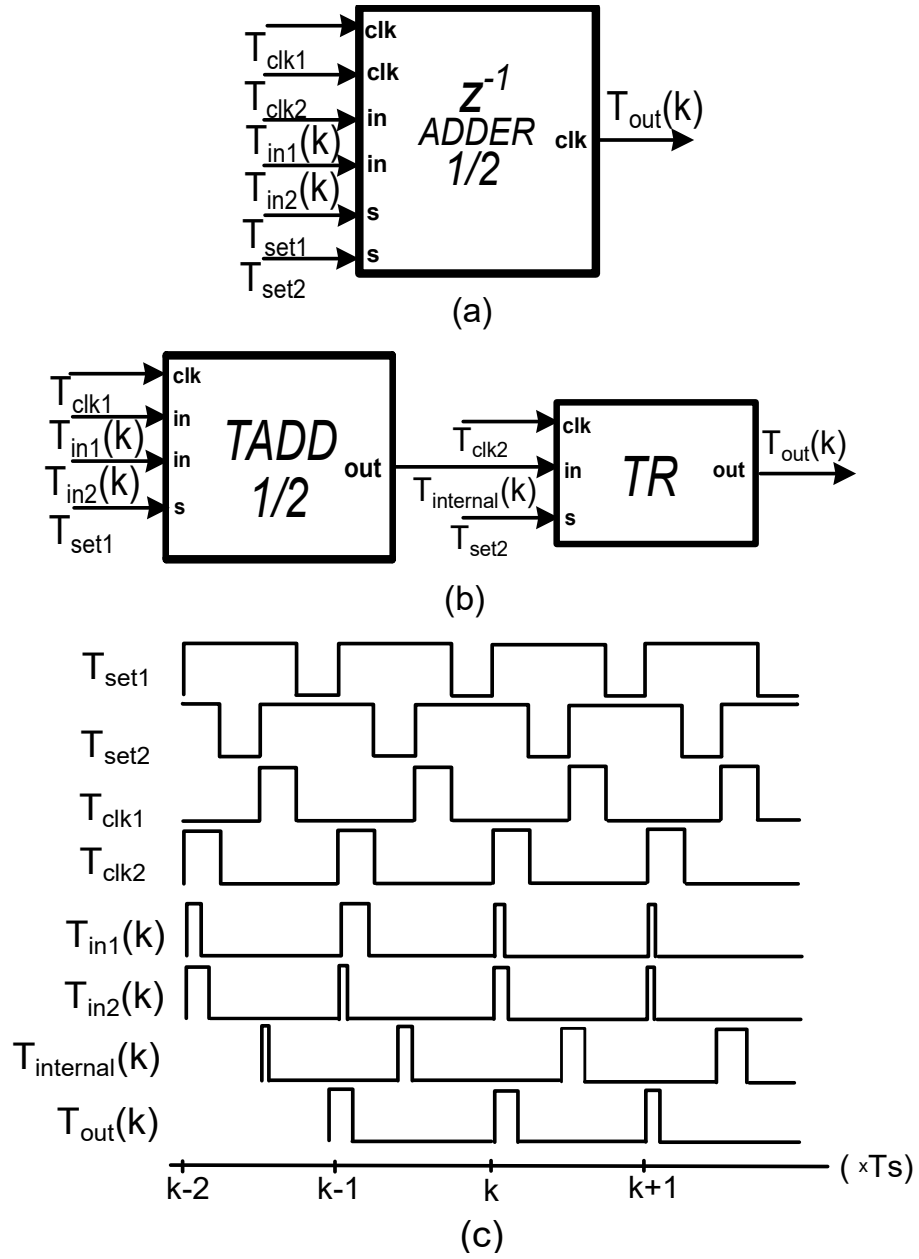

Figure 6. (**a**) Symbol of z^{-1} time-adder with gain 1/2. (**b**) architecture with the TADD 1/2 in series with time register, and (**c**) timing diagram.

3. Discharging Slope Digital Calibration

The value of the constant discharging slope of the time register and time-adder with gain 1/2 must be well defined for the maximum available input range to be achieved by the time-mode building blocks [19]. However, the discharging current and, also, the capacitor's capacitance that directly affects the value of the discharging slope are sensitive to process (P) and temperature (T) variations (PT variations). To compensate for the PT variations of the discharging slope, a digitally controlled calibration loop is adopted as described in [20] and briefly presented in Figure 7.

Briefly, in this calibration loop, the discharging current is controlled by an 8-bit digital control code. At the beginning of the calibration, the digital code takes its minimum value, generating the minimum value for the discharging current of the time register. In each calibration cycle, the value of the digital code (and the discharging current) increases until, during a time interval of the T_{clk} signal, the capacitor voltage drops from the voltage supply

to the triple point of the leading comparator. At this point, the digital code stops increasing and locks to a specific value, delivering the desirable constant discharging current to achieve maximum input range.

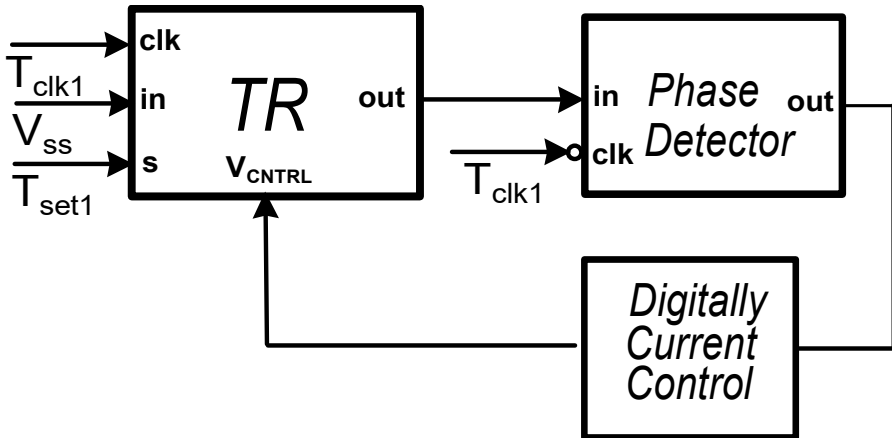

Figure 7. Intuitive topology of digital calibration loop.

4. Simulation Results

The low-pass time-mode filter was designed and described with respect to its frequency response, cut-off frequency, phase response, and power consumption over PT corners. The circuit was designed using the Cadence Virtuoso environment and simulated using the Spectre simulator. The time-mode building blocks were designed using the TSMC 65 nm technology process. The voltage supply was set in 1.2 V and the sampling frequency was equal to 5 MHz. The capacitor value in every time-mode building block was 2 pF. Transistor M1 size was selected to be 650 nm/260 nm in order to deliver enough current to charge the output capacitor and to have relatively large resistance when it is in the off state. Transistors M2, M3, and M4 had lengths equal to 2 μm in order to be characterized by large gate-to-source resistance and work as current sources. They also had widths equal to 2 μm, 1 μm, and 1 μm, respectively, to deliver discharging current equal to I_{ref}, $I_{ref}/2$, and $I_{ref}/2$ accordingly.

In Figure 8, the testbench that was used to simulate the behavior of the low-pass filter is presented. The VTC converts the input signal from voltage mode to time mode and the TVC converts the time-mode signal to the voltage-mode. These two blocks are ideal Verilog-A models in order to not disturb the performance metrics. On the input of the entire system, a sinusoidal signal is applied equal to $V_{in} = 0.5\ V_{DD} + V_{in.peak}\ \sin(2\pi f_{in} \cdot t)$, where $0.5\ V_{DD}$ is the average voltage, $V_{in.peak}$ is the amplitude, and f_{in} is the input frequency. The VTC converts this signal into a pulse train in which every pulse has magnitude:

$$T_{in}(t) = 25\ \text{ns} + T_{in.peak} \sin(2\pi f_{in} t) \quad (11)$$

where $T_{in.peak}$ is the corresponding pulse magnitude width and ranges from 0 to 25 ns. Therefore, the width of every pulse ranges from 0 to 50 ns in a sinusoidal manner.

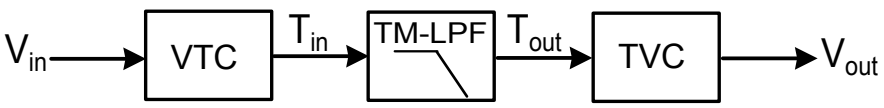

Figure 8. Simulation test bench for the characterization of the time-mode PWM low-pass filter.

In Figure 9, the transient response of the input and the output are presented for a signal with a frequency equal to 58.59375 kHz. As can be seen, the input and the output signals have equal magnitudes, since the input signal has a frequency much smaller than the sampling frequency. Hence, the filter achieves unit gain for small frequency signals,

verifying the correct behavior of the filter in this frequency range. The output signal is delayed by one sampling clock period due to the z^{-1} operation which is inherent to the time adder.

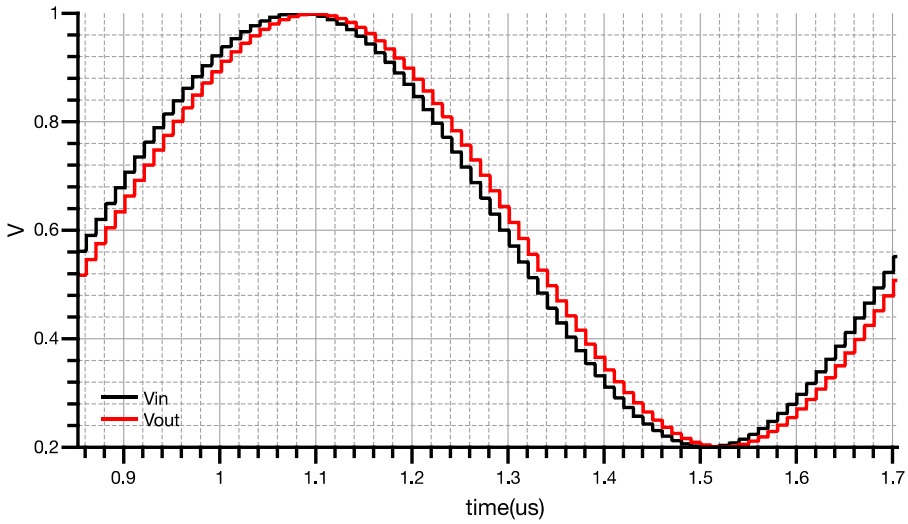

Figure 9. Input and output transient response of the low-pass filter for frequency 58.59375 kHz.

In Figure 10, the frequency response over PT corners of the first-order low-pass filter for a frequency range between 10 kHz and 2.5 MHz is presented. The filter's gain response for several input frequencies was measured by employing discrete Fourier transform (DFT) on the input and output signals of the system that is presented in Figure 8. The formula that was used to calculate the gain response is:

$$A_{dB} = \frac{A_{out.f0}}{A_{in.f0}} \tag{12}$$

where f_0 is the fundamental frequency of the input signal, and $A_{in.f0}$ and $A_{out.f0}$ are the magnitudes on the fundamental frequency of input and output signals, respectively.

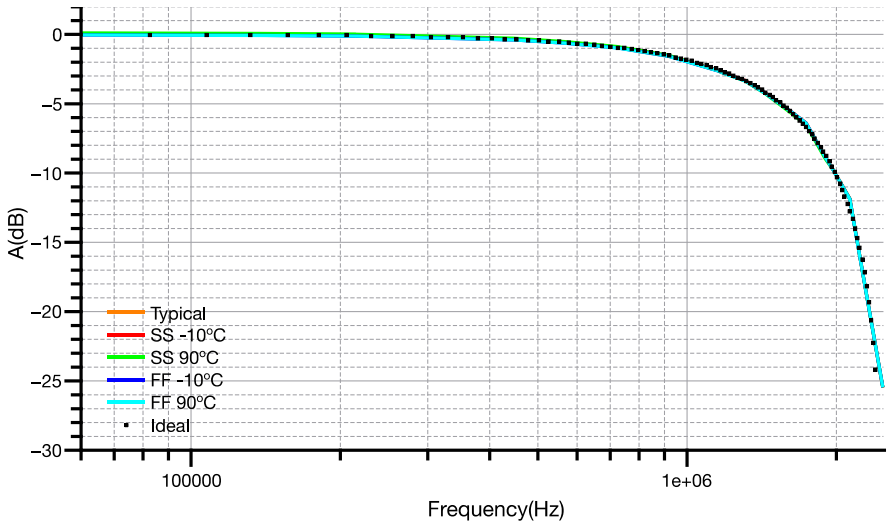

Figure 10. Frequency response of the time-mode low-pass filter over PT corners.

As it can be observed, the filter almost perfectly matched the ideal frequency response that is described with the dotted waveform for every corner. The gain in low frequencies (e.g., 58.59375 kHz) is equal to −0.016 dB for the typical case and 0.1 dB maximum variation

over the worst PT corners. The cut-off frequency of the filter for the typical case is equal to 1.2323 MHz featuring 4.13 kHz worst-case variation over PT corners. The difference in the cut-off frequency between the ideal behavior and the typical behavior of the circuit is around 13 kHz.

In Figure 11, the phase response of the time-mode low-pass filter is illustrated for a frequency range between 10 kHz and 2.5 MHz. The phase response was measured by employing DFT in the input and output signals of the system, calculating the phase difference described by:

$$Phase(^{o}) = \theta_{out.f0} - \theta_{in.f0} \quad (13)$$

where $\theta_{in.f0}$ and $\theta_{out.f0}$ are the phases of the input and output signals, respectively. The phase difference between the output and input of the system has a linear relationship with the frequency of the input signal, as is expected by discrete-time system theory. It should be mentioned that, in relation to the phase response of an ideal discrete z-domain low-pass filter, an additional phase difference is added due to the inherent z^{-1} operation of the time adder. As a result, the proposed system presents a phase difference of -135° at the cut-off frequency instead of -45° of the ideal discrete low-pass filter in which the time adder does not add additional time delay.

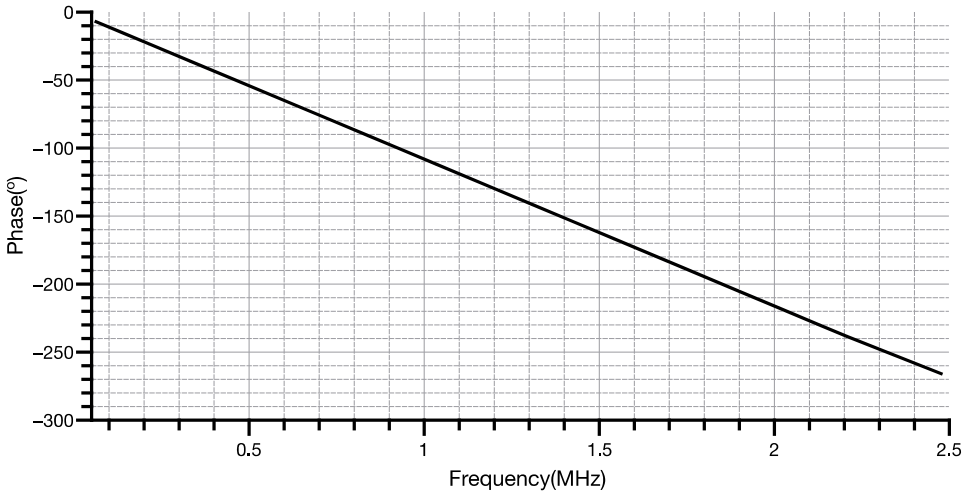

Figure 11. Phase response of the time-mode low-pass filter.

Lastly, the summary results of the time-mode z-domain low-pass filter are presented in Table 1.

Table 1. Summary results of the first-order time-mode low-pass filter.

	Units	Min.	Typ.	Max.
$F_{sampling}$	MHz		5	
Gain @ 58.59 kHz	dB	−0.045	−0.031	0.106
$f_{cut.off}$	MHz	1.2273	1.2323	1.2352
Power Consumption	μW		59.04	

5. Conclusions

In this work, a first-order low-pass time-mode filter was designed. The filter is constructed using a z^{-1} operator and a time adder with gain 1/2. The circuit achieves the desired frequency response, cut-off frequency, and phase response over process and temperature corners. Due to its modular design and the fact that is synchronous with the sampling signal of the system, it can be used as a fundamental building block in the field of time-mode z-domain circuits and systems. As a result, this topology is going

to be employed in the implementation of more complex filters suitable for time-mode z-domain signal processing, such as z-domain filters based on bilinear approximation and analog FIR/IIR filters. The implementation of time-mode z-domain filters is an interesting approach because it uses mainly digital standard cells while the analog part is minimized. Hence, it is characterized by low power consumption, high speed, and adaptation of technology scaling, in which the conventional pure analog approach fails [21].

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