Journal of
Low Power Electronics and Applications

MDPI

Article

A Novel Inductorless Design Technique for Linear Equalization in Optical Receivers

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Abstract: To mitigate the trade-off between gain and bandwidth of CMOS multistage amplifiers, a receiver front-end (FE) that employs a high-gain narrowband transimpedance amplifier (TIA) followed by an equalizing main amplifier (EMA) is proposed. The EMA provides a high-frequency peaking to extend the FE's bandwidth from 25% to 60% of the targeted data rate (f_{bit}). The peaking is realized by adding a pole in the feedback paths of an active feedback-based wideband amplifier. By embedding the peaking in the main amplifier (MA), the front-end meets the sensitivity and gain of conventional equalizer-based receivers with better energy efficiency by eliminating the equalizer stages. Simulated in TSMC 65 nm CMOS technology, the proposed front-end achieves 7.4 dB and 6 dB higher gain at 10 Gb/s and 20 Gb/s, respectively, compared to a conventional front-end that is designed for equal bandwidth and dissipates the same power. The higher gain demonstrates the capability of the proposed technique in breaking the gain-bandwidth trade-off. The higher gain also reduces the power penalty incurred by the decision circuit and improves the sensitivity by 1.5 dB and 2.24 dB at 10 Gb/s and 20 Gb/s, respectively. Simulations also confirm that the proposed FE exhibits a robust performance against process and temperature variations and can support large input currents.

Keywords: low-bandwidth TIA; equalizer; multi-stage main amplifier; amplitude response; group delay variation

Citation: Abdelrahman, D.; Williams, C.; Liboiron-Ladouceur, O.; Cowan, G.E.R. A Novel Inductorless Design Technique for Linear Equalization in Optical Receivers. *J. Low Power Electron. Appl.* **2022**, *12*, 19. https://doi.org/10.3390/jlpea12020019

Academic Editor: Andrea Acquaviva

Received: 27 December 2021
Accepted: 4 February 2022
Published: 1 April 2022

1. Introduction

Traffic in data centers has grown rapidly over the past decade due to the rapid growth of cloud computing and big data applications. This in turn drives the development of robust, high-speed, and energy-efficient interconnects to transfer the data around the data center. Several 100+ Gb/s optical links have recently been reported to satisfy the bandwidth and reach requirements [1–3]. However, the associated cost and power dissipation prevent their widespread adoption within the data center. In short-reach photonic links, the transmitted optical modulation amplitude (OMA) must be sufficiently large that, in spite of coupling and fiber losses, the received optical power exceeds the receiver's sensitivity limit. This sensitivity is a function of the input-referred noise current of the receiver as well as the voltage amplitude requirements of the decision circuit driven by the receiver front-end [4]. Therefore, an energy-efficient link design requires a low-noise as well as a high-gain receiver.

As data rates increase, traditional approaches to receiver design dictate that the bandwidth of the receiver also increases, which limits the maximum achievable gain [5]. This trade-off is less pronounced in SiGe BiCMOS technologies where the transistor has higher intrinsic gain and transit frequency. Therefore, a reasonable gain is still achievable

in wideband deigns. However, in CMOS, the trade-off limits the per-stage gain which necessitates cascading several gain stages to achieve the targeted output voltage amplitude. With increased number of stages, both noise and power dissipation increase.

This paper presents a novel inductorless design technique for high-gain optical receiver front-ends. Figure 1 illustrates the operation of the proposed front-end (FE) in contrast to the traditional wideband FE. Conventionally, the transimpedance amplifier (TIA) and the follow-on main amplifier (MA) are designed to have bandwidths in the order of $0.6f_{bit}$ and f_{bit}, respectively, to achieve an overall bandwidth of approximately $0.5f_{bit}$ [4]. In the proposed receiver, first, the TIA's bandwidth is reduced to approximately 25 % of the targeted data rate. The reduced TIA bandwidth allows for higher gain, lower input-referred noise, and fewer follow-on gain stages. The reduction in bandwidth also introduces inter-symbol interference (ISI) to the extent that the TIA's output eye diagram is fully closed. Unlike a bandlimited electrical channel which can introduce more than 30 dB of channel loss at the Nyquist frequency ($f_N = 0.5f_{bit}$), the low-bandwidth TIA introduces a moderate frequency-dependent attenuation. Consequently, a few dBs of amplitude peaking at f_N is sufficient to restore the required bandwidth (for example, the equalizer in [6] introduces only 7 dB of peaking). Therefore, in the second step of the proposed design technique, a high-frequency peaking is intentionally introduced in the main amplifier's amplitude response without impairing its low-frequency gain. Various possible designs of active feedback-based MA architectures [7–10] can introduce the required peaking by adding a pole in their feedback loops. The amplitude peaking in the equalizing main amplifier (EMA) is then used to compensate for the TIA's limited bandwidth to restore an overall bandwidth of approximately $0.5f_{bit}$. Although Figure 1 shows only the magnitude response of the TIA and EMA, group-delay variation must also be considered.

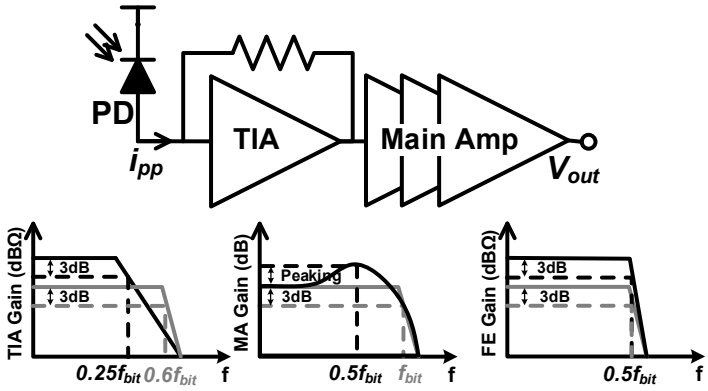

Figure 1. The proposed and the conventional receivers are represented by the same block diagram (**top**). The bottom graph illustrates the operation of the proposed receiver (black) in contrast to that of the conventional receiver (gray).

In contrast to traditional continuous-time linear equalizer (CTLE)-based designs [6,11], the proposed front-end attains the improved sensitivity and high-gain of these designs, while achieving better energy efficiency due to the elimination of the standalone equalizer stage(s). Traditional approaches to CTLE design, based on RC degenerated common-source amplifiers, suffer from a limited bandwidth and consequently insufficient peaking at high frequencies. When CTLEs are cascaded the reduction in overall bandwidth due to repeated real poles follows the same trend as that of 1st-order gain cells. Further, a 1st-order CTLE stage has a limited capability in equalizing a second-order TIA [6,12] which necessitates cascading several equalizer stages, further increasing power and area overheads. On the other hand, various inductorless feedback techniques can be used to design main amplifiers with gain-bandwidth products (GBW) far superior to a cascade of first-order stages [7–10]. The improvement is the result of poles moving away from the negative real axis. A combination of poles with high- and low-quality factors gives better GBW for the same pole magnitude. The proposed approach to design an EMA improves the overall

receiver performance by increasing the gain of the TIA and improving noise performance as argued [6], but with the wideband performance of state-of-the-art MA designs.

The proposed design technique requires co-designing the TIA and the subsequent equalizing amplifier. Therefore, both stages receive equal attention in the analysis. Section 2 in this paper provides a detailed analysis of the TIA, highlighting the trade-off between its gain and bandwidth. Section 3 introduces the concept and the block diagram of the proposed EMA. The performance of the overall FE (TIA/EMA) is studied in Section 4. Section 5 shows the circuitry and simulation results of the proposed FE in comparison to the conventional full bandwidth design. Finally, Section 6 concludes the work.

2. Transimpedance Amplifier

2.1. Small-Signal Model and Freuqency Response

The inverter-based TIA (Inv-TIA) is used in this work due to its superior noise performance over its common-gate (CG) counterpart. Further, unlike the CG-TIA, the Inv-TIA is a self-biased topology which decouples the gain from the transconductance of the input device and allows for performance optimization without being limited by DC biasing constraints. The circuitry and the small-signal model of the Inv-TIA are shown in Figure 2. The CMOS inverter is modeled by its total transconductance g_m and output resistance R_A. Therefore, the core voltage amplifier has an open-loop transfer function of $A_{core}(s) = -A_0/(1+sT_A)$, where $A_0 = g_m R_A$ is the DC voltage gain and T_A is the time-constant formed by the output resistance R_A and the total output capacitance C_L. In the model, C_T is the total input capacitance, including both the photodiode capacitance C_D and the circuit's input capacitance C_I. Considering this model, the Inv-TIA exhibits a second-order transfer function characterized by a natural oscillation frequency ω_0, a pole quality factor Q_0, and a midband transimpedance gain of $Z_{TIA,0} \cong R_F$ [13]. The natural oscillation frequency ω_0 is converted to the corresponding TIA's 3dB-bandwdith (f_{TIA}) through a coefficient ρ that depends on the shape of the TIA's amplitude response (i.e., ρ is a function of Q_0). Detailed expressions for ω_0, Q_0, and ρ can be found in [14].

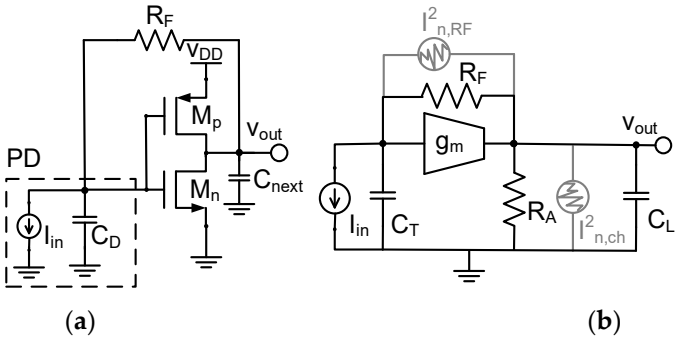

Figure 2. Inverter-based TIA (**a**) circuit and (**b**) small-signal model with noise sources indicated.

In the Inv-TIA, A_0 is constant for a given biasing condition, fixed ratio of W_p/W_n, and technology node. For example, an inverter with $V_{DD} = 1$ V, $W_n = W_p$, and simulated in TSMC 65 nm CMOS technology achieves A_0 of 6 V/V. Further, the gain-bandwidth product of the core amplifier $(GBW_A = A_0/(2\pi T_A))$ is also constant. The circuit's input capacitance (C_I) is determined by the total transistor width and is usually chosen as a fraction of the photodiode capacitance based on the noise and power constraints [14]. Therefore, for a given C_D, once C_I is fixed, the TIA's performance is controllable only through the feedback resistor. In this work, unless mentioned otherwise, A_0, GBW_A, and C_T are set to 6 V/V, 75 GHz, and 200 fF, respectively.

Figure 3a shows that both the 3 dB bandwidth and the pole quality factor Q_0 decrease with larger feedback resistor R_F. The bandwidth degrades almost linearly with the feedback resistor. In fact, the bandwidth does not follow the square-law relation

$\left(R_F \propto f_{TIA}^{-2}\right)$ predicted by the Transimpedance Limit [13]. This discrepancy can be explained as follows: Unlike [13], the model in this work allows Q_0 to change with R_F $\left(Q_0 = \sqrt{(A_0+1)R_F C_T T_A}/(R_F C_T + T_A)\right)$. For sufficiently large R_F that makes $R_F C_T \gg T_A$, Q_0 is proportional to $R_F^{-0.5}$. Consequently, it is reasonable to assume that ρ is also proportional to $R_F^{-0.5}$ with a percentage error of less than $\pm 8\%$, as shown in Figure 3b. Using this relation to rearrange the transimpedance limit from [13]:

$$f_{TIA}^2 = \frac{(A_0+1)}{A_0}\frac{GBW_A\,\rho^2}{2\pi R_F C_T} \tag{1a}$$

which implies:

$$f_{TIA}^2 \sim \frac{1}{R_F^2} \rightarrow f_{TIA} \sim \frac{1}{R_F} \tag{1b}$$

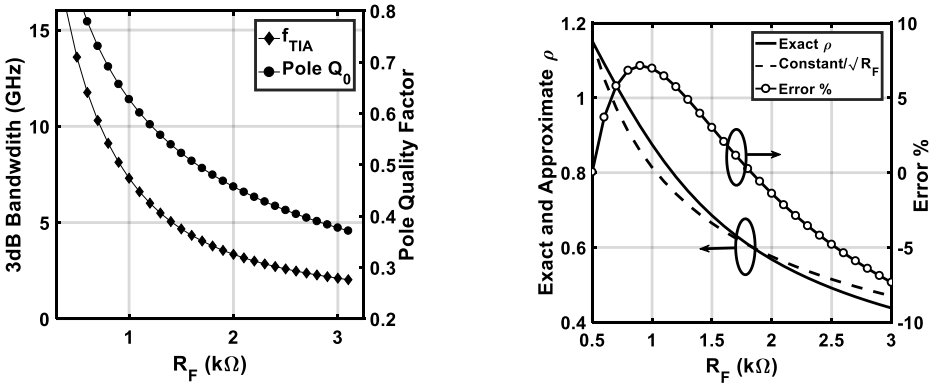

Figure 3. (**a**) TIA's 3dB bandwidth and pole Q_0 as a function of the feedback resistor. (**b**) The exact and the approximate calculations of ρ as a function of the feedback resistor along with the difference between the two as a percentage error.

This means that changing R_F changes both the pole magnitude (ω_0) and the pole quality factor (Q_0) which modifies the bandwidth dependency on the feedback resistor from that given in [13] where Q_0 is assumed to be constant. Assuming a constant Q_0 when R_F is increased by a factor of r requires both A_0 and T_A to scale up by a factor of $\sqrt{r}$. Practically, this approach is not feasible since the voltage gain of a single-stage CMOS inverter is constant for a given biasing and its maximum value is limited by the technology node.

2.2. Effective Gain

When f_{TIA} is reduced far below f_{bit}, severe ISI is introduced to the extent that the output eye diagram is fully closed. Therefore, the DC value of $Z_{TIA}(s)$ becomes a deceptive measure of the gain. The effective gain must be calculated from the transient response; more precisely, from the pulse response [15]. The TIA's pulse response is the response to an isolated binary one transmitted in a long sequence of binary zeros. Assuming a linear time-invariant (LTI) operation, if the TIA's response to a step input with a peak-to-peak value of i_{pp} is defined as $x(t)$, then its pulse response is calculated as $y(t) = x(t) - x(t - UI)$, where UI is the unit interval. The output pulse response of the Inv-TIA is plotted in Figure 4a for a data rate of 10 Gb/s with $i_{pp} = 10\ \mu A_{pp}$ and a bandwidth ranging from $0.2f_{bit}$ to $0.6f_{bit}$. To quantify the ISI, $y(t)$ is sampled at the symbol rate relative to its peak (as shown by the marker points in Figure 4a), resulting in a discrete-time sequence $V_{h,n}$ given by:

$$V_{h,n} = y(nT_b) \qquad -\infty < n < \infty \tag{2}$$

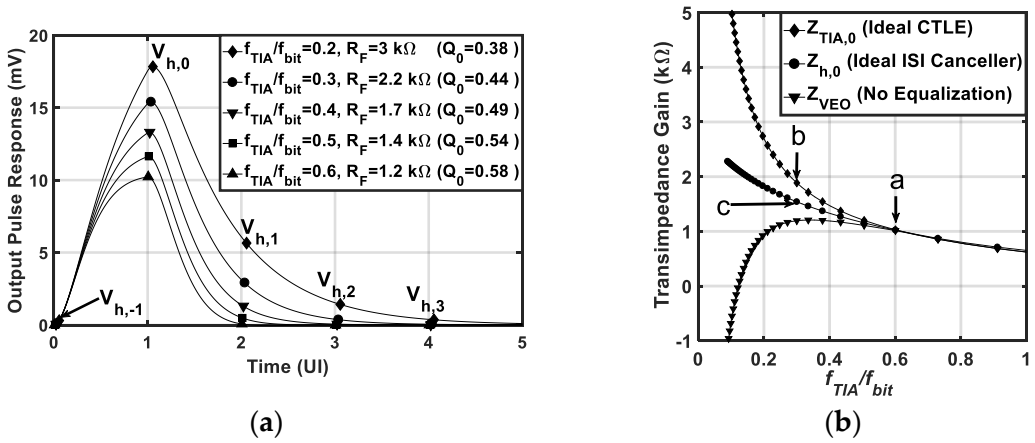

Figure 4. (**a**) Output pulse response for various values of f_{TIA}/f_{bit}. The input current pulse has a peak-to-peak value of 10 μA_{pp} and a unit interval of 100 ps. (**b**) Different gains as a function of f_{TIA}/f_{bit}. f_{bit} are fixed at 10 Gb/s while f_{TIA} is swept by varying R_F. The labeled points in (**b**) illustrate that linear equalization is favorable for applications that require high gain in the receiver FE.

The sample at the peak of the pulse is denoted as the main-cursor sample $(V_{h,0})$. An effective gain of $Z_{h,0}$ can be interpreted as $V_{h,0}/i_{pp}$ if all ISI is cancelled. In the absence of equalization, the ISI samples $(V_{h,n\neq 0})$ can be subtracted from $V_{h,0}$, closing the vertical eye opening (VEO) to:

$$VEO = V_{h,0} - \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \left|V_{h,n}\right| \tag{3}$$

The effective gain is calculated based on the receiver architecture as follows: 1. The VEO can be used to determine an effective gain of $Z_{VEO} = VEO/i_{pp}$ for the case in which the ISI is not removed or is only partially removed. The midband gain $Z_{TIA,0}$ can also be interpreted as an effective gain if an ideal unity-gain continuous-time linear equalizer (CTLE) is employed. The CTLE compensates for the bandwidth limitation of the TIA and restores an overall bandwidth on the order of $0.6f_{bit}$ without impairing the low-frequency gain. Therefore, the TIA's midband gain $Z_{TIA,0}$ at the low bandwidth point can be used as the effective gain for the combined (TIA/CTLE).

Figure 4b shows that linear equalization improves the effective gain over both full-bandwidth and ISI canceller-based designs. For example, if the TIA's bandwidth is reduced from $0.6f_{bit}$ (point a) to $0.3f_{bit}$ and an ideal CTLE is employed (point b), the effective gain improves by a factor of 1.86× compared to point a. The gain at $0.3f_{bit}$ (point b) is also 1.23× larger than that where an ideal ISI-canceller is employed (point c). That is, ISI cancellers have no bearing on the TIA's bandwidth which means that the output pulse of a limited-bandwidth TIA does not have enough time to settle at the voltage value $(i_{pp}Z_{TIA,0})$. Further, ideal cancelers that remove all pre- and post-cursor ISI are not implementable. For example, decision feedback equalizers (DFEs) [12] cancel only the post-cursor ISI. DFEs also suffer from a tight timing constraint where the feedback signal from the previously decided bit must arrive within one unit interval (UI) to resolve the current bit. These limitations make linear equalization a more attractive choice for applications that require high gain in the receiver FE. DFEs, on the other hand, are favorable over CTLEs from the noise point of view. That is, CTLEs extend the noise bandwidth to be a function of the bandwidth of the combined TIA/CTLE instead of being a function of the bandwidth of the low-bandwidth TIA as in the DFE-based receivers [15]. Therefore, a fair comparison between different receiver architectures should consider more complete figures of merit, such as OMA sensitivity and energy efficiency. The noise performance of the presented front-end is carefully examined in Section 4.3 in the presence of the equalizing main amplifier.

3. Equalizing Main Amplifier

In addition to high-gain and broadband operation, adjustable high-frequency peaking (HFP) is a desirable feature in MA design. The amplitude peaking at the Nyquist frequency can mitigate the bandwidth limitation introduced by other components in the optical link. For example, in [16], shunt and series passive inductors are employed between cascaded stages of a programmable gain amplifier to realize an HFP. The HFP is then used to partially compensate for the varying performance of the multi-mode fiber. In this work, passive inductors are avoided because they consume significant silicon area and potentially increase substrate coupling. The HFP is realized by introducing a pole in the feedback loop of an active feedback-based MA architecture and used to compensate for the TIA's limited bandwidth.

Equalizing MA Based on a Third-Order Gain Stage

The block diagrams of the conventional and proposed gain stages are shown in Figure 5a,b, respectively. The conventional architecture is presented in [17], where a third-order nested feedback technique achieves high-speed operation while maintaining robust stability compared to the traditional third-order gain stage. In the block diagram in Figure 5a, the first-order gain cell, $A(s)$, is modeled by the transconductance of the input device g_{m1}, load resistance R_1, and load capacitance C_1. The adjustable active feedback $\beta_{con}(s)$ cell is modeled by the transconductance $-g_{mf}$. Therefore, the transfer functions of the first-order gain and feedback cells are given by:

$$A(s) = \frac{A_1}{\frac{s}{\omega_1} + 1}, \qquad \beta_{con}(s) = \frac{\beta_1}{\frac{s}{\omega_1} + 1}, \tag{4}$$

where $A_1 = g_{m1}R_1$ and $\omega_1 = (R_1C_1)^{-1}$ are the DC gain and cut-off frequency of the first-order gain cell, respectively. $\beta_1 = g_{mf}R_1$ is the DC feedback gain. The transfer function of the overall architecture in Figure 5a is given by:

$$H_{MA}(s) = \frac{A^3(s)}{A^2(s)\beta_{con}(s) + A(s)\beta_{con}(s) + 1} \tag{5}$$

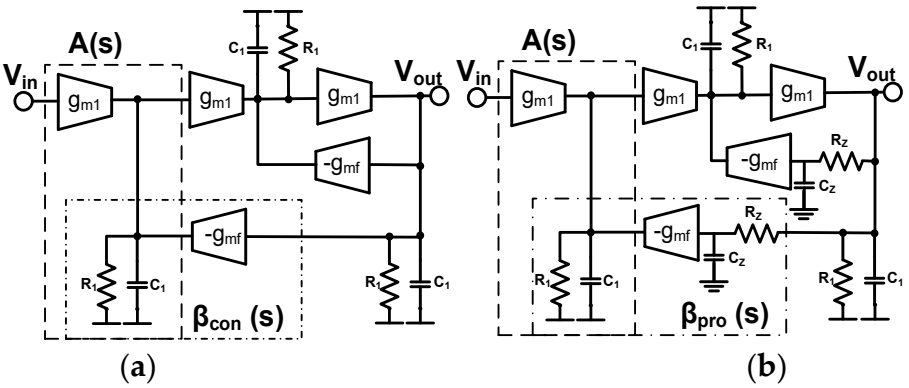

Figure 5. Block diagram of (**a**) the third-order gain stage in [17] (**b**) the proposed EMA with a LPF inserted in each feedback path.

In this work, two poles are introduced in the feedback loops to create an adjustable HFP without impairing the low-frequency gain. The transfer function of the proposed EMA is calculated using (5) by replacing $\beta_{con}(s)$ by β_{Pro} given in (6):

$$\beta_{pro}(s) = \frac{\beta_1}{\left(\frac{s}{\omega_1} + 1\right)\left(\frac{s}{\omega_Z} + 1\right)} \tag{6}$$

where $\omega_Z = (R_Z C_Z)^{-1}$ is the cut-off frequency of the introduced low-pass filter which is assumed to have negligible loading on the output node. Therefore, the transfer function of the EMA in Figure 5b is given by:

$$H_{EMA}(s) = \frac{A_1^3\left(\frac{s}{\omega_Z}+1\right)}{\left(\frac{s}{\omega_1}+1\right)^3\left(\frac{s}{\omega_Z}+1\right) + A_1\beta_1\left(\frac{s}{\omega_1}+1\right) + A_1^2\beta_1} \tag{7}$$

The pole-zero locations of (7) are plotted in Figure 6a in comparison with that of (5) for β_1, A_1, and ω_1, fixed at 0.25, 2.5, and $2\pi \times 30$ GHz, respectively. The poles of the conventional architecture are indicated by black x-markers. For the proposed EMA, ω_Z is swept from $0.5\omega_1$ to $5\omega_1$. The insertion of the LPF in the feedback loops of the proposed EMA creates a real zero at ω_Z (shown in blue). It also increases the order of the denominators of $\beta_{pro}(s)$ and $H_{EMA}(s)$ compared to their conventional counterparts. As a result, for low values of ω_Z, the proposed EMA has two sets of complex-conjugate poles (P_A and P_B) (shown in red). As ω_Z increases, P_A travels toward the complex poles of (5) while the damping factor of P_B increases until the two poles become real and start traveling in opposite directions. At sufficiently high ω_Z, P_{B2} and the real zero cancel each other, P_{B1} reaches the real pole of (5) and the overall architecture degenerates to the third-order gain stage in [17].

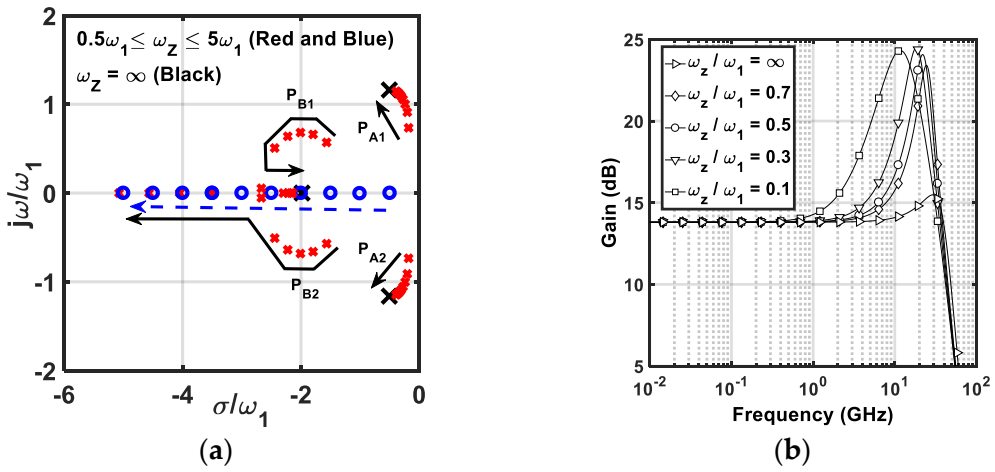

Figure 6. (**a**) Pole-zero locations of the proposed EMA for various values of ω_Z in comparison to the conventional third-order gain stage where $\omega_Z = \infty$. The dashed arrows indicate the direction of pole-zero movements as ω_Z increases (**b**) amplitude response of the proposed EMA for various ratios of ω_Z/ω_1. β_1, A_1, and ω_1 are fixed at 0.25, 2.5, and $2\pi \times 30$ GHz, respectively.

The impact of varying ω_Z on the amplitude response of the proposed EMA is depicted in Figure 6b. For a given β_1, HFP can be introduced independent from the low-frequency gain. The peak of the amplitude response moves to a lower frequency as ω_Z is reduced. As a numerical example from Figure 6b, for $\omega_Z = 0.1\omega_1$, the EMA achieves amplitude peaking of 6 dB at 5 GHz and increases to 10.5 dB at 11 GHz. In the presence of such high amplitude peaking, it is not instructive to explore the bandwidth of the EMA. Instead, the bandwidth extension ratio and the signal integrity are inspected in the following section for the overall front-end which includes the limited-bandwidth TIA and the EMA.

4. Front-End Performance Analysis

4.1. Performance Requirements for the EMA

The noise-limited input signal produces a peak-to-peak voltage of $V_O^{PP} = SNR\ i_{n,in}^{rms}\ Z_{TIA,0}\ A_{EMA,0}$ at the output of the front-end, assuming that the EMA restores a wide overall bandwidth, where SNR is the required signal-to-noise ratio and is

equal to 14.07 for a BER of 10^{-12} [4], $i_{n,in}^{rms}$ is the input-referred noise current, and $A_{EMA,0}$ is the DC gain of the EMA. V_O^{PP} is sufficiently large to drive an ideal clock-and-data recovery (CDR) circuit to achieve the desired BER. However, the decision circuit in a realistic CDR has finite sensitivity and requires a minimum input voltage amplitude $\left(V_{CDR}^{PP}\right)$. Therefore, the FE's output voltage needs to be increased by V_{CDR}^{PP} to attain the same BER as an ideal CDR. The finite sensitivity of the CDR incurs a power penalty (PP) of:

$$PP = \frac{V_O^{PP} + V_{CDR}^{PP}}{V_O^{PP}} = 1 + \frac{V_{CDR}^{PP}}{SNR\, i_{n,in}^{rms}\, Z_{TIA,0}\, A_{EMA,0}} \tag{8}$$

The optical power incident to the photodiode, the electrical current generated from the photodiode, and the voltage produced at the output of the main amplifier are linearly proportional. As a result, the amount of additional optical power required to overcome any nonideality (power penalty) can be expressed in voltage terms as shown in (8). The equation reveals that higher transimpedance gain relaxes the gain requirements for the EMA for a given PP. Figure 4b shown earlier indicates that reducing the ratio f_{TIA}/f_{bit} is beneficial for the gain as long as the equalizer is able to recover an overall bandwidth of approximately 50% to 60% of the targeted data rate. Therefore, the equalizer's capability in restoring the bandwidth determines how far the TIA's bandwidth can be reduced below the data rate. That is, excessive reduction of the TIA's bandwidth would require the equalizer to introduce a large amount of amplitude peaking which translates into large group delay variation (GDV). The latter causes horizontal and vertical eye closure which reduces the gain and noise improvements gained from equalization. In [6], it is concluded that the equalizer can restore the bandwidth by a factor of approximately 2× while simultaneously maintaining a good noise performance and a good quality of the equalized eye diagram.

For the conventional wideband TIA, a feedback resistor of 1.25 kΩ is chosen to achieve a bandwidth of $0.57f_{bit}$, sufficiently large to introduce no ISI. The TIA's bandwidth drops almost linearly with R_F as observed in Figure 3a. Therefore, in the proposed design, the value of the feedback resistor is doubled, leading to a bandwidth of $0.26f_{bit}$. At this bandwidth, the TIA achieves a $Z_{TIA,0}$ of 66.6 dBΩ (2143 Ω) while introducing an attenuation of 7.2 dB at the Nyquist frequency ($f_N = 0.5f_{bit} = 5$ GHz). The EMA is now required to recover the bandwidth by a factor ranging from 1.9× to 2.3× to achieve an overall bandwidth on the order of 50% to 60% of f_{bit}. For example, using the gain of the low-bandwidth TIA while assuming V_{CDR}^{PP}, SNR, and $i_{n,in}^{rms}$ of 50 mV_{pp}, 14.07, and 1 μA_{rms}, respectively, the PP defined in (8) can be used to calculate the required gain of the EMA. In addition to recovering the bandwidth, the EMA is required to amplify the TIA's output by a low-frequency gain of approximately 20 dB to reduce the PP to less than 0.67 dB (1.17). Practically, the EMA's gain is determined to reduce the PP to a pre-determined value obtained from link budget analysis.

4.2. Bandwidth Extension and Signal Integrity

Figure 7 shows the block diagram of the proposed front-end where the limited-bandwidth TIA is followed by a two-stage EMA. The EMA's second stage is added to relax the gain requirements. The two-stage EMA is modified based on the two-stage MA presented in [10] by inserting low pass filters in the feedback loops of the second stage. Therefore, the transfer function of the overall front-end (FE) is given by $Z_{FE}(s) = Z_{TIA}(s)H_{2-EMA}(s)$, where $H_{2-EMA}(s)$ is the transfer function of the two-stage EMA and given by:

$$H_{2-EMA}(s) = \frac{A^5(s)}{Den(s)} \tag{9}$$

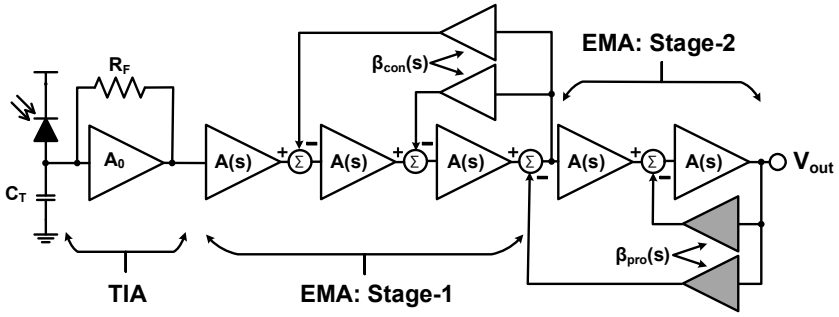

Figure 7. Block diagram of the proposed front-end. The two-stage EMA is modified based on the two-stage MA in [10]. The grayed feedback cells indicate the locations of the inserted poles.

The denominator $Den(s)$ is expressed as:

$$Den(s) = 1 + A(s)\left[\beta_{con}(s) + \beta_{pro}(s)\right] + A^2(s)\left[\beta_{con}(s) + \beta_{pro}(s) + \beta_{con}(s)\beta_{pro}(s)\right] + A^3(s)\beta_{con}(s)\beta_{pro}(s) \tag{10}$$

Once the TIA's feedback resistor is fixed, the full design space is reduced to only two variables: ω_Z and β_1. These two variables are swept, and the following equations are solved numerically to calculate the bandwidth (f_{FE}), the low-frequency gain $(Z_{FE,0})$, and the peaking (M_p) of the overall FE:

$$|Z_{FE}(2\pi f_{FE})| = \frac{1}{\sqrt{2}}|Z_{FE}(j\omega)|_{\omega=0} \tag{11a}$$

$$Z_{FE,0} = 20\log_{10}|Z_{FE}(j\omega)|_{\omega=0} \tag{11b}$$

$$M_P = 20\log_{10}\frac{\max(|Z_{FE}(j\omega)|)}{|Z_{FE}(j\omega)|_{\omega=0}} \tag{11c}$$

Several combinations of β_1 and ω_z can achieve the required bandwidth extension but with different noise performance. The noise analysis is presented in the following section. The feedback gain β_1 directly impacts the low-frequency gain of the EMA and is chosen to satisfy the power penalty condition indicated earlier. Then, ω_z is swept to achieve the required bandwidth extension ratio defined as f_{FE}/f_{TIA}. The pairing of $\omega_z = 0.075\omega_1$ and $\beta_1 = 0.25$ is chosen as it achieves a good noise performance as well as a good quality of the output eye. The corresponding frequency response is plotted in Figure 8a, where the EMA introduces 5 dB of peaking and extends the bandwidth by a factor of 2.2×. The gain peaking in the overall frequency response is less than 0.1 dB. Figure 8b shows the pulse response at the output of the FE. To quantify the vertical and horizontal eye openings, the output pulse is sampled at a bit rate clock relative to its peak. The pulse is sampled at both the rising and falling edges of the clock. The sum of the magnitude of the samples at the even clock edges (filled markers for $n \neq 0$) quantifies the ISI. The sum of the samples at the odd clock edges (hollow markers) is considered as a jitter indicator (JI). Note that the falling edges of the clock are the zero-crossing points of the data. Therefore, the defined JI includes only the deterministic jitter caused by the residual ISI or ringing in the time domain [18]. The sum of ISI and JI samples is less than 6.5% of the main cursor sample which implies that the eye has a wide internal opening area, as evident also from the eye diagram in Figure 9a, obtained through simulation. Figure 9b shows the output eye diagram when the limited bandwidth TIA is followed by a wideband MA. The comparison between the two eyes in Figure 9 demonstrates the capability of the presented technique in restoring the bandwidth without impairing the midband gain or increasing power dissipation.

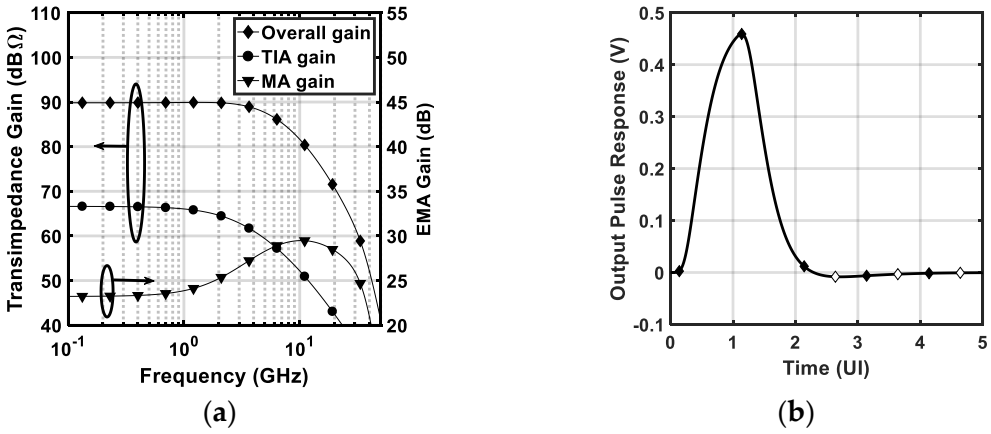

Figure 8. (**a**) Amplitude response (**b**) output response to an input current pulse with peak-to-peak value of 15 μA_{pp} and width of 100 *ps*. The EMA parameters are $\omega_Z/\omega_1 = 0.075$ and $\beta_1 = 0.25$.

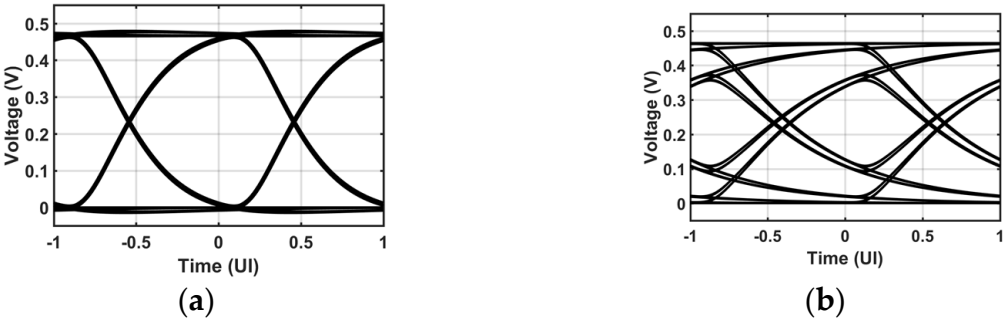

Figure 9. Matlab generated 10 Gb/s output eye diagrams when the limited-bandwidth TIA is followed by (**a**) an EMA, and (**b**) a wideband MA. The peak-to-peak value of the input current is fixed at 15 μA_{pp}.

4.3. Noise Analysis

Figure 10a shows the model used for noise analysis. The main noise sources in the Inv-TIA are the channel and feedback thermal noise, shown in Figures 2 and 10 as $I^2_{n,ch}$ and $I^2_{n,RF}$, respectively. The power spectral densities of these two sources can be expressed as: $I^2_{n,ch} = 4kT\gamma g_m$ and $I^2_{n,RF} = 4kT/R_F$ where k is the Boltzmann constant, T is the temperature in Kelvin, and γ is the excess noise factor. Under a constant gain-bandwidth product constraint, the noise-optimum FET size is $C_I = 0.7C_D$ [14]. Therefore, the transconductance of the TIA's input device can be calculated as $g_m = 2\pi f_T C_I$, where f_T is the technology transit frequency at the selected bias point. In Figure 10a, the amplifier following the TIA is modeled by $H_{post}(s)$ and its input-referred noise PSD is denoted by $V^2_{n,in} = 4kT/g_{m,post}$. $H_{post}(s)$ is given by (9) and (10) for both the proposed and conventional designs, using $\beta_{pro}(s)$ and $\beta_{con}(s)$, respectively. In simulations that follow, $g_{m,post}$, γ, and f_T are fixed at 10 $m\Omega^{-1}$, 2, and 150 GHz, respectively.

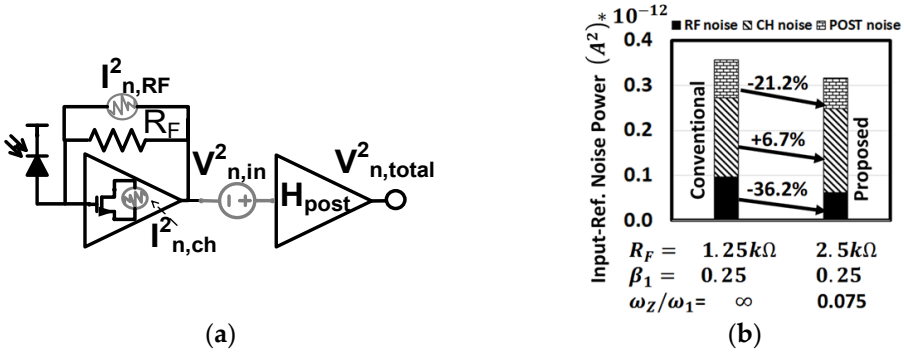

Figure 10. (**a**) Circuit model used for noise analysis (**b**) Matlab simulated noise reduction in the proposed FE compared to its conventional counterparts. The arrows indicate the amount of change for each noise component.

Linear equalization extends both the signal and the noise bandwidths [15]. Therefore, the integration of the noise power spectral density (PSD) must be performed at the receiver output to take into consideration how the equalizer processes the noise. To do so, the contribution to the output noise PSD from each noise source is first calculated. Because all noise sources are uncorrelated, the total output noise PSD is constructed by adding up all individual power spectra. The total output noise PSD is then integrated up to infinity to calculate the integrated output-referred noise power $\left(v^2_{n,total}\right)$ having units of V^2. The total integrated input-referred noise power $\left(i^2_{n,total}\right)$ in units of A^2 is then determined by dividing the $v^2_{n,total}$ by the squared effective gain $\left(Z_{TIA,eff}\right)^2$ calculated from the VEO at the output of the FE. This gain calculation accounts for the residual ISI in the signal presented to the decision circuit. The input-referred noise current is then calculated as the square root of $i^2_{n,total}$. Further discussion about the noise analysis for equalizer-based optical receivers is available in our previously published work [15].

4.4. Performance Comparison

To assess the improvement of the proposed FE versus its conventional counterpart, both FEs are simulated in Matlab. The traditional FE has the same block diagram as in Figure 7 without the pole insertion in the feedback loops. Therefore, its analysis is the same as presented earlier, but replacing each $\beta_{pro}(s)$ in (10) with $\beta_{con}(s)$. The value of the TIA's feedback resistor is tuned to set the ratio of f_{TIA}/f_{bit} to 0.57 and 0.26 for the conventional and the proposed FEs, respectively. In the latter, the values of β_1 and ω_Z are chosen to achieve an overall bandwidth of $f_{FE} = 0.56 f_{bit}$. The power consumption and the DC gain of the proposed EMA are kept equal to that of the conventional MA by fixing the values of A_1 and β_1 in both circuits. The performance of the two FEs is summarized in Table 1. Although the two FEs have approximately the same overall bandwidth, the proposed FE achieves 6 dB higher gain compared to its conventional version. This improvement in the transimpedance gain resulted from the increased value of R_F for the limited-bandwidth TIA. It is worth mentioning that this gain improvement comes without any additional power dissipation because changing R_F and ω_Z does not affect the DC power dissipation as will be shown in the practical implementation in the next section.

Table 1. Design parameters and performance summary of the proposed front-end in comparison to its conventional counterpart.

		MATLAB [1]		Spectre [2]			
		10 Gb/s		10 Gb/s		20 Gb/s [4]	
		Conventional	Proposed	Conventional	Proposed	Conventional	Proposed
TIA	R_F (kΩ)	1.25	2.5	0.7	1.6	0.4	0.8
	f_{TIA}/f_{bit}	0.57	0.26	0.64	0.27	0.68	0.3
MA/EMA	$\omega_Z/2\pi$ (GHz)	∞	2.25	∞	**5.25**	∞	**11.47**
	β_1	0.25	0.25	**0.14**	**0.14**	**0.15**	**0.15**
	Peaking (dB) @ f_N	0	5.05	0	4.8	0	3.5
FE	Z_{VEO} (dBΩ)	**83.6**	**89.98**	**79.7**	**87.1**	**71.2**	**77.2**
	f_{FE}/f_{bit}	0.57	0.56	0.6	0.61	0.59	0.54
	Peaking (dB)	0	0.084	0	0	0	0
	$i_{n,rms}$ (μA$_{rms}$)	**0.598**	**0.531**	**1.2**	**0.95**	**2.41**	**1.74**
Sensitivity Improvement (dB)							
	Noise-based	–	**0.52**	–	**1**	–	**1.4**
	PP-based [3]	–	**0.61**	–	**0.5**	–	**0.84**
	Total	–	**1.125**	–	**1.5**	–	**2.24**

[1] Simulations based on Figure 7. [2] Simulations based on Figure 11a. [3] For V_{CDR}^{PP} = 50 mV$_{pp}$. [4] The 20 Gb/s simulations are discussed in Section 5.4.

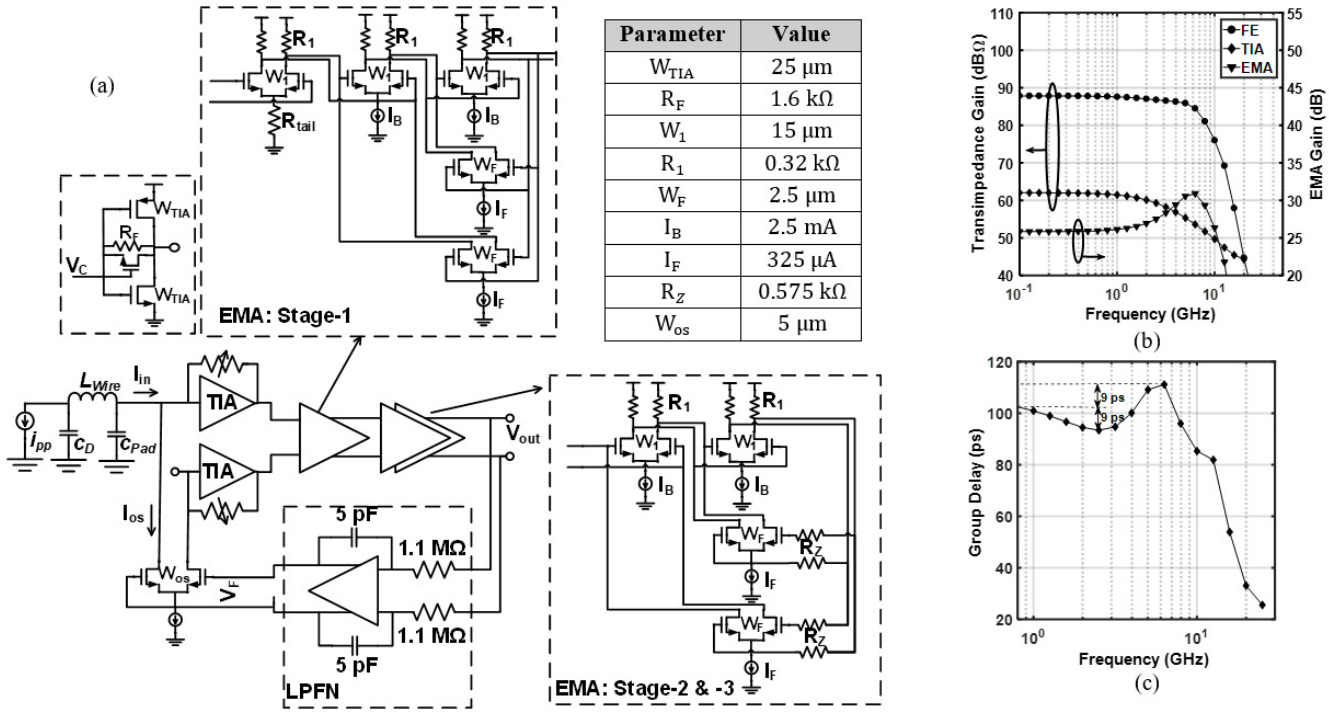

Figure 11. (**a**) Block diagram and circuitry of the implemented front-end. Parameter values for 10 Gb/s operation are tabulated. (**b**) Simulated amplitude response. (**c**) Simulated group-delay.

The input-referred noise power of both FEs is compared in Figure 10b. In the proposed FE, the feedback resistor and the post amplifier noise powers are improved compared to their counterparts in the conventional design. That is, increasing the value of R_F in the

proposed FE reduces its thermal noise contribution and increases the input-referral gain which suppresses the noise from the follow-on amplifier. The channel noise is slightly increased in the proposed FE due to HFP that amplifies the high-frequency noise. Overall, the presented design technique reduces the input-referred noise current by 11.2%. The lower noise and higher gain in the presented FE led to 0.52 dB and 0.61 dB improvements in the noise-based sensitivity and the PP compared to the traditional design.

5. Circuitry and Layout of the Implemented Front-End

Figure 11a shows the block diagram and the circuitry of the implemented front-end. A replica TIA is used to provide pseudodifferential power-supply noise rejection. The TIA is followed by a three-stage EMA. A series resistor (R_Z) is inserted in the feedback loops of the second and third stages. This resistor, in combination with the parasitic capacitance of the transistor in the feedback loops, creates the zero required for bandwidth extension. Compared to Figure 7, the EMA's third stage is added to relax the gain requirements and assist in recovering the bandwidth. A low-pass feedback network (LPFN) is connected between the output of the EMA and the input of the TIA. The LPFN amplifies the difference between the DC levels at V_{Out} and returns a feedback voltage of V_F that is then converted to a current I_{os} by the transconductance of M_{os} and subtracted from the input current for offset compensation. The LPFN is a single-pole RC filter using a Miller-boosted 5 pF capacitor and a 1.1 MΩ resistor. A low cut-off frequency of 1 MHz is achieved as a trade-off between the on-chip area and the tolerable baseline wander for long runs of consecutive identical digits. The low common-mode voltage at the TIA's output prevents the use of a tail current source for the first differential pair in the EMA's first stage and therefore a poly silicon resistor is used instead.

The FE is simulated in TSMC-65 nm using a Cadence Spectre simulator. The input parasitics are modeled by a pad capacitance (C_{Pad}) of 45 fF, a photodiode capacitance (C_D) of 80 fF and a bondwire inductance (L_{wire}) of 0.5 nH. The loading from the subsequent output buffer is modeled by a load capacitance of $(C_L = 150$ fF$)$ connected at the output of the EMA. An additional 50 fF capacitance is added to all nodes to model the wiring and layout parasitic. The receiver's output stage (not shown in Figure 11a) is a conventional differential amplifier with a load resistance of 100 Ω chosen as a trade-off between output signal amplitude and compatibility with the off-chip 50 Ω environment.

Figure 12 shows the chip layout in TSMC 65 nm CMOS technology. The chip includes two standalone FEs. One FE is the direct implementation of the circuit in Figure 11a while the other is its conventional version (i.e., R_Z is replaced by a short circuit). The total size of the chip is 1 mm × 0.7 mm. Each front-end is pad limited and occupies 665 µm × 460 µm $(0.31$ mm$^2)$, including the I/O RF pads, while the active area, including the offset compensation loop, is about 0.0114 mm^2. The high-speed RF input and output probing pads are differential G-S-G-S-G since each FE has differential inputs and outputs. The TIA, the MA/EMA, and the output buffer are powered by different supplies.

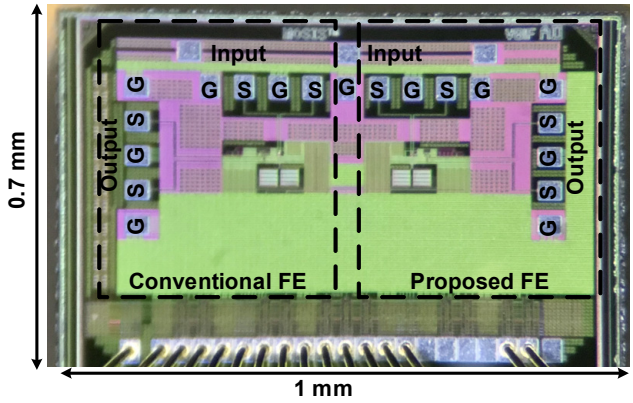

Figure 12. Chip layout.

5.1. Validation of Bandwidth Extension

Similar to the previous section, both the proposed and the conventional FEs are simulated and compared. The proposed FE's TIA bandwidth is 27% of the targeted 10 Gb/s data rate. The tail current source in the feedback pair I_F sets the feedback gain β_1 and is chosen to satisfy the power penalty condition. The series resistor R_Z is then chosen to achieve the required bandwidth extension. The device dimensions and component values are tabulated in Figure 11a for nominal 10 Gb/s operation. All transistors in the signal and feedback paths use minimum length. Current sources, however, employ transistors with longer than minimum length. The corresponding amplitude responses are shown in Figure 11b. The EMA introduces a peaking of 4.8 dB at the Nyquist frequency and restores the bandwidth by a factor of 2.28×, achieving an overall bandwidth of 6.1 GHz.

The simulated group-delay is also shown in Figure 11c where the GDV is within ±10% of the unit interval over the frequency range of interest. Figure 13a,b shows the 10 Gb/s eye diagrams at the output of the FE when the limited-bandwidth TIA is followed by a wideband MA or by the EMA, respectively. The eye diagrams obtained through simulation demonstrate the capability of the proposed peaking technique in restoring the bandwidth without impairing the low-frequency gain. The bandwidth extension improves the VEO by a factor of 1.7×. Figure 13c shows the eye diagram of the traditional FE. In this simulation, R_Z is shorted and R_F is reduced to widen the TIA's bandwidth while the current sources (I_F and I_B) are unchanged. Comparing Figure 13b,c shows that the presented design technique improves the effective gain by a factor of 2.34×. Interestingly, for the proposed design, the gain is improved by almost the same amount as the TIA's bandwidth is reduced. This emphasizes the linear relation between the gain and the bandwidth in the single-stage Inv-TIA. Table 1 summarizes the simulated performance of the two FEs where the presented FE shows 1.5 dB better sensitivity compared to its conventionally designed counterpart.

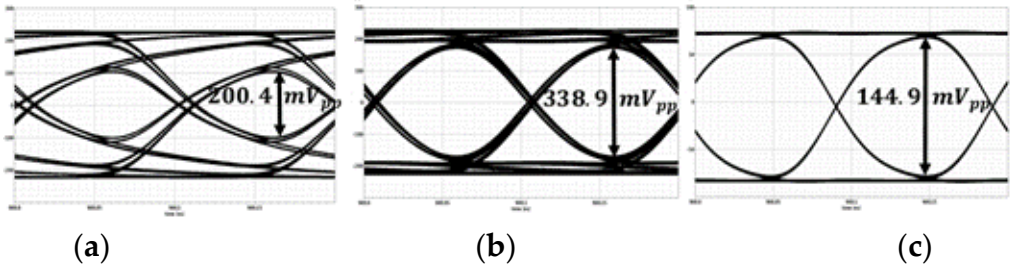

Figure 13. Simulation results for the 10 Gb/s output eye diagrams when the limited-bandwidth TIA is followed by (**a**) a wideband MA and (**b**) the proposed EMA. In (**c**), the TIA's bandwidth is widened, and a wideband MA is employed. The input current is fixed at 15 μA_{pp} for all simulations.

5.2. Sensitivity to Process and Temperature Variations

Figure 14 shows the simulated performance of the presented receiver under process and temperature variations. Figure 14a shows that the EMA exhibits more peaking at a lower temperature. For a given temperature, the peaking can vary by up to 6.5 dB over different process corners. The FE gain and bandwidth in Figure 14b can vary up to 13.5 dB and 3.4 GHz over different corners, respectively. The gain and bandwidth variations relative to their values at room temperature reach up to 24.3% and 22.5%, respectively, as the temperature varies from 20 °C to 80 °C. This performance variation is mainly caused by the constant current sources used in this design and can be counteracted by employing temperature-compensated or constant-*gm* biasing techniques [19]. Adaptation techniques can be also employed to continuously monitor the output eye diagram and set the circuit parameters accordingly to maintain the best quality for the equalized eye [20]. In the implemented prototype, the TIA's feedback resistor and current sources in the forward and feedback paths are made variable. This allows for post-fabrication control on peaking frequency, peaking magnitude, and the TIA's high-frequency roll-off. Therefore,

the amplitude responses of both the EMA and the TIA track each other to achieve the targeted bandwidth with minimal GDV.

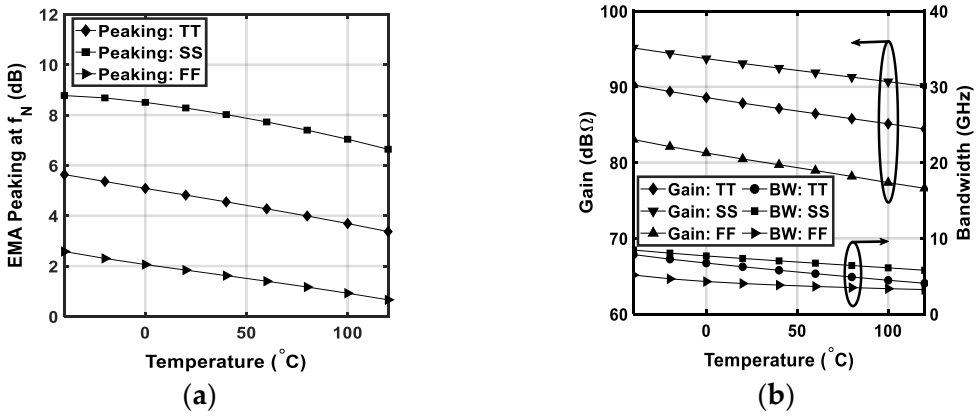

Figure 14. Simulated performance under process and temperature variations: (**a**) EMA's peaking at Nyquist frequency; (**b**) gain and bandwidth of the overall FE.

To prove that the proposed technique works despite the PT variations, Figure 15 shows the simulated 10 Gb/s eye diagram at the SS process corner and −20 °C. The uncompensated eye (left) shows a significant distortion. By carefully adjusting the circuit parameters, a clean eye is obtained (right) with an internal opening similar to that obtained under nominal operations. To generate the eye on the right, the circuit parameters are changed as follows: I_B is reduced from 2.5 mA to 1.65 mA, I_F is increased from 0.325 mA to 0.4 mA, and R_Z is reduced from 0.575 kΩ to 0.445 kΩ. The tunability range of all circuit parameters are limited to less than 35% of their nominal values which is feasible for realization. Further, the capacitance introduced by the configurable current sources appears at tail nodes and therefore does not alter the signal path.

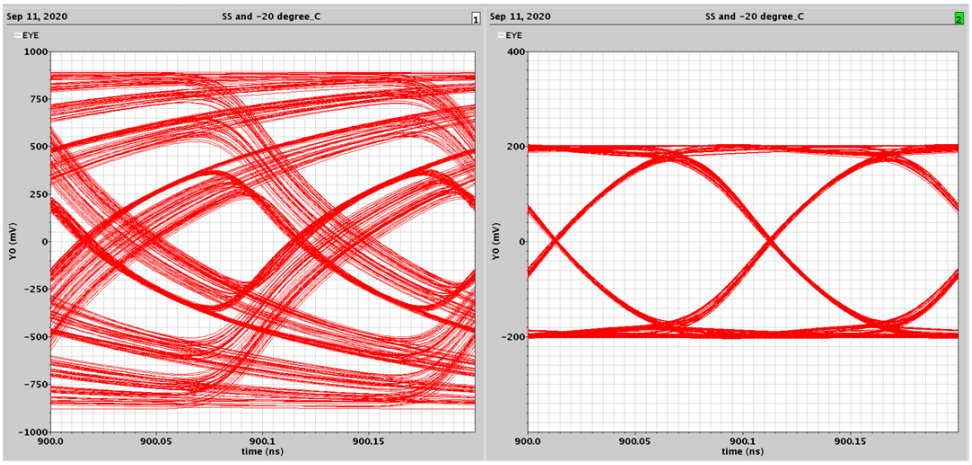

Figure 15. Simulated 10 Gb/s eye diagrams under SS process corner and −20 °C (**left**) uncompensated, (**right**) compensated.

5.3. Stability

In the presence of a complex feedback and high amplitude peaking in the EMA, the stability of the presented FE becomes an important consideration. The pole-zero simulation in Figure 6a shows that a pair of complex poles (P_A) moves toward the y-axis as ω_z is reduced. ω_z is the frequency of the introduced zero that ideally cancels the bandwidth-limiting pole created by the low-bandwidth TIA. As a result, the TIA's 3-dB bandwidth cannot be made arbitrarily small to avoid the EMA's pole pair travelling to the right-hand

plane (RHP). Further, for a given ω_z, the poles P_A may enter the RHP at excessively large feedback gain β_1. However, the values of β_1 that lead to RHP poles are far from those in the proposed design. For example, in the FE in Figure 7, when ω_z is set to $2\pi f_{bit}/4$, the poles P_A do not travel to the RHP until after $\beta_1 > 6$ and $\beta_1 > 5.5$ for f_{bit} of 10 Gb/s and 20 Gb/s, respectively, while β_1 is typically limited to less than 0.3.

5.4. Discussion and Comparison to Prior Work

The performance of the proposed FE is compared to other 10 Gb/s high-gain receivers in the literature as shown in Table 2. Although thorough circuit simulations are sufficient to prove the concept behind our design, the absence of optical measurements complicates the comparison with prior art. The work in [8] consists of an Inv-TIA followed by three stages of an Inv-based Cherry-Hooper voltage amplifier. In this architecture, active interleaving feedback and local positive feedback are applied to extend the bandwidth. The circuit is implemented in a single-ended structure and measured with electrical and optical inputs for various data rates. Only electrical measurements at 10 Gb/s are listed in Table 2. The work in [8] is measured for two modes of operation denoted on Table 2 by best sensitivity mode and lowest power mode (see Figure 18 in [8]). The average of these two modes shows approximately 2× better sensitivity and 2.3× better energy efficiency compared to the work presented here. The reason for this better performance is mainly because of the single-ended structure in [8] that reduces the power dissipation and thermal noise sources compared to the differential structure used in this work. Further, the single-ended implementation enabled measurements at low supply voltages, which are not available in this work due to the DC biasing requirements on differential amplifiers. The proposed design has a much higher output peak-to-peak amplitude at the sensitivity level than [8], which is not optimized for high-gain operation and incurs a significant PP when the receiver is followed by a practical decision circuit.

Table 2. Performance comparison with published 10 Gb/s receivers.

Performance Parameter	[9]	[12]	[8]		[21]	This Work [4]
			Lowest Power	Best Sens.		
RX topology	Diff.	Diff.	Sing.	Sing.	Diff.	Diff.
Passive inductor	No	No	No	No	Yes	No
CMOS tech. (nm)	130	65	65	65	40	65
f_T (GHz)	85	150	150	150	250	150
Data rate (Gb/s)	10	10	10	10	10	10
C_{PD} (fF)	NA	50	60 [2]	60 [2]	100 [1]	120
PRBS length	31	31	7	7	7	11
Sensitivity (μA_{pp})	–	13	–	–	23.9 [3]	24.4
Output voltage (mV_{pp})	175	400	15.85 [4]	53.55 [3]	136	339
Energy efficiency (pJ/b)	**18.9**	**2.3**	**0.6**	**1.6**	**7.5**	**2.4**

[1] On-chip capacitor is added to consider the effect of the PD junction capacitance. [2] Calculated from the average input-referred noise current. [3] Calculated from measured eye diagrams that are not shown in [8]. [4] Circuit simulation with parasitic capacitances taken into consideration.

The presented receiver shows better energy efficiency than [21] which is implemented in a more advanced technology node and a comparable energy efficiency to [12] which is implemented in the same technology. The combination of multistage shunt-feedback TIA and the noiseless DFE in [12] has resulted in an excellent sensitivity at the cost of more complexity and power dissipation on the equalizer that consumes 74% of the total power. Therefore, a design that incorporates the high-gain FE in [12] with our proposed equalization technique with no additional power dissipation could lead to significant

improvement on the energy-efficiency of the receiver while maintaining a good sensitivity. The work presented here shows comparable voltage sensitivity to the limiting amplifier introduced in [9], built by applying an active interleaving feedback to third-order gain cells. Finally, our work shows the largest output voltage amplitude for an input set to the sensitivity limit which makes it suitable to drive the subsequent clock and data recovery (CDR) circuit with negligible power penalty.

5.5. Operation at Higher Data Rate

The circuit in Figure 11a is also examined for 20 Gb/s operation with the same simulation setups described in Section 5.1 First, the TIA's bandwidth is set to 6 GHz (30% of the targeted data rate) by employing a feedback resistor of 800 Ω. Then, the limited-bandwidth TIA is followed by a wideband MA and the EMA, one at a time. Both amplifiers have the same value of I_B and I_f and therefore they consume the same DC power. The MA has a flat amplitude response with a bandwidth of 18.7 GHz. However, the overall bandwidth of the combined TIA/MA is dominated by the TIA's bandwidth. The EMA, on the other hand, introduces 3.5 dB of amplitude peaking at 10 GHz that extends the overall bandwidth of the combined TIA/EMA to 10.9 GHz. Figure 16a,b shows the simulation results for the output eye diagram for both scenarios. The internal eye opening improves by 1.6× when the EMA is employed compared to the case in which the wideband MA is used, demonstrating the capability of the presented technique in restoring the targeted bandwidth. The eye diagram in Figure 16c is obtained from the FE that includes TIA/MA after extending the TIA's bandwidth to 13.5 GHz by reducing its feedback resistor to 400 Ω, achieving an overall bandwidth of 11.8 GHz. Comparing Figure 16b,c) emphasizes that the presented design technique improves the effective gain compared to its conventional wide-bandwidth counterpart. The performance of the proposed FE at 20 Gb/s in comparison to its conventional counterpart is summarized in Table 1.

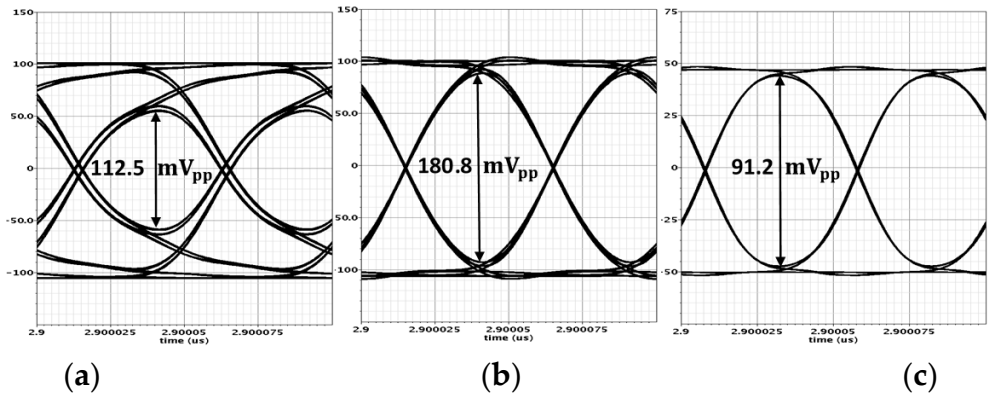

Figure 16. Simulation results for the 20 Gb/s output eye diagrams when the limited-bandwidth TIA is followed by (**a**) a wideband MA and (**b**) the proposed EMA (**b**). In (**c**), the TIA's bandwidth is widened, and a wideband MA is employed. The input current is fixed at 25 μA_{pp} for all simulations.

5.6. Operation with Large Input Signal

The presented analysis assumes that the gain cells are in linear operation. In reality, the circuit performance is strongly affected by the signal amplitude. As the signal propagates through cascaded stages, the latter gain cells start to saturate as a result of the increased voltage swing. Eventually, these cells act as unity-gain buffers and consequently the loop-gain falls below unity due to the presence of the active feedback. This in turn reduces the bandwidth. The impact of large input levels on the bandwidth of the active feedback-based structure is observed in [9] and an inverse scaling technique [22] is proposed as a potential solution for the problem. However, inverse scaling complicates the system analysis especially in the presence of interleaving feedback.

Alternatively, a straightforward automatic gain control similar to that presented in [6] can be employed. The technique has three steps: (1) aggressively reducing the TIA's gain at the cost of introducing a severe peaking in its amplitude response; (2) re-configure one of the MA stages to act as a low-pass filter to suppress the TIA's peaking and set the receiver bandwidth; (3) increasing the transconductance of the active feedback cell in the remaining MA stages to reduce their gain. In other words, at very high inputs, the TIA and the EMA interchange their roles. That is, the TIA introduces a high-frequency peaking that is then suppressed by the subsequent low-bandwidth amplifier. Figure 17 shows the simulation results for output eye diagrams when the input is set to 1 mA_{pp} at 10 Gb/s and 20 Gb/s. To generate these eyes, the TIA's feedback resistor is reduced to 60 Ω and the LPFs are removed from the EMA circuit. Despite the 7 dB of peaking in the TIA's amplitude response, the overall FE shows a flat amplitude response and a bandwidth of 12 GHz. The eye is fully open at 10 Gb/s. At 20 Gb/s, the internal eye opening is better than 60% of the maximum value. At both data rates, the eye opening is larger than it was at the sensitivity level. The widened eyes demonstrate the capability of the circuit to handle large input signals.

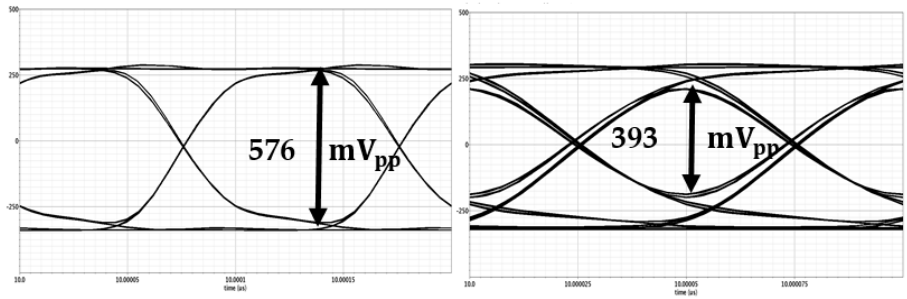

Figure 17. Simulation results for the output eye diagram when the input current is set to 1 mA_{pp} at (**a**) 10 Gb/s and (**b**) 20 Gb/s.

6. Conclusions

A design technique that relaxes the trade-off between gain and bandwidth in CMOS multi-stage amplifiers has been presented. To improve gain and reduce noise, the transimpedance amplifier is designed with a larger feedback resistor and its bandwidth limitation is compensated by a follow-on equalizing main amplifier (EMA). The EMA leverages the improved performance of state-of-the-art active-feedback main amplifier designs, but with the added benefit of high-frequency peaking. By embedding the equalizer stage in the gain stage, the overall circuit attains the improved performance of traditional equalizer-based designs, while achieving better energy efficiency due to the elimination of the standalone equalizer stage. The proposed front-end outputs an eye diagram with vertical openings of 338.9 mV_{pp} and 180 mV_{pp} at 10 Gb/s and 20 Gb/s, respectively. The vertical eye openings are doubled compared those of the conventional wide band front-end that operates at the same data rate and dissipates the same power, demonstrating the capability of the proposed technique to drive a subsequent decision circuit with a negligible power penalty. Simulation results also verify that the presented FE functions properly with large input signals and exhibits a robust performance against process and temperature variations.

Author Contributions: Conceptualization, D.A.; methodology, D.A.; software, D.A.; validation, D.A. and C.W.; formal analysis, D.A.; investigation, D.A.; resources, O.L.-L. and G.E.R.C.; writing—original draft preparation, D.A.; writing—review and editing, O.L.-L. and G.E.R.C.; visualization, D.A.; supervision, O.L.-L. and G.E.R.C.; project administration, O.L.-L. and G.E.R.C.; funding acquisition, O.L.-L. and G.E.R.C. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the Natural Sciences and Engineering Research Council of Canada through the Strategic Project Grant Program (Grant number is STPGP 494385-16) and in part by the Faculty of Engineering and Computer Science at Concordia University.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Acknowledgments: The authors would like to thank CMC Microsystems for providing access to CAD tools, fabrication, and test equipment. They would like to thank T. Obuchowicz for CAD support. They would also like to thank A. I. Abbas and R. Priti for assistance in testing the receiver prototype.

Conflicts of Interest: The authors declare no conflict of interest.

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