



Article

Probing the Field-Effect Transistor with Monolayer MoS₂ Prepared by APCVD

Tao Han , Hongxia Liu * , Shulong Wang * , Shupeng Chen, Haiwu Xie and Kun Yang

Key Laboratory for Wide-Band Gap Semiconductor Materials and Devices of Education,
The School of Microelectronics, Xidian University, Xi'an 710071, China

* Correspondence: hxliu@mail.xidian.edu.cn (H.L.); slwang@xidian.edu.cn (S.W.);

Tel.: +86-130-8756-8718 (H.L.); +86-150-9115-4611 (S.W.)

Received: 25 July 2019; Accepted: 22 August 2019; Published: 27 August 2019



Abstract: The two-dimensional materials can be used as the channel material of transistor, which can further decrease the size of transistor. In this paper, the molybdenum disulfide (MoS₂) is grown on the SiO₂/Si substrate by atmospheric pressure chemical vapor deposition (APCVD), and the MoS₂ is systematically characterized by the high-resolution optical microscopy, Raman spectroscopy, photoluminescence spectroscopy, and the field emission scanning electron microscopy, which can confirm that the MoS₂ is a monolayer. Then, the monolayer MoS₂ is selected as the channel material to complete the fabrication process of the back-gate field effect transistor (FET). Finally, the electrical characteristics of the monolayer MoS₂-based FET are tested to obtain the electrical performance. The switching ratio is 10³, the field effect mobility is about 0.86 cm²/Vs, the saturation current is 2.75 × 10⁻⁷ A/μm, and the lowest gate leakage current is 10⁻¹² A. Besides, the monolayer MoS₂ can form the ohmic contact with the Ti/Au metal electrode. Therefore, the electrical performances of monolayer MoS₂-based FET are relatively poor, which requires the further optimization of the monolayer MoS₂ growth process. Meanwhile, it can provide the guidance for the application of monolayer MoS₂-based FETs in the future low-power optoelectronic integrated circuits.

Keywords: monolayer MoS₂; FET; mobility; Raman spectrum; photoluminescence (PL) spectrum

1. Introduction

The field effect transistors (FETs) are the basic unit of very large scale integrated circuits [1,2]. The feature size of the transistor has reached the physical limit with the integration of integrated circuits increases. Therefore, it is necessary to find the suitable semiconductor materials to improve the electrical performance of transistor [3,4]. Many researchers have focused on the two-dimensional materials with the single layer of atomic thickness [5]. The two-dimensional material is used as the channel material compared to the traditional bulk material, which can not only help to suppress the short channel effect, but also effectively reduces the static leakage current [6,7]. In addition, the two-dimensional materials also have the higher specific surface area, excellent mechanical strength, higher optical transparency, and various excellent photoelectric characteristics, so it can be widely used in the gas sensors [8], flexible electronics [9], and photodetectors [10]. Compared to the Si material, there are no dangling bonds in the low-dimensional transition metal sulfur compound materials when the transistor size is at the zoom limit [11]. The molybdenum disulfide (MoS₂) has the semiconductor characteristics, excellent physical and chemical properties, and unique microstructure, which can directly construct the field effect transistor. Therefore, the MoS₂ has become the very promising channel material in the process of the transistor scale.

As we all know, the thickness of the MoS₂ sample obtained by the mechanical peeling is larger, and the MoS₂ sample is smaller and irregular, so the MoS₂ is grown on the SiO₂/Si substrate by the

atmospheric pressure chemical vapor deposition (APCVD) [12]. There are many factors that affect the continuity and uniformity of the MoS₂ deposition while using the APCVD method to obtain the MoS₂, such as the growth temperature, growth time, the amount of S powder and MoO₃ powder, and the gas flow rate. The band gap of MoS₂ changes with the number of layers, the bulk MoS₂ has the moderate electron mobility and an indirect band gap of 1.29 eV, whereas the monolayer MoS₂ is a direct bandgap material with a band gap of 1.8 eV. The MoS₂ is a promising material for the flexible and transparent substrates, which can be applied in the logic circuits and optoelectronic devices [13]. The size and quality of MoS₂ have a great influence on the performance of the device. Therefore, we can improve the continuity and uniformity of the MoS₂ deposition by adjusting the growth process parameters and treating the SiO₂/Si substrate with the graphene quantum dot solution [14]. The FETs with the direct bandgap monolayer MoS₂ have the larger switching ratio and the lower off-state current. However, the mobility and on-state current of the FETs are very lower, so it is very meaningful to optimize and enhance the electrical performance, which can provide the application reference of the monolayer MoS₂-based FETs.

The paper is composed of five parts: First, the large-area high-quality monolayer MoS₂ is prepared by the APCVD to facilitate the fabrication of FETs [15]. Then, the monolayer MoS₂ is confirmed and characterized by the high resolution microscopy, Raman spectroscopy, photoluminescence spectroscopy, and field emission scanning electron microscopy. Next, the main preparation process of monolayer MoS₂-based FET is described. Subsequently, the electrical performance of the back-gate FET is measured. Finally, the conclusion of this paper is summarized. The following are the electrical performance parameters of the prepared monolayer MoS₂-based FET in this paper, the electrical performance parameters have increased by improving the electrode contact and channel material [16]. The switching ratio is as high as 10³, the field effect mobility is about 0.86 cm²/Vs, the saturation current is 2.75 × 10⁻⁷ A/μm, and the lowest gate leakage current is 10⁻¹² A. Besides, the monolayer MoS₂ can form the ohmic contact with the Ti/Au electrode. Although the electrical performance of monolayer MoS₂-based FETs is not ideal, we have mastered the fabrication process of monolayer MoS₂-based FETs, and the growth process of monolayer MoS₂ needs further optimization, which can provide the reference for the preparation of high quality monolayer MoS₂-based FETs [17].

2. The Growth and Characterization of Monolayer MoS₂

2.1. The Growth Process of Monolayer MoS₂

In this paper, the monolayer MoS₂ on SiO₂/Si substrate was grown by APCVD. First, the solid sulfur powder and MoO₃ powder could be melted into the gas state under the high temperature. Then the argon gas with a purity of 99.999% was passed as the carrier gas, and the sulfur gas was transferred to the vicinity of the SiO₂/Si substrate. At the same time, there was a certain concentration of MoO₃ vapor in the vicinity of the SiO₂/Si substrate. Finally, the sulfur gas could react with MoO₃ gas on the surface of the SiO₂/Si substrate to form the MoS₂. The specific growth experiment process of monolayer MoS₂ was as follows: The SiO₂/Si substrate was selected as the growth substrate of MoS₂, wherein 300 nm SiO₂ was the back gate dielectric layer of FET [18]. Before the growth experiment of MoS₂, the 1 cm × 1 cm SiO₂/Si substrate was first subjected to the oxygen plasma treatment. The vacuum tube furnace of the MoS₂ growth experiment was TF55035C-1, and the front end is equipped with a heater that could be heated to 400 °C, which could help to assist the evaporation of sulfur powder. First, the quartz boat with 100 ± 5 mg sulfur powder (Alfa Aesar, Shanghai, China, 99.5%) was placed in the middle zone of the heater. Then, the quartz boat with 2 ± 0.1 mg MoO₃ powder (Alfa Aesar, Shanghai, China, 99.95%) and SiO₂/Si substrate was placed in the middle of the tube furnace. Next, the argon gas with 200 sccm was introduced into the tube furnace for 10 min to eliminate the air of the tube furnace. Subsequently, the temperature of the sulfur powder was heated to 200 °C, and the MoO₃ powder was heated to 750 °C. During the growth of MoS₂, the argon gas with a flow rate of 40 sccm was continuously provided and the growth temperature was maintained for

10 min [19]. Finally, the growth reaction of MoS₂ was completed, and the MoS₂ sample was taken out while the temperature of the tube furnace was cooled to room temperature.

2.2. The Test Characterization Conditions of Monolayer MoS₂

The MoS₂ sample could be obtained by the APCVD. At the same time, the MoS₂ could be systematically characterized by optical microscopy, Raman spectroscopy, photoluminescence spectroscopy, and field emission scanning electron microscopy to further determine the layer number and quality of the MoS₂ sample. The Raman model was LabRam HR Evolution with a laser wavelength of 532 nm (HORIBA JobinYvon, Paris, France) [20]. The specific test conditions of the Raman spectrometer were the 100× objective lens, 1800 groove/mm grating, the spot size of 532 nm laser was 342 nm, and the incident laser power density was 140 μW/μm². Besides, the field emission scanning electron microscopy (FESEM, JSM-6700F, Hitachi, Tokyo, Japan) was also used at the accelerating voltage of 5 kV.

The monolayer MoS₂ and the SiO₂ of SiO₂/Si substrate could interfere with the light, so there was a reflection enhancement effect on the visible light wavelength of 532 nm. Figure 1a,b respectively show the 50× and 100× objective optical micrograph of monolayer MoS₂, the pink and blue patches in the optical images respectively represents the monolayer MoS₂ on SiO₂/Si substrate and the scale, it could be observed by the optical microscope that monolayer MoS₂ on SiO₂/Si substrate exhibited the bright blue color. As shown in Figure 1c, the typical FESEM image of monolayer MoS₂ clearly exhibited the quasi-equilateral triangles, which was consistent with the crystal structure. Besides, the Raman mapping was tested to observe the film formation quality and uniformity of the triangular MoS₂. It can be seen from the Figure 1d that the color of MoS₂ mapping was relatively uniform, which could indicate that the sample was the high-quality uniform monolayer MoS₂.

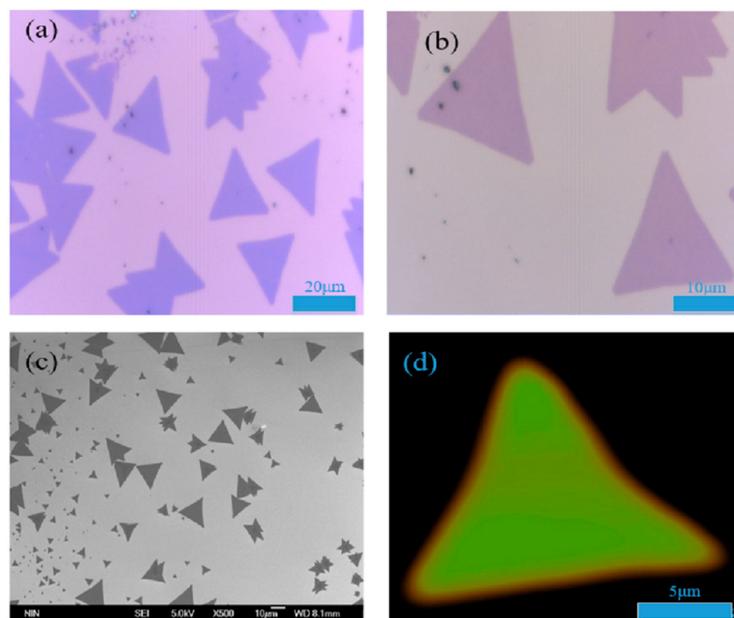


Figure 1. (a) The 50× objective optical micrograph of monolayer MoS₂; (b) the 100× objective optical micrograph of monolayer MoS₂; (c) the FESEM image of triangular monolayer MoS₂; and (d) the mapping diagram of monolayer MoS₂.

There were two characteristic peaks in the Raman spectrum of MoS₂, the layer number of MoS₂ sample could be measured by the Raman spectrum between the E¹_{2g} mode and the A_{1g} mode. It could be found by observing Figure 2a that the distance Δk between the E¹_{2g} characteristic peak and A_{1g} characteristic peak was $18 \pm 0.1 \text{ cm}^{-1}$, and the ratio of A_{1g}/E¹_{2g} was about 1.043, which indicates that the MoS₂ sample was a monolayer [21]. Figure 2b shows the photoluminescence spectrum of the

monolayer MoS₂ sample at different points. The photoluminescence spectrum of monolayer MoS₂ on SiO₂/Si substrate had I and B exciton peaks, the strongest I exciton peak position of monolayer MoS₂ was at 684.6 ± 0.5 nm, which could be explained by the direct exciton excitation [22]. The corresponding electron volt was at 1.82 ± 0.02 eV through the conversion relationship between wavelength and electron volts, which was consistent with the direct band gap width of monolayer MoS₂. In addition, there was also the B exciton peak at 1.97 ± 0.02 eV due to the 3d orbital electron interaction of Mo atoms, which could further prove that the sample was the large-area high-quality monolayer MoS₂.

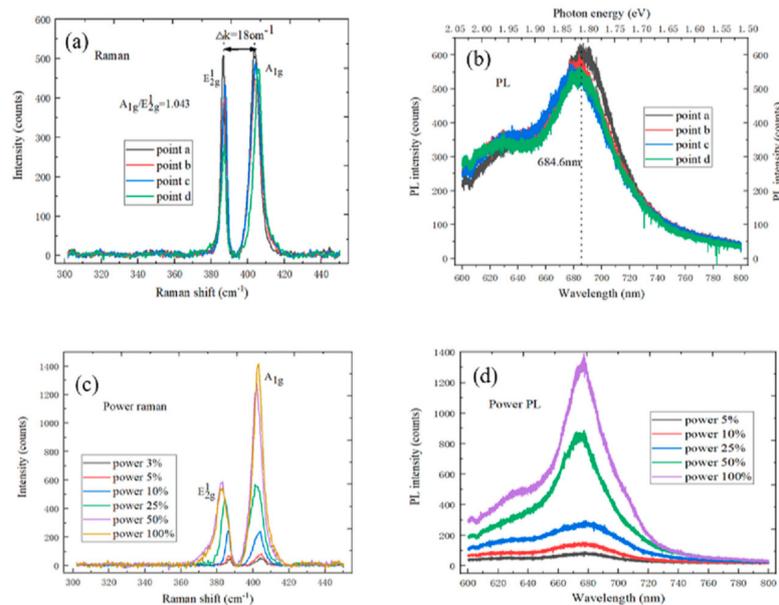


Figure 2. (a) The Raman spectrum of monolayer MoS₂ at the different test points; (b) the PL spectrum of monolayer MoS₂ at the different test points; (c) the Power Raman spectrum of monolayer MoS₂; and (d) the Power PL spectrum of monolayer MoS₂.

In Figure 2c, the Raman spectrum intensity of monolayer MoS₂ increased with the laser power increase. There was a blue shift of the E_{12g} characteristic peak when the laser power increased, and the A_{1g} characteristic peak position did not change. This was because the MoS₂ on the SiO₂/Si substrate was an n-type doped semiconductor material [23]. Figure 2d shows the power photoluminescence spectrum of monolayer MoS₂. The peak intensity of the photoluminescence spectrum increased when the laser power increased. At the same time, the relative positions between the I exciton peak and B exciton peak were red-shifted to some extent when the laser power increased. The reason was that the MoS₂ on SiO₂/Si substrate was the n-type doped material [24]. It is known from the above Raman spectrum and photoluminescence spectrum that the MoS₂ sample was a monolayer.

3. The Discussion of Electrical Performance Results

The field effect transistor is the most basic electronic component in the digital logic circuits, which consists of the channel, a source electrode, a drain electrode, and the gate dielectric layer [25]. It can control the channel internal carrier density and the source–drain current by adjusting the gate voltage, which can achieve the current amplification and power amplification.

3.1. The Fabrication Process of Monolayer MoS₂-Based FET

The monolayer MoS₂-based back-gate FET can be fabricated by the photolithography, electron beam evaporation, and lift-off micromachining processes, the above steps used the polymethyl methacrylate (PMMA) resist process. The following is the specific process flow schematic diagram of monolayer MoS₂-based FET [26]. First, the high-quality triangular monolayer MoS₂ is grown on the surface of Si/SiO₂ substrate by APCVD, as shown in Figure 3a; in Figure 3b, the pre-baking, gluing,

exposing, and developing processes were performed to complete the photolithography, then using the photoresist as a mask, and the Ar plasma etching process was performed to remove the exposed MoS₂ film, the photoresist was removed by the acetone solution, the ethanol solution was cleaned to determine the source and drain windows of monolayer MoS₂-based FET; Subsequently, the 20 nm Ni/70 nm Au were used as the source-drain metal contact by the electron beam evaporation, as shown in Figure 3c; Next, the photoresist was dissolved in the acetone solution, and the metal solution was removed by the ethanol solution, as shown in Figure 3d.

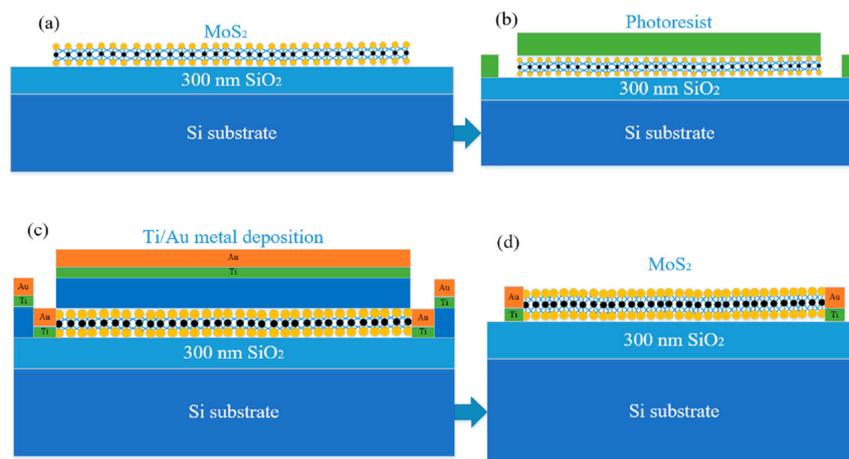


Figure 3. The main preparation process schematic diagram of the monolayer MoS₂-based field effect transistor (FET; (a) the growth process of the high-quality triangular monolayer MoS₂; (b) the photolithography and the Ar plasma etching process; (c) the electron beam evaporation process; and (d) the cleaning process of the photoresist.

Finally, the device was annealed in the vacuum environment of 180 °C for 2 h to remove the photoresist residue and decrease the contact resistance between the Ti/Au metal and monolayer MoS₂. The fabrication of monolayer MoS₂-based FET was completed, and the electrical performance of monolayer MoS₂-based FET was analyzed and tested by the multi-function probe station and the B1500A semiconductor parameter analyzer (Santa Clara, CA, USA).

Figure 4a–c respectively show the 10×, 50×, and 100× objective optical microscope images of the monolayer MoS₂-based back-gate FET, and the pink and blue patches in the optical images respectively represents the monolayer MoS₂ on SiO₂/Si substrate and the scale, it can be found that the area of monolayer MoS₂ was usually 10–30 μm, and the size of the triangular monolayer MoS₂ was relatively smaller compared to the metal electrodes, so the source and drain metal electrodes were divided into an electrode lead and the pad. The electrode lead (line width of 5 μm) was directly in contact with monolayer MoS₂, and the pad of the source and drain metal electrodes was a square of 100 μm × 100 μm, which was for the electrical performance tests on the multi-function probe station [27]. The FESEM image of the monolayer MoS₂-based back-gate FET is given in Figure 4d, it can be seen that the uneven brightness and blurred focus appeared on the surface of monolayer MoS₂, which was affected by the charging effect of the SiO₂/Si substrate during the FESEM scanning.

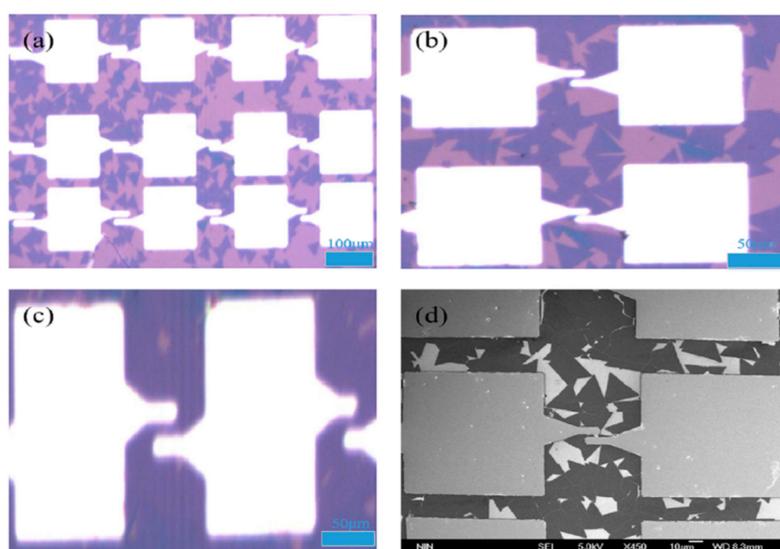


Figure 4. (a) The 10× objective optical microscope image; (b) the 50× objective optical microscope image; (c) the 100× objective optical microscope image of the monolayer MoS₂-based back-gate FET; and (d) the FESEM image of the monolayer MoS₂-based back-gate FET.

3.2. The Electrical Properties of Monolayer MoS₂-Based FET

Figure 5 shows the electrical test structure schematic diagram of the monolayer MoS₂-based back-gate FET. The gate oxide of the back gate electrode was 300 nm SiO₂, and monolayer MoS₂ was used as the conductive channel material. To decrease the contact resistance, the source/drain metal electrodes were made of 20 nm Ti/70 nm Au. The 20 nm Ti metal acted as the adhesion layer between monolayer MoS₂ and the Au, which could prevent the Au metal falling off from the MoS₂ film [28]. Besides, the Ti metal could also facilitate the formation of the ohmic contact between the monolayer MoS₂ sample and the Au electrode.

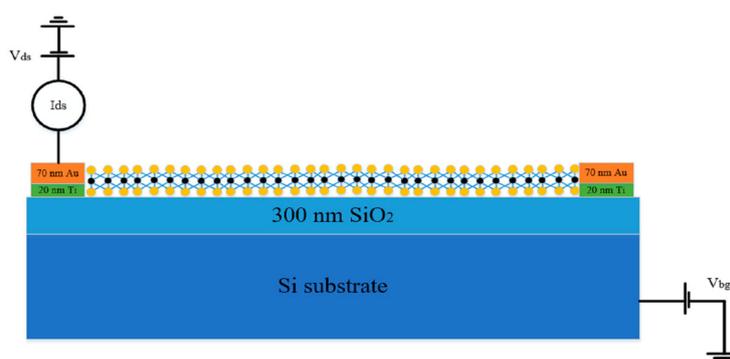


Figure 5. The electrical test structure of the monolayer MoS₂-based back-gate FET.

The transfer and output characteristics of monolayer MoS₂-based back-gate FET are shown in Figure 6. It can be seen by observing Figure 6a that the on-state current of the FET increased with the source–drain voltage increase. When the source–drain voltage was 0.9 V, the on-state current was about 2.75×10^{-7} A/ μ m, which was far from the application requirement of the high-performance FET [29]. In Figure 6b, the gate voltage could effectively regulate the channel resistance and the source–drain current, which exhibited the better switching characteristics. The source–drain current decreased when the back-gate electrode was at the negative voltage, whereas the source–drain current increased when a forward voltage was applied to the back-gate electrode, so the monolayer MoS₂-based FET was the *n*-type transmission, and the switching ratio could reach 10³. The reason was that monolayer

MoS₂ had the smaller grain size and the relatively poor quality, which had a major effect on the device performance.

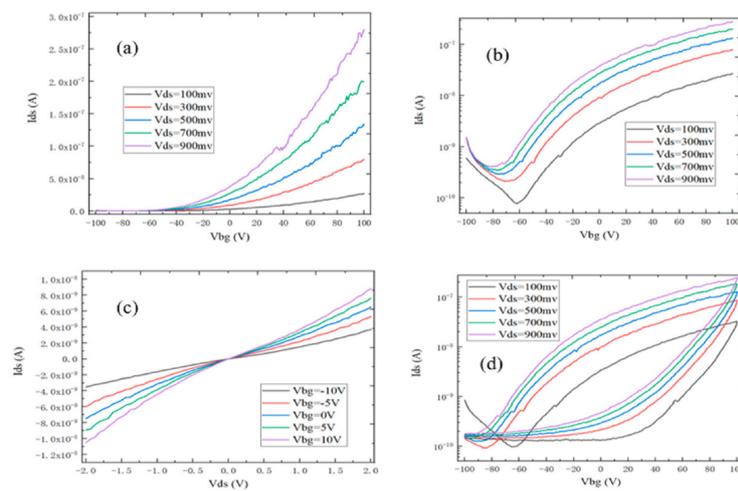


Figure 6. The monolayer MoS₂-based back-gate FET. (a) The I_{ds} - V_{bg} transfer curve; (b) the I_{ds} - V_{bg} transfer curve with the ordinate semi-logarithmic coordinate; (c) the I_{ds} - V_{ds} output curve; and (d) the hysteresis loop of MoS₂ FET under different V_{ds} .

Based on the I_{ds} - V_{gs} transfer curve, the field effect mobility can be calculated by using the following equation [30]:

$$\mu = \frac{dI_{ds}}{dV_{gs}} \frac{L}{W(\epsilon_0 \epsilon_r / d) V_{ds}} \quad (1)$$

The channel length of device $L = 10 \mu\text{m}$, the channel width of device $W = 10 \mu\text{m}$, the source and drain voltage $V_{ds} = 0.9 \text{ V}$, vacuum dielectric constant $\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m}$, the relative dielectric constant of SiO₂ $\epsilon_r = 3.9$, the thickness of SiO₂ $d = 300 \text{ nm}$, dI_{ds}/dV_{gs} is the slope of the transfer curve. Therefore, when the V_{ds} is 0.9 V , the field effect mobility is approximately $0.86 \pm 0.05 \text{ cm}^2/\text{Vs}$ according to the slope of the linear region between 40 V and 100 V . This is because the lattice structure of MoS₂ grown by APCVD is not complete. There are the lattice defects, which can deteriorate the mobility of monolayer MoS₂-based FET. Due to the large forbidden band width of monolayer MoS₂, the lowest gate leakage current of MoS₂ FET is at the 10^{-12} A when the gate voltage gradually increase from -100 to 100 V , so it is suitable for the low-power logic circuits. The lower gate leakage current can effectively decrease the leakage power, which can help to improve the lifetime of the device [31]. As shown in Figure 6c, the output curve of monolayer MoS₂ FET was linear, the gate voltage could well control the output current, and the output current increased with the gate voltage increase, which indicates that the monolayer MoS₂-based FET was an n -type carrier transmission. For the monolayer MoS₂-based back-gate FET, the current was proportional to V_{ds} in the linear regime at the small source-drain voltage, and the I_{ds} - V_{ds} curve of FET device exhibited the odd function characteristic with the good linearity and central symmetry when the V_{ds} increased from -2 to 2 V . Moreover, the V_{gs} had a significant regulation effect on the slope of the output curve, which indicates that the monolayer MoS₂-based back gate FET could form the good ohmic contact between the Ti/Au metal and MoS₂ channels. It can be found from Figure 6d that the transfer characteristic curve had the obvious hysteresis phenomenon. This is due to the fact that the channel material used monolayer MoS₂, which was very sensitive to the environmental change [32]. The monolayer MoS₂-based FET could absorb the moisture and impurity gases from the air, which would have the important impact on the electrical performance of the monolayer MoS₂-based FET.

4. Conclusions

In this paper, the monolayer MoS₂ on SiO₂/Si substrate was grown by APCVD, and the MoS₂ sample was characterized by the high resolution microscope, the Raman spectroscopy, photoluminescence spectroscopy, and field emission scanning electron microscopy, which could prove the existence of monolayer MoS₂. In order to evaluate the quality of monolayer MoS₂ systematically, the monolayer MoS₂ was used as the channel material of the FET, and the back gate FET was fabricated on the monolayer MoS₂. It could be found from the electrical parameters of FET that the ohmic contact could be formed between monolayer MoS₂ and Ti/Au metal electrode, the gate leakage current and static power consumption were lower. At the same time, the on-state current was about 2.75×10^{-7} A/ μ m when the source-drain voltage was 0.9 V, both the switching ratio and the mobility increased to some extent, which still need further improvement. The growth process of MoS₂ was optimized to obtain the higher quality monolayer MoS₂, so that the monolayer MoS₂-based FET could be applied to the future low-power optoelectronic integrated circuits.

Author Contributions: Conceptualization and writing—original draft preparation, T.H. and K.Y.; methodology, S.W. and S.C.; validation, T.H. and H.X.; writing—review and editing, H.L. and S.W.; funding acquisition, H.L.

Funding: This research was funded by the National Natural Science Foundation of China (Grant Nos. U1866212 and 61904136), the Foundation for Fundamental Research of China (Grant No. JSZL2016110B003), the Major Fundamental Research Program of Shaanxi (Grant No. 2017ZDJC-26), innovation Foundation of Radiation Application (Grant No. KFZC2018040206), and supported by the Fundamental Research Funds for the Central Universities, and the Innovation Fund of Xidian University.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Lin, M.-W.; Kravchenko, I.; Fowlkes, J.; Li, X.; Poretzky, A.; Rouleau, C.M.; Geohegan, D.B.; Xiao, K. Thickness-dependent charge transport in few-layer MoS₂ field-effect transistors. *Nanotechnology* **2016**, *27*, 165203. [[CrossRef](#)] [[PubMed](#)]
2. Chae, W.H.; Cain, J.D.; Hanson, E.D.; Murthy, A.A.; Dravid, V.P. Substrate-induced strain and charge doping in CVD-grown monolayer MoS₂. *Appl. Phys. Lett.* **2017**, *111*, 143106. [[CrossRef](#)]
3. Momeni, K.; Ji, Y.; Zhang, K.; Robinson, J.A.; Chen, L.-Q. Multiscale framework for simulation-guided growth of 2D materials. *NPJ 2D Mater. Appl.* **2018**, *2*, 27. [[CrossRef](#)]
4. Zhu, H.; Wang, X.; Zhang, T.-B.; Yang, W.; Chen, L.; Sun, Q.-Q.; Zhang, D.W. Improved integration of ultra-thin high-k dielectrics in few-layer MoS₂ FET by remote forming gas plasma pretreatment. *Appl. Phys. Lett.* **2017**, *110*, 053110.
5. Zubair, A.; Sajjad, R.N.; Tavakkoli, K.G.A.; Fang, S.; Ling, X.; Kong, J.; Dresselhaus, M.S.; Kaxiras, E.; Berggren, K.K.; Antoniadis, D.; et al. MoS₂ Field-Effect Transistor with Sub-10-nm Channel Length. *Nano Lett.* **2016**, *16*, 7798–7806.
6. Xu, H.; Zhou, W.; Zheng, X.; Huang, J.; Feng, X.; Ye, L.; Xu, G.; Lin, F. Control of the nucleation density of molybdenum disulfide in large-scale synthesis using chemical vapor deposition. *Materials* **2018**, *11*, 870. [[CrossRef](#)] [[PubMed](#)]
7. Sanne, A.; Ghosh, R.; Rai, A.; Yogeesh, M.N.; Shin, S.H.; Sharma, A.; Jarvis, K.; Mathew, L.; Rao, R.; Akinwande, D.; et al. Radio Frequency Transistors and Circuits Based on CVD MoS₂. *Nano Lett.* **2015**, *15*, 5039–5045. [[CrossRef](#)] [[PubMed](#)]
8. Han, T.; Liu, H.; Wang, S.; Li, W.; Chen, S.; Yang, X.; Cai, M. Research on the Factors Affecting the Growth of Large-Size Monolayer MoS₂ by APCVD. *Materials* **2018**, *11*, 2562. [[CrossRef](#)] [[PubMed](#)]
9. Liu, H.; Neal, A.T.; Ye, P.D. Channel Length Scaling of MoS₂ MOSFETs. *ACS Nano* **2012**, *6*, 8563–8569. [[CrossRef](#)]
10. Zafar, A.; Nan, H.; Zafar, Z.; Wu, Z.; Jiang, J.; You, Y.; Ni, Z. Probing the intrinsic optical quality of CVD grown MoS₂. *Nano Res.* **2017**, *10*, 1608–1617. [[CrossRef](#)]
11. Li, X.; Zhu, H. Two-dimensional MoS₂: Properties, preparation, and applications. *J. Mater.* **2015**, *1*, 33–44. [[CrossRef](#)]

12. Wang, J.; Yao, Q.; Huang, C.-W.; Zou, X.; Liao, L.; Chen, S.; Fan, Z.; Zhang, K.; Wu, W.; Xiao, X.; et al. High Mobility MoS₂ Transistor with Low Schottky Barrier Contact by Using Atomic Thick h-BN as a Tunneling Layer. *Adv. Mater.* **2016**, *28*, 8302–8308. [[CrossRef](#)] [[PubMed](#)]
13. Xu, W.; Li, S.; Zhou, S.; Lee, J.K.; Wang, S.; Sarwat, S.G.; Wang, X.; Bhaskaran, H.; Pasta, M.; Warner, J.H. Large Dendritic Monolayer MoS₂ Grown by Atmospheric Pressure Chemical Vapor Deposition for Electrocatalysis. *ACS Appl. Mater. Interfaces* **2018**, *10*, 4630–4639. [[CrossRef](#)] [[PubMed](#)]
14. Di Bartolomeo, A.; Genovese, L.; Foller, T.; Giubileo, F.; Luongo, G.; Croin, L.; Liang, S.-J.; Ang, L.K.; Schleberger, M. Electrical transport and persistent photoconductivity in monolayer MoS₂ phototransistors. *Nanotechnology* **2017**, *28*, 214002. [[CrossRef](#)] [[PubMed](#)]
15. Das, S.; Demarteau, M.; Roelofs, A. Nb-doped single crystalline MoS₂ field effect transistor. *Appl. Phys. Lett.* **2015**, *106*, 173506. [[CrossRef](#)]
16. Chen, T.; Zhou, Y.; Sheng, Y.; Wang, X.; Zhou, S.; Warner, J.H. Hydrogen-Assisted Growth of Large-Area Continuous Films of MoS₂ on Monolayer Graphene. *ACS Appl. Mater. Interfaces* **2018**, *10*, 7304–7314. [[CrossRef](#)]
17. Bhattacharjee, S.; Ganapathi, K.L.; Mohan, S.; Bhat, N. A sub-thermionic MoS₂ FET with tunable transport. *Appl. Phys. Lett.* **2017**, *111*, 163501. [[CrossRef](#)]
18. Zhang, F.; Appenzeller, J. Tunability of Short-Channel Effects in MoS₂ Field-Effect Devices. *Nano Lett.* **2014**, *15*, 301–306. [[CrossRef](#)]
19. Han, T.; Liu, H.; Wang, S.; Chen, S.; Li, W.; Yang, X. Probing the Growth Improvement of Large-Size High Quality Monolayer MoS₂ by APCVD. *Nanotechnology* **2019**, *9*, 433. [[CrossRef](#)]
20. Bhattacharjee, S.; Ganapathi, K.L.; Nath, D.N.; Bhat, N. Intrinsic limit for contact resistance in exfoliated multilayered MoS₂ FET. *IEEE Electron Device Lett.* **2015**, *37*, 119–122. [[CrossRef](#)]
21. Kim, C.-K.; Yu, C.H.; Hur, J.; Bae, H.; Jeon, S.-B.; Park, H.; Choi, K.C. Abnormal electrical characteristics of multi-layered MoS₂ FETs attributed to bulk traps. *2D Mater.* **2016**, *3*, 15007. [[CrossRef](#)]
22. Zhang, Y.; Xu, L.; Walker, W.R.; Tittle, C.M.; Backhouse, C.J.; Pope, M.A. Langmuir films and uniform, large area, transparent coatings of chemically exfoliated MoS₂ single layers. *J. Mater. Chem. C* **2017**, *5*, 11275–11287. [[CrossRef](#)]
23. Amani, M.; Chin, M.L.; Birdwell, A.G.; O'Regan, T.P.; Najmaei, S.; Liu, Z.; Ajayan, P.M.; Lou, J.; Dubey, M. Electrical performance of monolayer MoS₂ field-effect transistors prepared by chemical vapor deposition. *Appl. Phys. Lett.* **2013**, *102*, 193107. [[CrossRef](#)]
24. Li, Z.; Ye, R.; Feng, R.; Kang, Y.; Zhu, X.; Tour, J.M.; Fang, Z. Graphene quantum dots doping of MoS₂ monolayers. *Adv. Mater.* **2015**, *27*, 5235–5240. [[CrossRef](#)] [[PubMed](#)]
25. Strojnik, M.; Kovic, A.; Mrzel, A.; Buh, J.; Strle, J.; Mihailovic, D. MoS₂ nanotube field effect transistors. *AIP Adv.* **2014**, *4*, 97114. [[CrossRef](#)]
26. Yu, F.; Liu, Q.; Gan, X.; Hu, M.; Zhang, T.; Li, C.; Kang, F.; Terrones, M.; Lv, R. Ultrasensitive Pressure Detection of Few-Layer MoS₂. *Adv. Mater.* **2017**, *29*, 1603266. [[CrossRef](#)] [[PubMed](#)]
27. Chang, H.Y.; Yogeesh, M.N.; Ghosh, R.; Rai, A.; Sanne, A.; Yang, S.; Lu, N.; Banerjee, S.K.; Akinwande, D. Large-Area Monolayer MoS₂ for Flexible Low-Power RF Nanoelectronics in the GHz Regime. *Adv. Mater.* **2016**, *28*, 1818–1823. [[CrossRef](#)]
28. Li, X.; Li, X.; Zang, X.; Zhu, M.; He, Y.; Wang, K.; Xie, D.; Zhu, H. Role of hydrogen in the chemical vapor deposition growth of MoS₂ atomic layers. *Nanoscale* **2015**, *7*, 8398–8404. [[CrossRef](#)]
29. Liu, F.; Wang, J.; Wang, L.; Cai, X.; Jiang, C.; Wang, G. Enhancement of photodetection based on perovskite/MoS₂ hybrid thin film transistor. *J. Semicond.* **2017**, *38*, 34002. [[CrossRef](#)]
30. Chow, P.K.; Singh, E.; Viana, B.C.; Gao, J.; Luo, J.; Li, J.; Lin, Z.; Elías, A.L.; Shi, Y.; Wang, Z. Wetting of mono and few-layered WS₂ and MoS₂ films supported on Si/SiO₂ substrates. *ACS Nano* **2015**, *9*, 3023–3031. [[CrossRef](#)]

31. Kang, J.; Liu, W.; Banerjee, K. High-performance MoS₂ transistors with low-resistance molybdenum contacts. *Appl. Phys. Lett.* **2014**, *104*, 93106. [[CrossRef](#)]
32. Li, H.; Yin, Z.; He, Q.; Li, H.; Huang, X.; Lu, G.; Fam, D.W.H.; Tok, A.I.Y.; Zhang, Q.; Zhang, H. Fabrication of single- and multilayer MoS₂ film-based field-effect transistors for sensing NO at room temperature. *Small* **2012**, *8*, 63–67. [[CrossRef](#)] [[PubMed](#)]



© 2019 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).