Article

Improvement of the Bias Stress Stability in 2D MoS_2 and WS_2 Transistors with a TiO_2 Interfacial Layer

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1. Fabrication process and band diagram for Fermi-level pinning with various metals

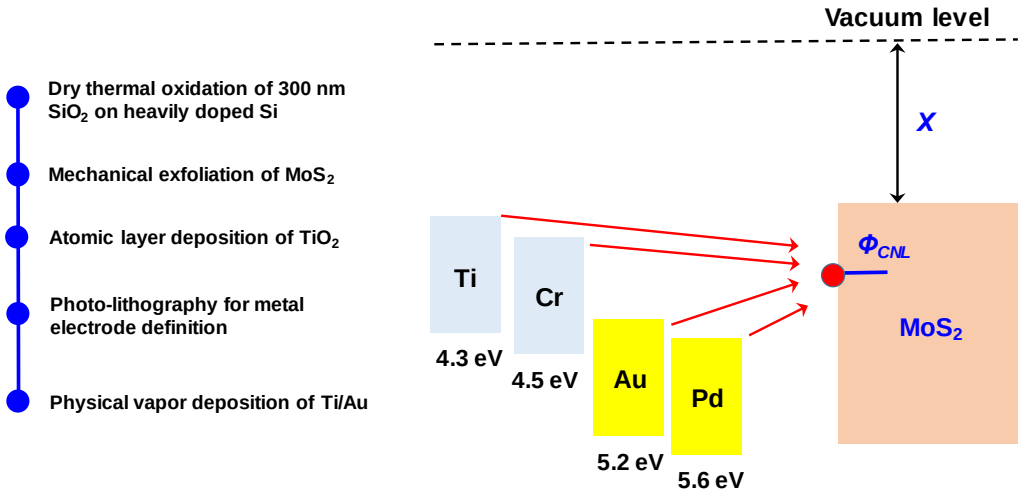

Figure S1. Fabrication process and band diagram for Fermi-level pinning with various metals.

Figure S1 shows fabrication process and the schematic for Fermi-level pinning in MoS_2. This is corresponding to the previous study [1].

2. Transfer and output curves for MoS_2 FETs without and with a TiO_2 layer

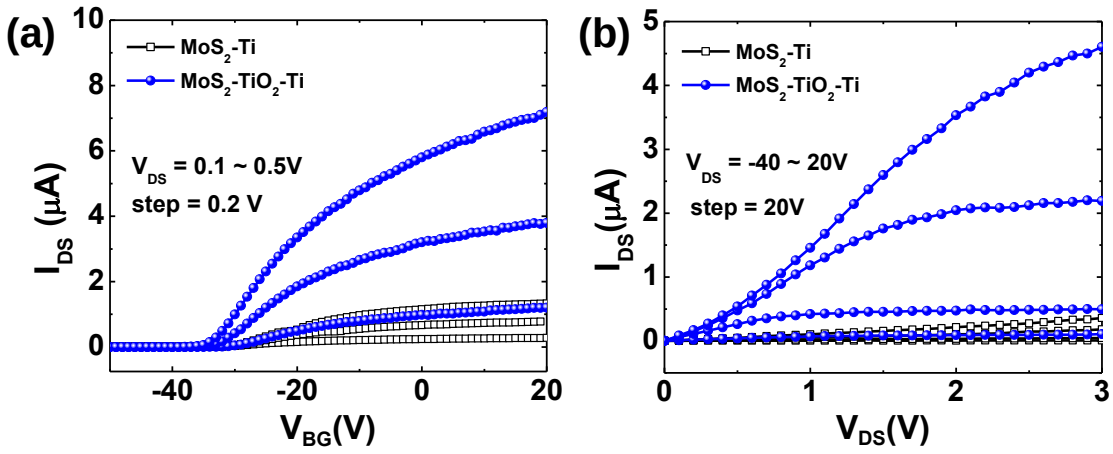

Figure S2. Transfer and output curves for MoS_2 FETs without and with a TiO_2 layer.

Figure S2 shows transfer and output curves for MoS_2 FETs without and with a TiO_2 layer. In the transfer curve, V_{BG} sweep was -50 ~ 20 V with V_{DS} = 0.1 ~ 0.5 V with 0.2 V of step. Improved performance was shown in the device with a TiO_2 layer, showing increased drain current. In the output curve, increased drain current and reduced series resistance (R_{SD}) were observed in the device with a TiO_2 layer.

3. Field-effect mobility (μ_{FE}) for MoS_2 FETs without and with a TiO_2 layer

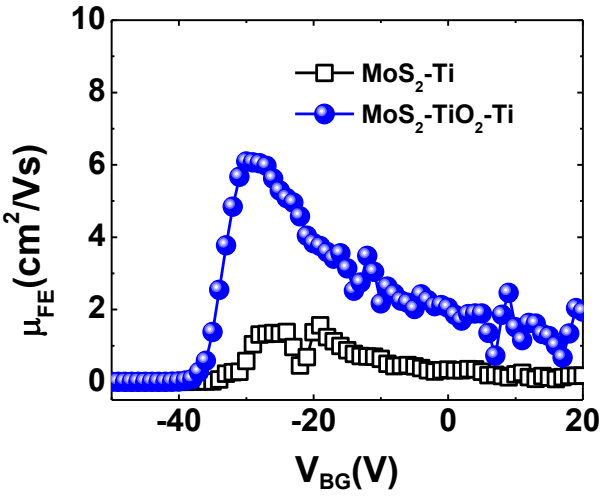

Figure S3. Field-effect mobility (μ_{FE}) for MoS_2 FETs without and with a TiO_2 layer.

Figure S3 shows field-effect mobility (μ_{FE}) for MoS_2 FETs without and with a TiO_2 layer. μ_{FE} values are changed as a function of V_{BG}, featuring maximum transconductance (g_m)

4. Transfer curves for WS_2-Ti, WS_2-TiO_2-Ti, WS_2-Pd, and WS_2-TiO_2-Pd structured FET device

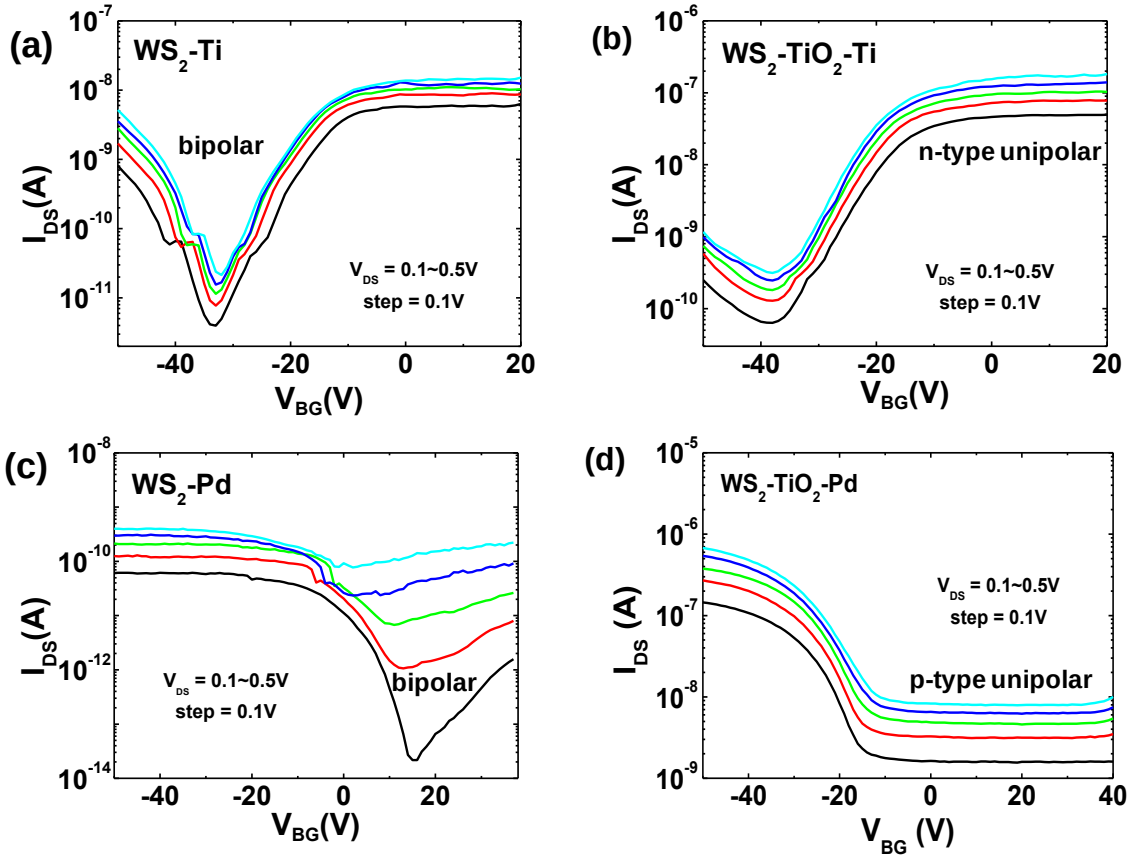

Figure S4. Transfer curves for WS_2-Ti, WS_2-TiO_2-Ti, WS_2-Pd, and WS_2-TiO_2-Pd structured FET devices.

Figure S4 shows the transfer curves for WS_2-Ti, WS_2-TiO_2-Ti, WS_2-Pd, and WS_2-TiO_2-Pd stack FETs. By inserting a TiO_2 layer, improved drive current was observed. Interestingly, type change behavior was observed from bi-polar to uni-polar behavior. Bi-polar behavior was observed from WS_2-Ti stack and it was changed to n-type unipolar behavior by using a TiO_2 layer. For Pd contact electrode, it was changed from bipolar to p-type unipolar behavior with the help of a TiO_2 layer. Previously, WS_2 FET have shown bipolar behavior and using a TiO_2 layer offers a benefit to achieve unipolar behavior which is usually used for an integrated circuit [2].

5. Energy band diagrams for TMDC-Ti and TMDC-TiO_2-Ti structures

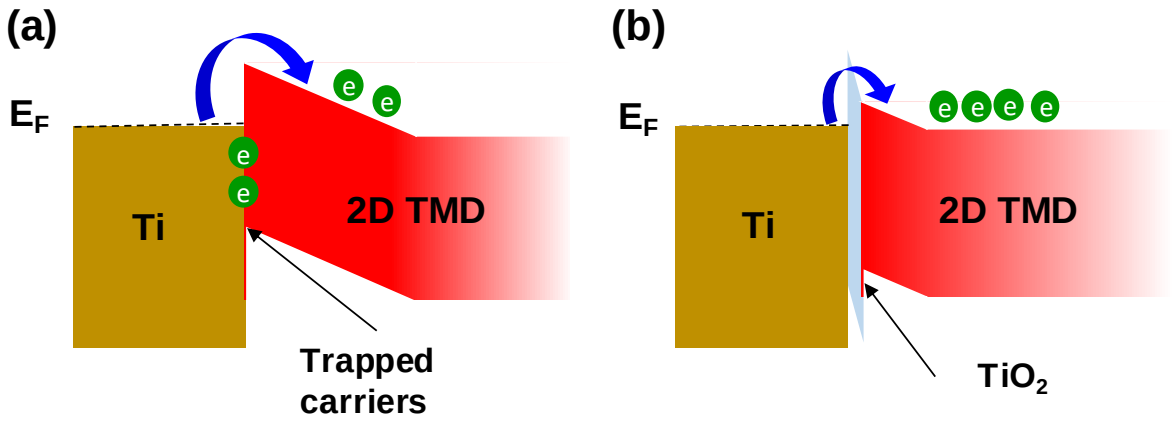

Figure S5. Energy band diagrams for TMDC-Ti and TMDC-TiO_2-Ti stacks.

Figure S5 shows band diagram for TMD-Ti and TMD-TiO_2-Ti stacks. The role of a TiO_2 layer is a buffer layer to cover dangling bonds to induce both Fermi-level pinning and device performance deviation. The effective Schottky barrier height becomes decreased in the TMD-TiO_2-Ti structure, leading to the increase in the electron conduction.

6. Bias stress measurement sequence

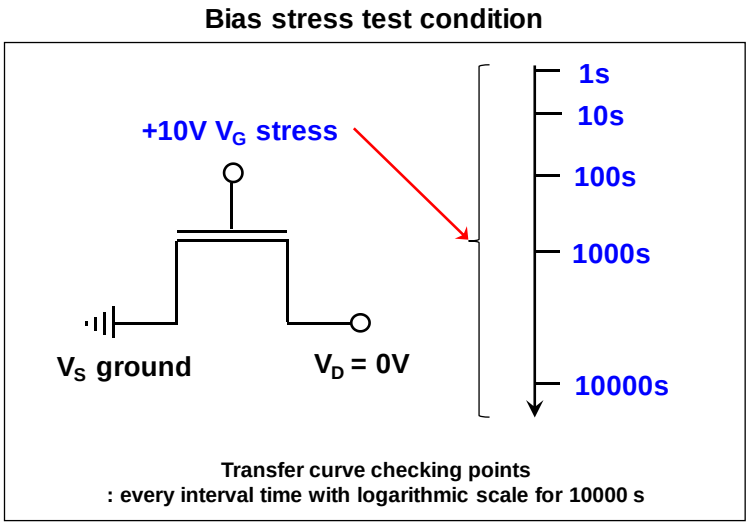

Figure S6. Bias stress measurement sequence.

Figure S6 shows the stress measurement set up environment and sequence. We followed the conventional repetitive stress-measurement-stress sequence. The stress measurements were conducted for 10000s and transfer curve was achieved every interval time with logarithmic scale (1s, 10s, 100s, 1000s, 10000s).

References

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