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Improvement of the Bias Stress Stability in 2D MoS_2 and WS_2 Transistors with a TiO_2 Interfacial Layer

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Abstract: The fermi-level pinning phenomenon, which occurs at the metal–semiconductor interface, not only obstructs the achievement of high-performance field effect transistors (FETs) but also results in poor long-term stability. This paper reports on the improvement in gate-bias stress stability in two-dimensional (2D) transition metal dichalcogenide (TMD) FETs with a titanium dioxide (TiO_2) interfacial layer inserted between the 2D TMDs (MoS_2 or WS_2) and metal electrodes. Compared to the control MoS_2, the device without the TiO_2 layer, the TiO_2 interfacial layer deposited on 2D TMDs could lead to more effective carrier modulation by simply changing the contact metal, thereby improving the performance of the Schottky-barrier-modulated FET device. The TiO_2 layer could also suppress the Fermi-level pinning phenomenon usually fixed to the metal–semiconductor interface, resulting in an improvement in transistor performance. Especially, the introduction of the TiO_2 layer contributed to achieving stable device performance. Threshold voltage variation of MoS_2 and WS_2 FETs with the TiO_2 interfacial layer was ~2 V and ~3.6 V, respectively. The theoretical result of the density function theory validated that mid-gap energy states created within the bandgap of 2D MoS_2 can cause a doping effect. The simple approach of introducing a thin interfacial oxide layer offers a promising way toward the implementation of high-performance 2D TMD-based logic circuits.

Keywords: MoS_2; WS_2; interfacial layer; contact resistance; bias stress stability

1. Introduction

The process of extreme scaling-down to reach a physical channel length limit of sub-100 nm has caused critical problems, such as a short channel effect and increased leakage current. To address these limitations, efforts have recently been made to scrutinize promising semiconducting materials. In particular, atomically thin layered transition metal dichalcogenides (TMDs) have attracted great attention due to their extraordinary electrical, optical, and mechanical properties [1–9]. One of their most attractive properties is the existence of a band-gap and its facile engineering. For instance, single-layer molybdenum disulfide (MoS_2) has a direct band-gap of ~1.8 eV, and multilayer MoS_2 has an indirect band-gap of ~1.2 eV [1]. The physical properties of 2D TMDs have led to their applications in various electronic devices such as transistors, memory devices, and opto-electronic devices [10–18]. Among them, the most promising device is the field caused effect transistor (FET), which functions as an essential switching component of display back-plane circuits [12].

However, a few challenging issues around employing 2D TMD-based FETs for practical applications have to be resolved. Fabricating large-scale, high-quality continuous 2D TMD films and the direct deposition of the gate dielectric layer on a 2D surface with a low surface energy are important issues in terms of the utilization of conventional Si fabrication infrastructures and the realization of high-mobility FETs. Furthermore, the unreliable performance of 2D TMD FETs has been a critical concern that must be preferentially addressed. Chemically and mechanically disordered surface and interface states are the origin of the performance instability of semiconductor devices, causing a large hysteresis window and a significant threshold voltage (V_{TH}) shift.

The passivation of the polymer layer on the 2D TMDs is an efficient countermeasure against the instability of 2D semiconductor-based FET performance [19,20]. Using a similar method, Zheng et al. reported that the hysteresis window of the 2D layered materials capped with an Al_2O_3 was considerably reduced [20]. Meanwhile, the contact engineering strategy for modifying the interface states between a metal and a 2D semiconductor has been actively studied [21–28]. Because the operation of the 2D TMD FET is based on a modulation of the Schottky-barrier, the interface quality at the metal/TMD contact becomes more critical. Several approaches to reduce the contact resistance, including a doping technique and selection of proper work function metal, have been proposed [26,28]. Meanwhile, Fermi-level pinning usually occurs at a metal/semiconductor contact region, causing high contact resistance due to a fixed high band offset regardless of the work function value of the metal [25,26,29]. Because the interface states usually serve as carrier trapping sites, it is hard to realize the high performance of 2D TMD FETs. Thus, a reliable and simple approach for Fermi-level depinning is necessary. The corresponding result was reported for an MoS_2 device with an interfacial oxide layer [29].

Herein, the effect of the interfacial buffer layer at the metal/2D TMD (MoS_2 and WS_2) contact on transistor performance was experimentally and theoretically investigated. Titanium dioxide (TiO_2) was used as a buffer layer because its band offset with MoS_2 and WS_2 is relatively small and tunnel resistance can be minimized with the thin TiO_2 layer. By employing a TiO_2 interlayer, interface states were successfully reduced, achieving an increased drive current and the enhancement of long term bias stress stability. In addition, the role of the TiO_2 layer on MoS_2 was theoretically elucidated using a density function theory (DFT) simulation. It can be highlighted that we suggested a facile approach to achieve both higher transistor performance and stability at the same time.

2. Materials and Methods

A mechanical exfoliation method using scotch tape to obtain high-quality 2D TMD flakes was adopted, and then the exfoliated 2D TMD flakes (MoS_2 and WS_2) were transferred onto a SiO_2 (300 nm)/heavily doped Si substrate. To identify the existence of the 2D TMDs, MoS_2 was mechanically exfoliated from the bulk mineral, and the multilayer MoS_2 was characterized using Raman spectroscopy (Figure 1a). LabRAM ARAMIS (laser wavelength: 473 nm, 50 mW) was used for Raman measurements. Two prominent peaks feature the in-plane E^1_{2g} mode (~384 cm^{-1}) and the out-of-plane A_{1g} mode (~409 cm^{-1}) of the MoS_2. A frequency difference of ~25 cm^{-1} between two vibrational modes indicates a multilayer MoS_2. To determine the thickness of the exfoliated MoS_2, we performed an atomic force microscopy (AFM) analysis. As shown in Figure 1b, the 92 nm-thick MoS_2 was transferred onto the SiO_2/Si substrate using a typical scotch-tape exfoliation method.

To investigate the effect of the TiO_2 interlayer on the device's contact properties, 2D FET devices with back gate electrodes were fabricated: a control device without TiO_2 and a testing device with TiO_2. Figure 1c shows the 3D schematic image of the FET device with the 2D TMD-TiO_2-Ti/Au structure. The TiO_2 interfacial layer on the 2D TMDs was deposited using an atomic layer deposition (ALD) technique based on a tetrakis-dimethyl-amido-titanium (TDMAT) precursor at 200 °C. The pulse and purging times were 0.2 s and 20 s, respectively. The number of cycles were 15, resulting in a 2~3 nm thickness. The thickness of the TiO_2 layer was also optimized to avoid high tunnel resistance. The 2D TMD transistor devices were made by a conventional photolithography process. Photolithography was

conducted after spin-coating of the photoresist (AZ 5214, MicroChemicals, Germany), and the metal was deposited by a physical vapor evaporator. Electron beam evaporation was selected to minimize the physical damage on the surface of the TMDs. Lift-off processes were sequentially performed to make the source and drain electrodes. The channel distance between source and drain was ~3 μm. After device fabrication, the post-annealing process was conducted in a vacuum environment at 300 °C. The process of the vacuum annealing step included a 30 min ramping time to 300 °C, for a 1 h duration, and a cool down at room temperature. The electrical characterization (transfer, output, and stress measurement) was performed with a Keithley 4200-SCS (Keithley, Cleveland, OH, US). Stress measurement followed the conventional stress-measure-stress sequence for 10,000 s, which is summarized in Figure S6 of the Supplementary Materials information.

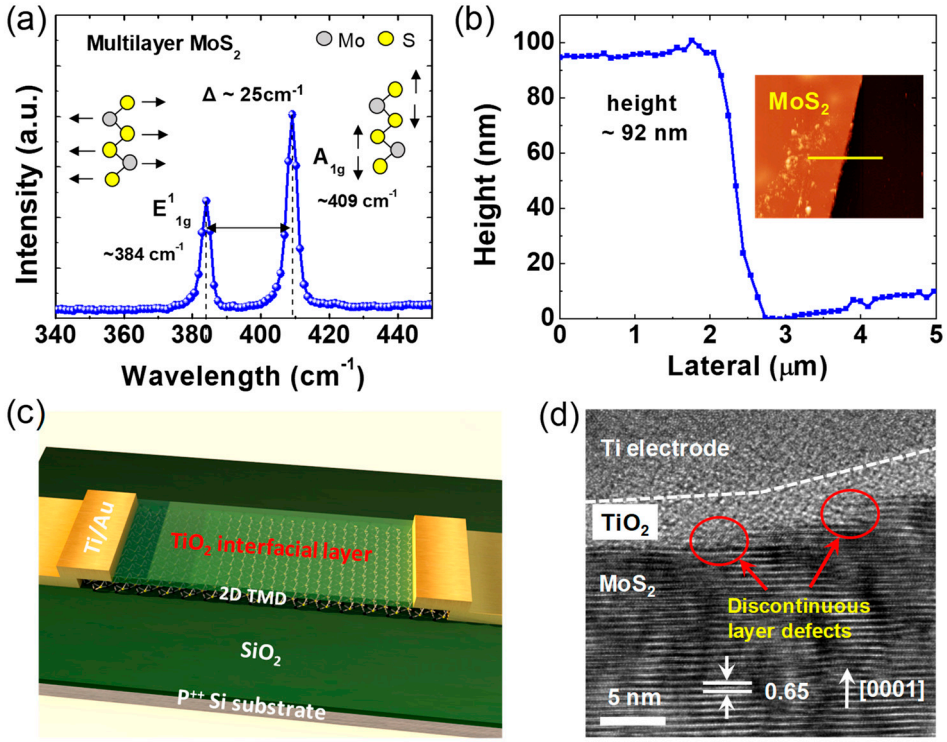

Figure 1. (**a**) Raman spectrum and (**b**) atomic force microscopy (AFM) analysis of a multilayer MoS_2; (**c**) 3D schematic image of a transition metal dichalcogenide field effect transistor (TMD FET) device; (**d**) a high-resolution transmission electron microscopy (HRTEM) image of the MoS_2-TiO_2-Ti stacked structure.

Figure 1d shows a cross-sectional high-resolution transmission electron microscopy (HRTEM) image of the MoS_2-TiO_2-Ti stacked structure. The lattice constant of the MoS_2 was measured to be ~0.65 nm along the c-plane [0001] direction in a hexagonal close-packed crystal structure. A thin (~3 nm-thick) TiO2 layer, deposited using the atomic layer deposition process, was inserted between the Ti metal and MoS_2. Interestingly, the discontinuous layers of the MoS_2 layers exhibited a step-like crystal structure. Thus, it is reasonably expected that randomness in the defect density for the exposed edge planes and basal planes can cause considerable deviation from the physical interface states, thereby inducing a large difference in the electrical properties of MoS_2. The structural disorder of the MoS_2 surface is also a strong source for Fermi-level pinning, which caused some points of the band gap to be locked (pinned) to the Fermi-level. This made the Schottky-barrier height considerably insensitive to the metal's work function. The Fermi-level pinning phenomenon, with respect to various metals (for instance, Ti, Cr, Au, and Pd), is illustrated in Figure S1 in the Supplementary Materials information. Even in the corresponding literature studies, the existence of dangling bonds in TMD has

been proven via in-depth analyses, such as scanning tunneling microscopy and inductively coupled plasma-mass spectroscopy [30–33].

3. Results and Discussion

To investigate the influence of a TiO_2 interfacial layer on the MoS_2 and WS_2 device performance, electrical measurements were performed. Basic electrical characterizations were carried out with a Keithley 4200-SCS (Keithley, Cleveland, OH, US) analyzer. Figure 2a shows a comparison between the transfer characteristics (I_{DS}-V_{BG}) of the MoS_2-Ti and MoS_2-TiO_2-Ti devices. The gate-bias sweeping ranged from −50 to 20 V at a fixed drain voltage of 0.1 V. A typical unipolar n-type behavior and a depletion mode of MoS_2 transistor devices were observed. The MoS_2-TiO_2-Ti device with a TiO_2 interfacial layer showed more enhanced performance with a higher drive on current (I_{ON}). I_{ON} values for devices without and with the TiO_2 layer are 0.36 and 1.22 μA, respectively. The field effect mobility (μ_{FE}) values for MoS_2-Ti and MoS_2-TiO_2-Ti devices were estimated to be 1.38 and 6.08 $cm^2/V{\cdot}s$, respectively. The transfer curves at variable drain voltages and output characteristic also confirmed the better performance of the testing devices with the TiO_2 layer (Figure S2 in the Supplementary Materials information). The μ_{FE} values of the MoS_2-TiO_2-Ti device as a function of gate voltage were higher than those of the MoS_2-Ti device (Figure S3 in the Supplementary Materials information).

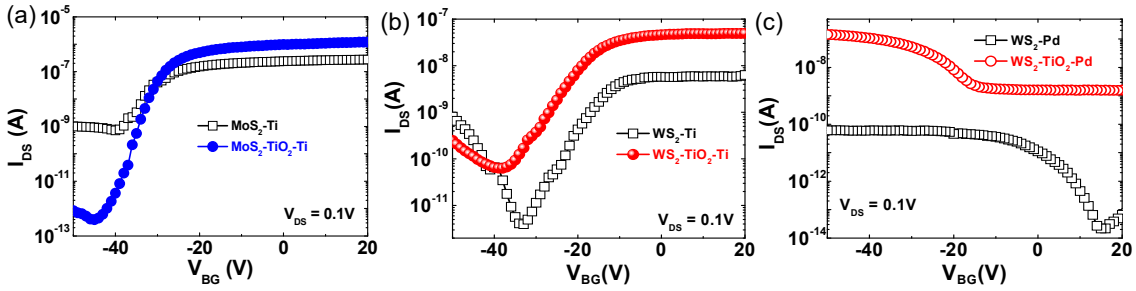

Figure 2. Transfer curves (I_{DS}-V_{BG}) for (**a**) MoS_2-Ti and MoS_2-TiO_2-Ti, (**b**) WS_2-Ti and WS_2-TiO_2-Ti, (**c**) and WS_2-Pd and WS_2-TiO_2-Pd.

A more interesting result was observed on the WS_2 FETs. Figure 2b shows a comparison of the I_{DS}-V_{BG} transfer characteristics of the WS_2-Ti and WS_2-TiO_2-Ti structured devices. The bi-polar behavior of the WS_2-Ti structured devices was observed, which is consistent with the previous results [34]. It is highly likely that the Fermi-level of the Ti metal exists within the mid-gap of WS_2. The transfer curve of the WS_2-TiO_2-Ti structured device showed stronger n-type unipolar behavior with a higher I_{ON} current than that of the WS_2-Ti device. As shown in Figure 2c, we also characterized the WS_2 devices using Pd metal electrodes with a relatively high work function of ~5.1 eV to understand the mid-gap pinning and the effects of an interfacial layer. The addition of the TiO_2 layer on the WS_2 caused a change from a weak bipolar to a p-type unipolar behavior. This result indicates that a high Schottky-barrier can be effectively reduced by a contact engineering approach utilizing a very thin TiO_2 interfacial layer. The I_{DS}-V_{BG} curves of the WS_2 FETs at various drain voltages are also shown in Figure S4 of the Supplementary Materials information. The performance enhancement of the 2D FET devices with the interfacial TiO_2 layer is attributed to the considerable reduction in the density of the diverse interface states, resulting from the direct contact between the metal and the 2D semiconductor channel. Comparison of the proposed band diagrams between the 2D TMD-Ti and 2D TMD-TiO_2-Ti devices highlights the change in the Schottky-barrier height as shown in Figure S5 in the Supplementary Materials information. In principle, the theoretical Fermi-level alignment between the metal and semiconductor, called Fermi-level depinning, also creates a more effective carrier modulation of the 2D TMD FET device.

For practical transistor applications, the electrical stability of the MoS_2 based FET devices was examined under a long-term positive gate-bias stress condition, as shown in Figure 3a–d. Figure 3a,b

shows the shift of the I_{DS}-V_{BG} curves during the long-term gate-bias stress test. The transfer I-V curve properties were monitored every logarithmic time interval (1, 10, 100, 1000, and 10,000 s) while continuously applying +10 V to the gate electrode. Schemes to illustrate the stress measurement set up environment and the data checking points are shown in Figure S6 of the Supplementary Materials information. Even if the I_{DS}-V_{BG} curves in all of the MoS_2-Ti and MoS_2-TiO_2-Ti devices were slightly shifted to the positive direction, the device with the TiO_2 layer showed less of a shift than that without TiO_2, indicating more stable electrical properties compared to the control device without TiO_2. Interestingly, in Figure 3b, the variation of I_{OFF} values for the MoS_2-TiO_2-Ti stack seems more severe than that of the control MoS_2-Ti device. The actual differences of the minimum and maximum I_{OFF} values are 4.20×10^{-12} A and 3.68×10^{-10} A for MoS_2-Ti and MoS_2-TiO_2-Ti, respectively. The I_{OFF} fluctuation of all the devices was less than 1 nA, and this fluctuation was negligible in operation. Figure 3c shows a summary of the threshold voltage (V_{TH}) change for MoS_2-Ti and MoS_2-TiO_2-Ti stacked devices as a function of stress time, which was extracted from the raw data from Figure 3a,b. The MoS_2 FET without a TiO_2 layer showed a more positive V_{TH} shift than that of the MoS_2 FET with a TiO_2 layer. The V_{TH} shift for the MoS_2 FET without and with a TiO_2 interfacial layer was 3.1 and 1.1 V, respectively. The TiO_2 layer could serve as a buffer layer to mitigate the interfacial damage from electrical stress. As shown in Figure 3d, we also compared the field-effect mobility (μ_{FE}) values for the devices without and with a TiO_2 layer. The μ_{FE} was estimated by following equation:

$$\mu_{FE} = g_m \frac{L}{W} \frac{1}{V_{DS}} \frac{1}{C_{ox}} \text{ and } g_m = \frac{\partial I_D}{\partial V_G}$$

where g_m is the maximum transconductance that can be achieved from I_{DS}-V_{BG}, L is the channel length, W is the channel width, V_{DS} is the applied drain bias, and C_{ox} is the gate oxide capacitance.

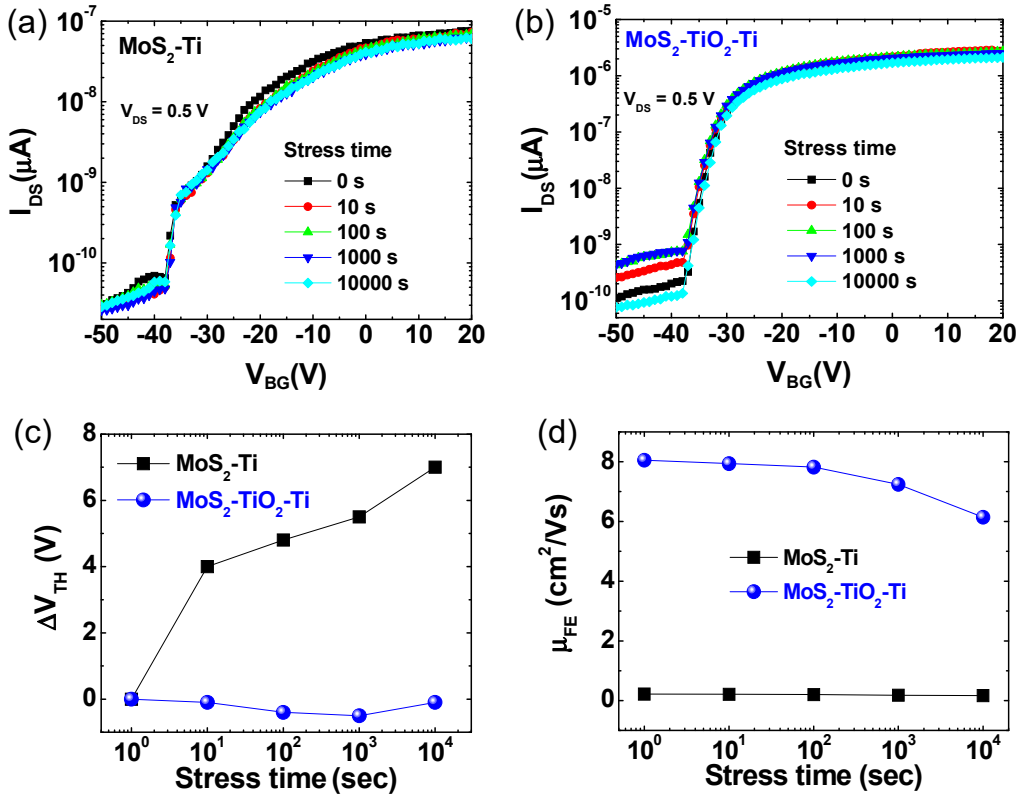

Figure 3. Transfer curves (I_{DS}-V_{BG}) of MoS_2 FETs (**a**) without TiO_2 and (**b**) with a TiO_2 layer during a 10,000 s gate-bias stress measurement at room temperature. The summary of (**c**) the ΔV_{TH} shift and (**d**) the μ_{FE} change as function of stress time for MoS_2-Ti and MoS_2-TiO_2-Ti.

Overall, the μ_{FE} of MoS_2-TiO_2-Ti device was higher than that of the MoS_2-Ti device. After 10,000 s stress time, the μ_{FE} was reduced from 0.22 to 0.17 cm^2/Vs for the device without a TiO_2 layer and from 8.05 to 6.14 cm^2/Vs for the device with a TiO_2 layer. Approximately, 25% of the μ_{FE} reduction was observed for both cases.

Additionally, the stability of the contact region for the WS_2-based FET devices was also determined for the effect of the interfacial TiO_2 layer on bias stress stability, as shown in Figure 4a,b. As can be seen, the transfer curves of the WS_2-Ti contact FET device showed bipolar behavior where both electron and hole carriers contribute to the current flow of the semiconductor channel. Overall, a lower V_{TH} shift was observed for the FET with a TiO_2 layer compared to the FET without a TiO_2 layer, indicating that the introduction of the TiO_2 interfacial layer on the WS_2 layered film is also an effective approach for improving the contact reliability of the WS_2 device, as well as the case of MoS_2 device. Specifically, the V_{TH} shifts for the WS_2 FET without and with a TiO_2 interfacial layer were 8 and 4.3 V, respectively (Figure 4c). As shown in Figure 4d, the change of μ_{FE} as a function of stress time was also fitted: the mobility value was almost unchanged for the control device without a TiO_2 layer and from 0.41 to 0.18 cm^2/Vs for the testing device with a TiO_2 layer.

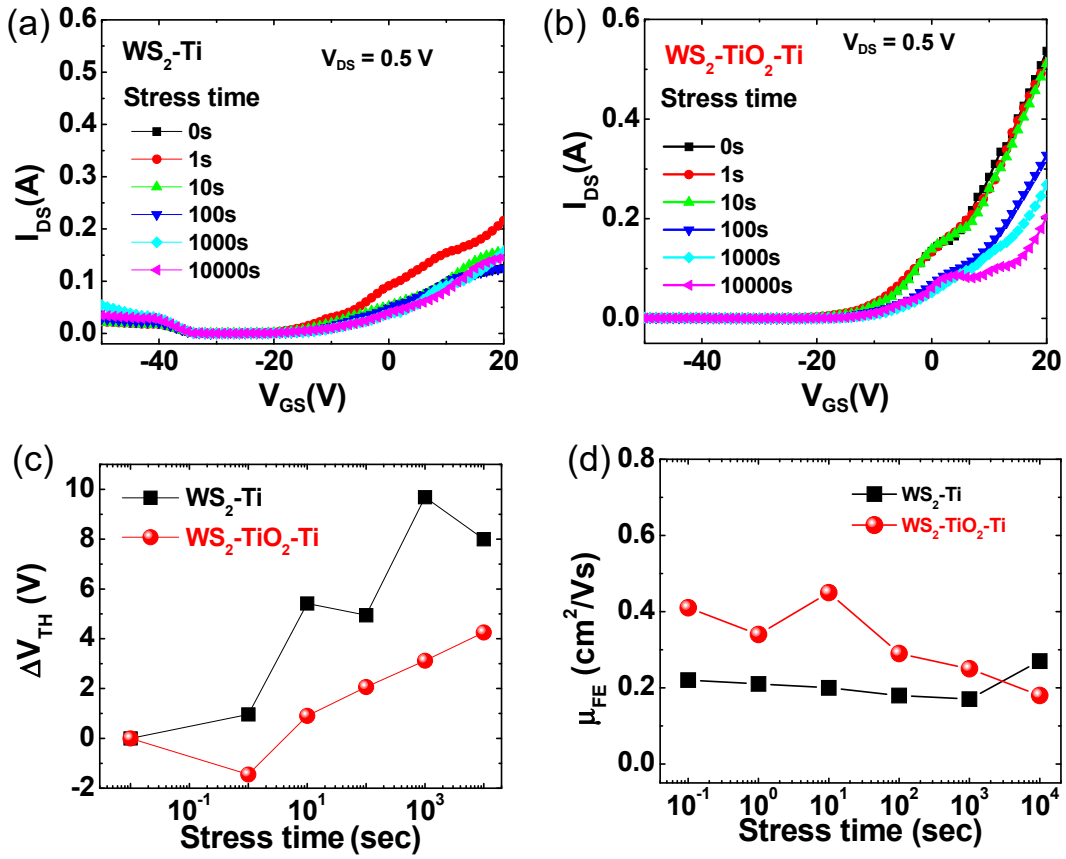

Figure 4. Transfer curves (I_{DS}-V_{BG}) of WS_2 FETs (**a**) without TiO_2 and (**b**) with a TiO_2 layer during a 10,000 s gate-bias stress measurement at room temperature. The summary of (**c**) the ΔV_{TH} shift and (**d**) the μ_{FE} change as a function of the stress time for WS_2-Ti and WS_2-TiO_2-Ti devices.

Indeed, the WS_2 FET device was more vulnerable to electrical stress than MoS_2, which might be due to greater number of interface states at the metal/semiconductor contact. The metal-induced gap states indispensably exist on the metal/semiconductor interface, which induces the instability of transistor performance. Additionally, there is a quantum mechanically long distance of 2–3 Å between the metal and 2D TMD, which increases the tunneling probability of charge carriers [35]. The more stable performance of the 2D TMD devices with an insulating TiO_2 layer might be understood by a mitigation of those gap states and a reduction in physical distance.

To unveil how the TiO_2 layer electronically influences the MoS_2 semiconductor, we explored a theoretical simulation of electronic states for free-standing MoS_2 and MoS_2/TiO_2 materials via a density functional theory (DFT) calculation (Figure 5). The density of states (DOS) calculation result of the free standing MoS_2 showed the existence of a forbidden gap (Figure 5a). Meanwhile, the TiO_2/MoS_2 hybrid combination featured a spin-polarized metallic behavior. The calculated DOS clearly validates that the addition of the TiO_2 layer leads to the modification of the electronical band structure of the junction region, offering the benefit of a doping effect on MoS_2.

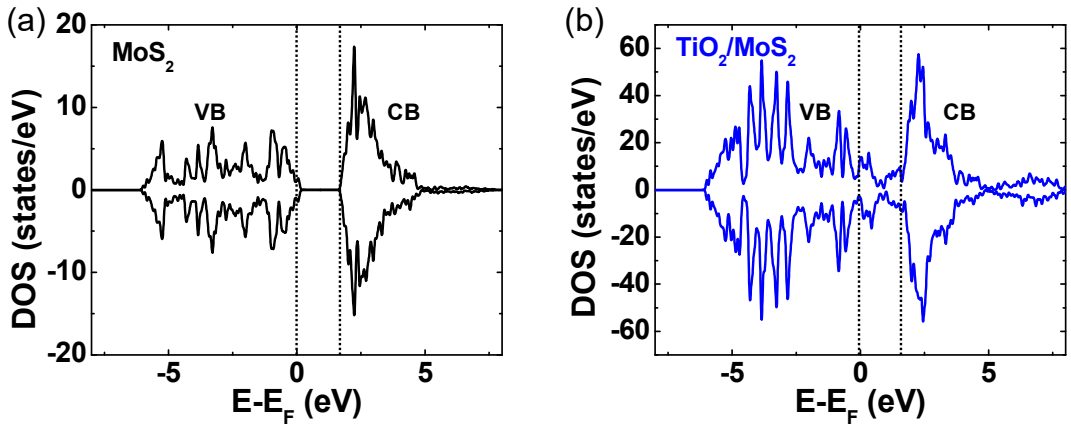

Figure 5. Density function theory (DFT)-calculated density of states (DOS) of (**a**) MoS_2 and (**b**) TiO_2/MoS_2.

4. Conclusions

The effect of a TiO_2 interfacial layer on metal/TMD (MoS_2 and WS_2) contact was experimentally and theoretically studied. The advantages of a Schottky-type FET device, possibly implemented according to the value of a metal work function, were achieved in the 2D TMD devices with a TiO_2 layer. Furthermore, a more enhanced and stable electrical performance for the 2D TMD FET devices with the TiO_2 interfacial layer could be obtained under a gate-bias stress condition. The TiO_2 interfacial layer could serve as a Fermi-level de-pinning layer, reducing the density of the interface states. Additionally, the DFT calculation validates the doping effect of the TiO_2 interfacial layer on the 2D MoS_2. The strategy of inserting a very thin insulating layer into the contact region will be also applied to diverse 2D TMD-based FET devices.

Supplementary Materials: The following are available online at http://www.mdpi.com/2079-4991/9/8/1155/s1, Figure S1: Fabrication process and band diagram for Fermi-level pinning with various metals; Figure S2: Transfer and output curves for MoS_2 FETs without and with a TiO_2 layer; Figure S3: Field-effect mobility (μFE) for MoS_2 FETs without and with a TiO_2 layer; Figure S4: Transfer curves for WS_2-Ti, WS_2-TiO_2-Ti, WS_2-Pd, and WS_2-TiO_2-Pd structured FET devices; Figure S5: Energy band diagrams for TMDC-Ti and TMDC-TiO_2-Ti stacks; Figure S6: Bias stress measurement sequence.

Author Contributions: W.P. designed and conducted the experiments, and H.Y.J., J.H.N., and S.O. supported the electrical measurement and analysis. T.H.K. set up the experiment system. Y.P., Y.K. and S.M.C. supported the process of experiments and the analysis of data. B.C. supported and guided the experiment and the results. B.C. conceived and advised the publication of paper.

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Conflicts of Interest: The authors declare no conflict of interest.

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