

Editorial

# Thin-Film Transistors

Feng-Tso Chien \*, Yu-Wei Chang and Jo-Chin Liu 

Department of Electronic Engineering, Feng Chia University, Taichung 407, Taiwan; j96590@gmail.com (Y.-W.C.); julia09281996@gmail.com (J.-C.L.)

\* Correspondence: ftchien@fcu.edu.tw

Thin film transistors (TFTs) are key components used in a variety of fields such as solar cell, active-matrix liquid crystal displays (AM-LCDs), pixel switches, peripheral driver circuit and flexible electronics. With many studies and technological breakthroughs in TFTs, the display technology of active array liquid crystals using these devices as switching elements has matured. To achieve high performance color saturation, response time, lifespan, and flexible use of the panel, which are highly desirable on the market, TFTs are of particular interest in studies of various semiconductor materials, gate dielectrics, improved device structure, core processing and device simulation.

This Special Issue, entitled “Thin-Film Transistors”, for the journal *Membranes*, aims to discuss the significant recent progress in TFTs. Twelve research articles contribute to this Special Issue. The selected topics include metal oxide and semiconductor materials, device characteristics improvement, fabrication process, theory discussion, device structure simulation, and integration circuit implementation.

For the improvement of metal oxide semiconductor materials and device characteristics, metal oxide semiconductors have higher electron mobility than amorphous silicon to improve display panel resolution. A more powerful display can be achieved in terms of refresh rate, greater efficiency in power consumption, integration applications such as flexible displays or integrated circuits. With an Ar-O<sub>2</sub> mixed plasma treatment and rapid thermal annealing, dual gate (DG) indium–gallium–zinc oxide (IGZO) TFTs can decrease the oxygen vacancy density in the IGZO thin film and demonstrate a greater accumulation of conduction electrons caused by modulation of the carrier transportation path in a DG structure [1], therefore improving device performance. Indium oxide has high transmittance features, and tin oxide has strong conductivity. Indium tin oxide ITO TFTs have attracted great attention in the field of displays and low-cost integrated circuits. The proper channel thickness on ITO TFT performance and positive bias stress stability are examined in [2] to achieve better device performance. It is found that the thickness of ITO dominates the content of oxygen defects and therefore synthetically affect the device characteristics by trap states and carrier concentration. Two-dimensional (2D) crystals have been suggested as a class of materials that may impact future electronic technologies. Black phosphorus is a single elemental 2D material with a sizable band gap and remarkable high hole mobility that is suitable for developing future nanoelectronic applications. Dewu Yue et al. [3] reveal that ambipolar black phosphorus devices fabricated by capping with transparent hexagonal boron nitride offers a feasible approach to implement digital circuits and high photoresponse BP photodetectors.

TFT characteristics can be improved by different process methods. A steep subthreshold swing (SS) can be achieved with plasma oxidation on a SiN<sub>x</sub> gate dielectric for InGaZnO TFTs by reducing the amount of oxygen vacancy near the interface between the SiN<sub>x</sub> and InGaZnO layer [4]. A Zirconium-doped Mg<sub>x</sub>Zn<sub>1-x</sub>O (Zr-doped MZO) mixed-oxide film by radio-frequency magnetron sputtering to reduce resistance and improve the electron mobility of MZO films is proposed in [5]. The dielectric layer is also an important core material of the TFTs. High relative dielectric constant (high-k) and a wide band gap material can be achieved by using multiple metals to increase the entropy of the structure.



**Citation:** Chien, F.-T.; Chang, Y.-W.; Liu, J.-C. Thin-Film Transistors. *Membranes* **2022**, *12*, 411. <https://doi.org/10.3390/membranes12040411>

Received: 6 April 2022

Accepted: 8 April 2022

Published: 9 April 2022

**Publisher's Note:** MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



**Copyright:** © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

Four metal oxides, zirconium–yttrium–aluminum–magnesium-oxide (ZYAMO), high-k dielectric layers were prepared using the solution method to reduce device leakage and improve the ability to store charges, as discussed in [6].

Channel traps and structural disorder in an amorphous oxide semiconductor (AOS) affect TFT's performance. An empirical modeling procedure to capture the gate bias dependency of In-Ga-Zn-O (IGZO) AOS TFTs while considering contact resistance and disorder effect is described and derived in [7], which is helpful to the development of an accurate compact TFT model. The hysteresis in TFT is another issue affecting circuit operation. It is believed that holes trapped in the dielectric are the main source of hysteresis. Improved hysteresis of the polycrystalline SnO<sub>2</sub> TFTs by various curing and a fixed annealing temperature to analyze and understand hysteresis behaviors and its application to the circuits is studied in [8]. Nanowire junctionless TFTs also demonstrate high potential in circuit application, owing to their small number of defects, high-density integration, and flexible dimension design. Poly-Si nanowire TFTs with external connection of a BiFeO<sub>3</sub> capacitor is studied to improve device characteristics on on-current and SS [9]. Moreover, a small hysteresis effect in this structure is achieved.

Technology Computer-Aided Design (TCAD) also provides a powerful way to predict device performance. High bandgap materials use TCAD to construct a suitable process and device structure and is a low-cost way to set up a pre-study procedure. A nitrogen ion implantation, along with an annealing process converting thin film normally on Al-GaN/GaN structures into normally off devices is simulated and discussed in [10]. TCAD simulation also help us to understand the device's physical operation mechanism. Offset, LDD (lightly doped drain), GOLDD (gate overlapped lightly doped drain) and RSD (raised source drain) structures are common designs to reduce a device's electric field and improve the kink effect and leakage current. TCAD helps researchers to design a new device frame. An RSD and vertical LDD concept in TFTs are discussed in regard to different structure simulations [11]. The performance of more complicated thin film transistors can also be predicted by the TCAD simulation procedure.

For circuit application, most organic semiconductors exhibit p-type properties, unlike 2D materials and most oxide semiconductors; those are almost n-type devices. P-type structures are very important for the fabrication of CMOS inverters. Furthermore, their simple synthesis process allows them to be fabricated on flexible devices. Carbon nanotubes (CNT) used in TFTs have attracted great attention for their printable synthesis method and p-type semiconductor characteristics. However, CNT is still limited due to inadequate air stability and limited tunability. Gunhoo Woo et al. [12] discuss the emerging materials for thin film transistors and the methods of using hybrid thin film material combinations for complementary integration circuit implementation in detail. A capping process with transparent hexagonal boron nitride offers a feasible approach to implement both n and p type semiconductors [3]. Those provide some ways to achieve digital circuits by TFTs.

In conclusion, the above contributions show the recent developments in the area "Thin Film Transistor" research. This Special Issue includes the emerging materials and related process technologies to improve device performance, and the need for further development in the TFTs field.

**Author Contributions:** Conceptualization, F.-T.C.; writing—original draft preparation, F.-T.C.; writing—review and editing, F.-T.C.; supervision, F.-T.C.; data curation, Y.-W.C. and J.-C.L.; All authors have read and agreed to the published version of the manuscript. **Funding:** This research was funded by Ministry of Science and Technology, Taiwan, grant number MOST 110-2221-E-035-088.

**Conflicts of Interest:** The authors declare no conflict of interest.

## References

1. Liu, W.-S.; Hsu, C.-H.; Jiang, Y.; Lai, Y.-C.; Kuo, H.-C. Improving Device Characteristics of Dual-Gate IGZO Thin-Film Transistors with Ar–O<sub>2</sub> Mixed Plasma Treatment and Rapid Thermal Annealing. *Membranes* **2022**, *12*, 49. [[CrossRef](#)] [[PubMed](#)]
2. Li, Q.; Dong, J.; Han, D.; Wang, Y. Effects of Channel Thickness on Electrical Performance and Stability of High-Performance InSnO Thin-Film Transistors. *Membranes* **2021**, *11*, 929. [[CrossRef](#)] [[PubMed](#)]
3. Yue, D.; Rong, X.; Han, S.; Cao, P.; Zeng, Y.; Xu, W.; Fang, M.; Liu, W.; Zhu, D.; Lu, Y. High Photoresponse Black Phosphorus TFTs Capping with Transparent Hexagonal Boron Nitride. *Membranes* **2021**, *11*, 952. [[CrossRef](#)] [[PubMed](#)]
4. Liu, Y.; Liu, C.; Qin, H.; Peng, C.; Lu, M.; Chen, Z.; Zhao, Y. Steep Subthreshold Swing and Enhanced Illumination Stability InGaZnO Thin-Film Transistor by Plasma Oxidation on Silicon Nitride Gate Dielectric. *Membranes* **2021**, *11*, 902. [[CrossRef](#)] [[PubMed](#)]
5. Lin, W.-Y.; Chien, F.-T.; Chiu, H.-C.; Sheu, J.-K.; Hsueh, K.-P. Effects of Thermal Annealing on the Properties of Zirconium-Doped Mg<sub>x</sub>Zn<sub>1-x</sub>O Films Obtained through Radio-Frequency Magnetron Sputtering. *Membranes* **2021**, *11*, 373. [[CrossRef](#)] [[PubMed](#)]
6. Yang, H.; Liang, Z.; Fu, X.; Xu, Z.; Ning, H.; Liu, X.; Lin, J.; Pan, Y.; Yao, R.; Peng, J. Application of Amorphous Zirconium-Yttrium-Aluminum-Magnesium-Oxide Thin Film with a High Relative Dielectric Constant Prepared by Spin-Coating. *Membranes* **2021**, *11*, 608. [[CrossRef](#)] [[PubMed](#)]
7. Lee, S. An Empirical Modeling of Gate Voltage-Dependent Behaviors of Amorphous Oxide Semiconductor Thin-Film Transistors including Consideration of Contact Resistance and Disorder Effects at Room Temperature. *Membranes* **2021**, *11*, 954. [[CrossRef](#)] [[PubMed](#)]
8. Avis, C.; Jang, J. Understanding the Origin of the Hysteresis of High-Performance Solution Processed Polycrystalline SnO<sub>2</sub> Thin-Film Transistors and Applications to Circuits. *Membranes* **2022**, *12*, 7. [[CrossRef](#)] [[PubMed](#)]
9. Kang, T.-K.; Lin, Y.-Y.; Liu, H.-W.; Lin, C.-L.; Chang, P.-J.; Kao, M.-C.; Chen, H.-Z. Improvements of Electrical Characteristics in Poly-Si Nanowires Thin-Film Transistors with External Connection of a BiFeO<sub>3</sub> Capacitor. *Membranes* **2021**, *11*, 758. [[CrossRef](#)] [[PubMed](#)]
10. Sheu, G.; Song, Y.-L.; Susmitha, D.; Issac, K.; Mogarala, R. A Novel Nitrogen Ion Implantation Technique for Turning Thin Film “Normally On” AlGaIn/GaN Transistor into “Normally Off” Using TCAD Simulation. *Membranes* **2021**, *11*, 899. [[CrossRef](#)] [[PubMed](#)]
11. Chien, F.-T.; Ye, J.; Yen, W.-C.; Chen, C.-W.; Lin, C.-L.; Tsai, Y.-T. Raised Source/Drain (RSD) and Vertical Lightly Doped Drain (LDD) Poly-Si Thin-Film Transistor. *Membranes* **2021**, *11*, 103. [[CrossRef](#)] [[PubMed](#)]
12. Woo, G.; Yoo, H.; Kim, T. Hybrid Thin-Film Materials Combinations for Complementary Integration Circuit Implementation. *Membranes* **2021**, *11*, 931. [[CrossRef](#)] [[PubMed](#)]