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Influence of N_2/O_2 Partial Pressure Ratio during Channel Layer Deposition on the Temperature and Light Stability of a-InGaZnO TFTs

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Abstract: The electrical characteristics of amorphous InGaZnO (a-IGZO) thin film transistors (TFTs) deposited with different N_2/O_2 partial pressure ratios ($P_{N/O}$) are investigated. It is found that the device with 20% $P_{N/O}$ exhibits enhanced electrical stability after positive-bias-stress temperature (PBST) and negative-bias-stress illumination (NBSI), presenting decreased threshold voltage drift (ΔV_{th}). Compared to the N-free TFT, the average effective interface barrier energy (E_τ) of the TFT with 20% $P_{N/O}$ is increased from 0.37 eV to 0.57 eV during the bias-stress process, which agrees with the suppressed ΔV_{th} from 3.0 V to 1.12 V after the PBS at T = 70 °C. X-ray photoelectron spectroscopy analysis revealed that the enhanced stability of the a-IGZO TFT with 20% $P_{N/O}$ should be ascribed to the control of oxygen vacancy defects at the interfacial region.

Keywords: a-IGZO TFTs; stability; N_2/O_2 partial pressure ratio; oxygen vacancy

1. Introduction

Transparent metal oxide-based thin film transistors (TFTs) have attracted substantial attention as backplane technology for next-generation active matrix display applications. In particular, amorphous InGaZnO (a-IGZO) TFTs have been extensively studied because they show attractive characteristics including desirable channel electron mobility, large-area uniformity, and low off-state leakage compared with conventional a-Si:H TFTs [1,2]. However, high density localized states originating from oxygen vacancies (O_V) exist within the bandgap of the a-IGZO active layer due to the disordered amorphous nature, which would considerably degrade the device performance and reliability [3,4]. It has been demonstrated that the threshold voltage instability in a-IGZO TFTs induced by electrical, light, and thermal stress is generally related to the O_V defects trapping electrons or holes within the a-IGZO active layer and at the device interface region [5–7]. Hence, suppressing the O_V defects in the active layer or at the interface is crucial to enhance the reliability of a-IGZO TFTs.

In previous reports, the nitrogen has been used to passivate O_V-related defects within a-IGZO by forming N-metal (In, Ga and Zn) bonds [8,9]. For example, the ambient stability of N-doped a-IGZO TFTs can be enhanced by the mitigation of the oxygen absorption/desorption behavior due to the substitution of the O atom by an N atom within the a-IGZO [10]. Moreover, the a-IGZO TFTs fabricated with N-doped a-IGZO layer inserted at the a-IGZO/SiO_2 interface exhibit superior bias stability, which is improved by the passivation of the interface O_V defects [11]. However, excess N incorporation into the a-IGZO channel layer would induce extra O_V-related defects or N-related defects within the active layer or at the channel/dielectric interface, which would cause the degradation of device performance and electrical reliability [12,13]. In this work, to achieve an optimal level of nitrogen doping in the active layer, a-IGZO TFTs with various nitrogen/oxygen partial pressure ratios ($P_{N/O}$) during active layer deposition are fabricated. The electrical characteristics of the fabricated devices are investigated under positive-bias-stress temperature (PBST) and negative-bias-stress illumination (NBSI). The TFT fabricated with a proper $P_{N/O}$ exhibits improved reliability with decreased threshold voltage drift (ΔV_{th}) after PBST and NBSI conditions. Such improvements are related to the passivation of O_V defects at the a-IGZO/SiO_2 interface.

2. Experiments

The inverted staggered TFTs structure are fabricated in this work. Firstly, a 200 nm SiO_2 gate insulator layer is prepared on a heavily doped n-Si substrate by plasma enhanced chemical vapor deposition (PECVD). Next, the channel layer of a 45 nm a-IGZO film is grown by dc reactive sputtering. During the a-IGZO film sputtering process, the Ar flow rate is set to 30 sccm, and the gas mixing ratio of $N_2/(O_2 + N_2)$ is set to 0%, 20%, and 40% under a total sputtering pressure of 5×10^{-3} Torr. Then, the TFTs active region with a channel width/length of 100 µm/20 µm are fabricated by photolithography and wet chemical etching. Next, the drain/source (Ti/Au) contact electrodes and passivation layer (100 nm SiO_2) are prepared successively. Lastly, the fabricated devices are annealed at 300 °C in air for 1 h. The inset of Figure 1 shows the cross-sectional schematic of the fabricated TFT.

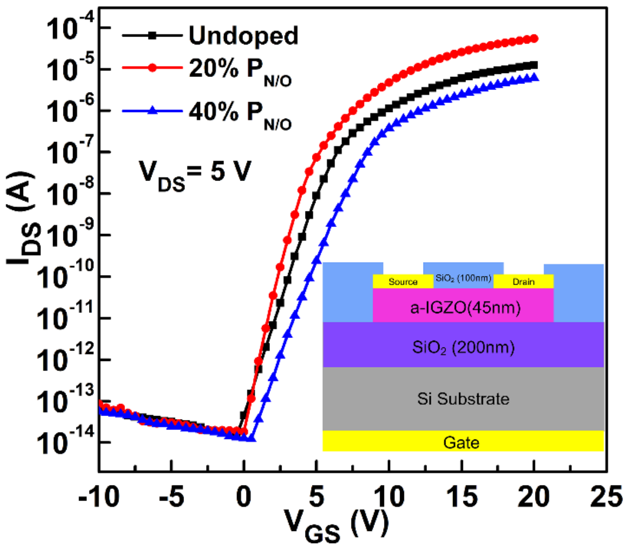

Figure 1. The transfer characteristics of the a-IGZO thin film transistors (TFTs) fabricated with different nitrogen/oxygen partial pressure ratios ($P_{N/O}$). The inset shows the schematic of the fabricated TFTs structure.

3. Results and Discussion

Figure 1 shows the transfer characteristics of the a-IGZO TFTs fabricated with 0%, 20%, and 40% $P_{N/O}$. The corresponding device parameters are extracted in Table 1. In this study, the V_{th} is determined by the gate voltage (V_{GS}) at which the drain current (I_{DS}) reaches 10 nA. The subthreshold swing (SS) can be calculated by the equation:

$$SS = \left[\frac{\partial \log(I_{DS})}{\partial V_{GS}}\right]^{-1} \quad (1)$$

Table 1. Extracted electrical parameters of the a-IGZO TFTs with different $P_{N/O}$.

$P_{N/O}$ (%)	V_{th} (V)	μ_{FE} (cm^2/Vs)	SS (V/dec)	$I_{on/off}$
0	5.0	2.2	0.8	$>10^8$
20	3.8	8.0	0.6	$>10^9$
40	7.0	1.2	0.9	$>10^7$

It can be seen that the V_{th} and SS of the a-IGZO TFT with 20% $P_{N/O}$ are improved than that of the undoped a-IGZO TFT, where the V_{th} is decreased from 5.0 V to 3.8 V, and the SS is reduced from 0.8 V/dec to 0.6 V/dec. It has been demonstrated that the V_{th} and SS in TFTs are mainly associated with the density of trap states in the active region and at the a-IGZO/SiO_2 interface [14]. Therefore, the improved electrical properties of a-IGZO TFT fabricated with 20% $P_{N/O}$ can be determined by the decrease of trap density in the device active region. In contrast, the V_{th} and SS of the a-IGZO TFT with 40% $P_{N/O}$ are increased, which indicates that the new trap states are generated by excess N-doping.

The reliability of the a-IGZO TFTs with different $P_{N/O}$ are evaluated by positive-bias-stress temperatures. During the bias stress process, the devices are applied at V_{GS} = 15 V for 5000 s at T = 30 °C, 50 °C, and 70 °C, respectively. Figure 2a–c selectively show the transfer characteristics for the a-IGZO TFTs with different $P_{N/O}$ against the PBS time at T = 70 °C. The transfer curves of the TFTs show a parallel shift toward the positive direction with no apparent degradation in SS and field effect mobility (μ_{FE}) after PBS, which indicates that the ΔV_{th} of the TFTs after PBS should be ascribed to the field-induced electron trapping at the a-IGZO/SiO_2 interface [5,11]. Meanwhile, it is clearly observed that the a-IGZO TFT with 20% $P_{N/O}$ apparently exhibits better electrical stability compared with the undoped and 40% $P_{N/O}$ devices after PBST at T = 70 °C. Correspondingly, the ΔV_{th} of the a-IGZO TFT fabricated with 20% $P_{N/O}$ (1.12 V) is lower than that of the undoped a-IGZO TFT (3.0 V) and 40% $P_{N/O}$ device (2.75 V).

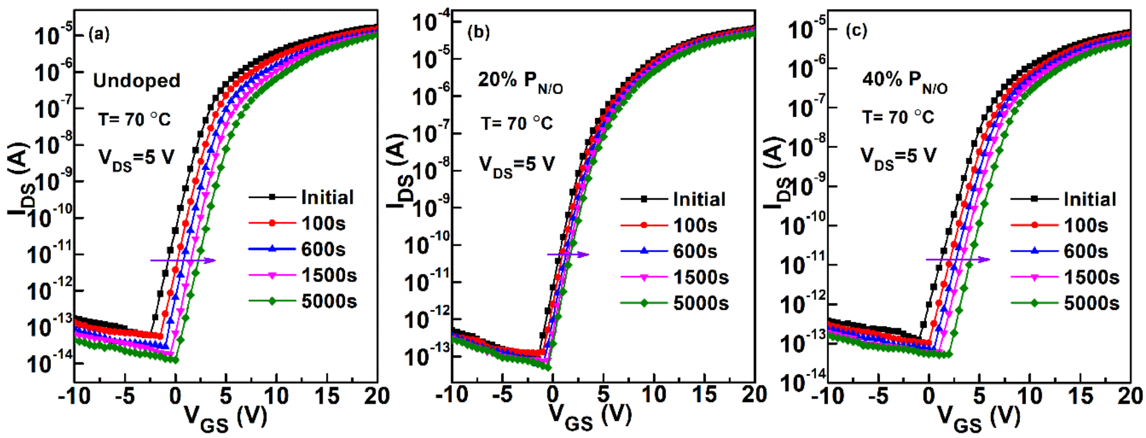

Figure 2. Evolution of the transfer curves against positive bias stress (PBS) time for the a-IGZO TFTs fabricated using $P_{N/O}$ of (**a**) 0% at T = 70 °C, (**b**) 20% at T = 70 °C, and (**c**) 40% at T = 70 °C.

Figure 3a–c show the quantity of the ΔV_{th} for the a-IGZO TFTs with different $P_{N/O}$ against the bias-stress time at different temperatures. It is observed that the relationship between ΔV_{th} and time is fitted by a stretched-exponential equation, which reveals the mechanism of the carrier trapping near the active layer/dielectric interface [15,16]. The stretched-exponential function is described as below

$$\Delta V_{th} = \Delta V_{th0}\left\{1 - exp\left[-(t/\tau)^{\beta}\right]\right\} \quad (2)$$

where Δ_{Vth0} is the ΔV_{th} at infinite stressing time, β is a stretched-exponential exponent, and τ is the time content for the charge trapping process, which is given by $\tau = \tau_0 exp(E_\tau/k_B T)$. In this expression, E_τ is the average effective interface energy barrier, which needs to exceed for channel carrier to inject into the device interface region or insulator. To investigate the effect of N-doping on the carrier trapping process in the a-IGZO TFTs, the E_τ is extracted by the Arrhenius plot of τ. As shown in Figure 3d, a good linear relationship in the lnτ-1000/T plots is observed, which indicates that the carrier trapping process in the a-IGZO TFT is thermally activated [15]. Meanwhile, the E_τ of the a-IGZO TFT with 20% $P_{N/O}$ (0.57 eV) is increased to that of the undoped a-IGZO TFT (0.37 eV). The increased E_τ suggests that fewer channel carriers can be trapped into the a-IGZO/SiO_2 interface or insulator during the bias-stress process and the corresponding device exhibits better bias-stress stability. On the contrary, compared with the a-IGZO TFT with 20% $P_{N/O}$, the E_τ of the a-IGZO TFT with 40% $P_{N/O}$ is decreased to 0.43 eV, which means that the interface quality is degraded when excess N is incorporated into the a-IGZO active layer. Therefore, the results indicate that the drift of V_{th} for the a-IGZO TFTs could be mitigated by the moderate N-doping.

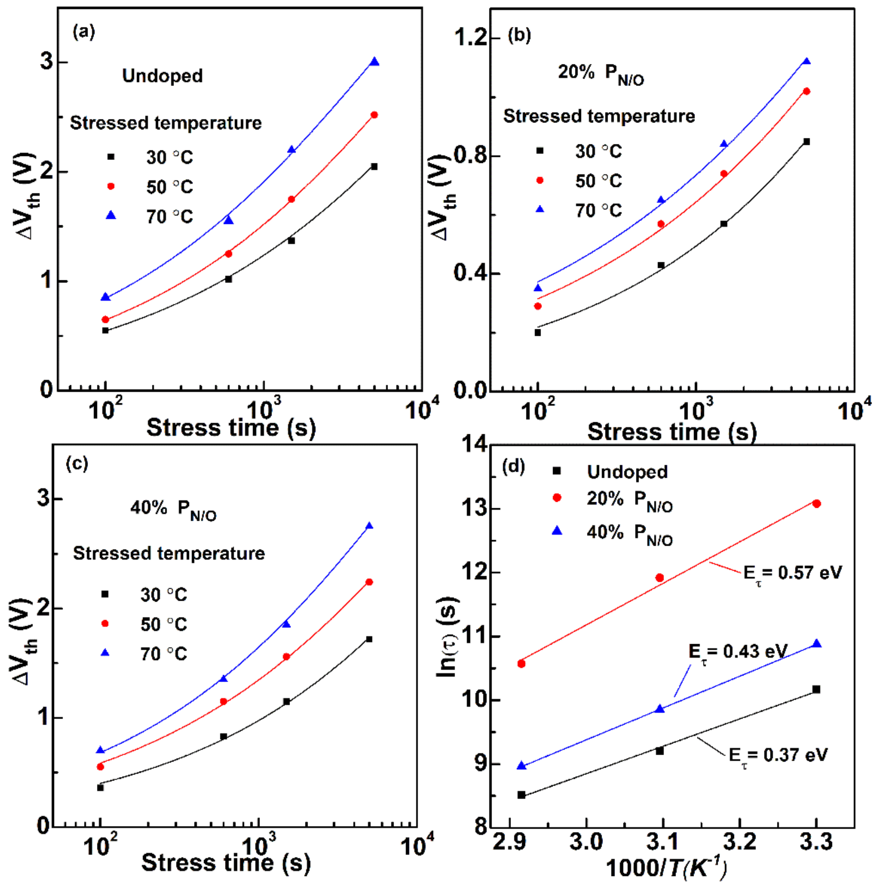

Figure 3. Time dependence of threshold voltage drift (ΔV_{th}) for the a-IGZO TFTs fabricated using $P_{N/O}$ of (**a**) 0%, (**b**) 20%, (**c**) 40% at different stress temperatures, and (**d**) Stress time constant lnτ as a function of the reciprocal temperature.

In addition, in real applications, switching TFTs are usually negatively biased for keeping off-state and exposed to light emitted from the backlight in active-matrix displays [17,18]. Thus, the electrical reliability of the TFTs fabricated with different $P_{N/O}$ is also evaluated by negative- bias-stress illumination (NBSI). Figure 4a–c show the transfer curves of the a-IGZO TFTs fabricated with different $P_{N/O}$ against NBS time under white light illumination, in which the device is stressed at $V_{GS} = -15$ V for 5000 s. The transfer curves of the TFTs exhibit a shift toward negative gate voltage direction with no apparent change in SS and μ_{FE} after the NBSI condition, which indicates that the negative shift of V_{th} should be determined by photo-induced holes trapped into the a-IGZO/SiO_2 interface [19,20]. Meanwhile, as shown in Figure 4a,b, it is clear that the negative shift of V_{th} is decreased from 3.0 V to 1.1 V for N-free a-IGZO TFT and 20% $P_{N/O}$ a-IGZO TFT after 5000 s NBSI, which means that the a-IGZO/SiO_2 interface quality is improved by N-doping. However, as shown in Figure 4c, the a-IGZO TFT with 40% $P_{N/O}$ exhibits a large negative shift of V_{th} (2.65 V) compared with TFT with 20% $P_{N/O}$ after 5000 s NBIS, which indicates that additional defects are generated at the a-IGZO/SiO_2 interface by heavy N-doping.

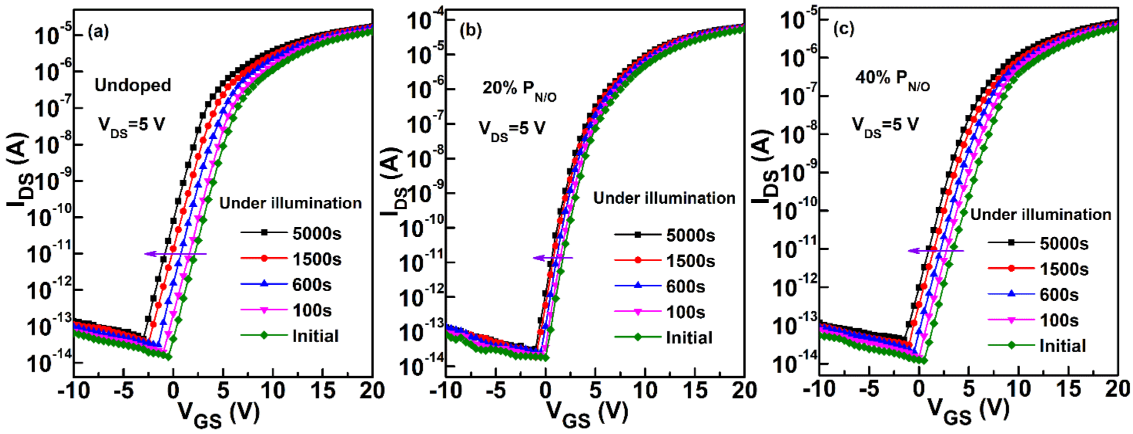

Figure 4. Evolution of the transfer curves against negative bias stress (NBS) time under white light illumination for the a-IGZO TFTs fabricated using $P_{N/O}$ of (**a**) 0%, (**b**) 20%, and (**c**) 40%.

To reveal the mechanism of the effect of N-doping on the reliability of the a-IGZO TFTs, the chemical properties of the a-IGZO, a-IGZO: 20% $P_{N/O}$, and a-IGZO: 40% $P_{N/O}$ films are analyzed by the X-ray photoelectron spectroscopy (XPS) measurement. The deconvolution of XPS spectra of O 1s is shown in Figure 5a–c. The combined O 1s peak could be divided into three components by Gaussian fitting, which is located at 530.1 eV (O_I), 531.3 eV (O_{II}), and 532.4 eV (O_{III}), respectively. The peaks of O_I, O_{II}, and O_{III} are associated with the oxygen ions in the lattice surrounded by Ga, In, and Zn atoms, O_V and oxygen in hydroxide (O_{OH}), respectively [11,21]. Thus, the relative amount of O_V existing in the a-IGZO film can be calculated by the proportion of the peak area O_V to the whole area O 1s (O_{whole}). As shown in Figure 5a,b, it can be seen that the area ratio of O_{II}/O_{whole} is clearly reduced from 35% to 25% for the undoped a-IGZO film and a-IGZO: 20% $P_{N/O}$ film, indicating that the O_V is suppressed by N-doping. In contrast, compared with the a-IGZO: 20% $P_{N/O}$ film, the O_V rises to 31% in a-IGZO: 40% $P_{N/O}$ film as shown in Figure 5c, suggesting that the extra O_V is generated when excess nitrogen atoms are incorporated into the a-IGZO film. This result agrees with previous reports that heavy N-doping in the a-IGZO film could suppress the bonding of O and Ga because of the facilitated formation of N-Ga bonds, which could result in the increase of O_V within the a-IGZO film. Besides, as shown in Figure 5d, the N 1s spectrum of the a-IGZO: 20% $P_{N/O}$ film is fitted by two energy bonds centered at 395.7 eV and 397.3 eV corresponding to the Ga Auger and N-Ga bonds [22], respectively. Thus, the XPS analysis reveals that the enhanced reliability of the a-IGZO TFT with moderate $P_{N/O}$ is determined by passivating the O_V at the a-IGZO/SiO_2 interface.

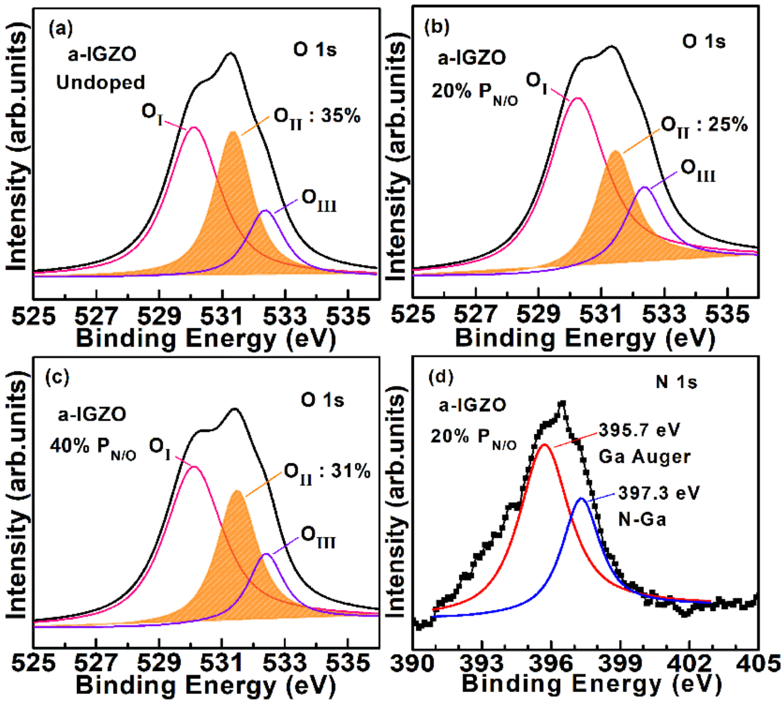

Figure 5. O 1s XPS spectra of the a-IGZO films grown using $P_{N/O}$ of (**a**) 0%, (**b**) 20%, (**c**) 40%, and (**d**) N 1s XPS spectra of a-IGZO film grown with 20% $P_{N/O}$.

4. Conclusions

In this work, the effect of different $P_{N/O}$ during the a-IGZO layer deposition on the electrical properties of a-IGZO TFTs is investigated. It is found that the electrical performances of a-IGZO TFT with 20% $P_{N/O}$ are improved. Correspondingly, the device shows considerably enhanced electrical stability after PBST and NBSI conditions, with a significantly suppressed threshold voltage drift. According to XPS analysis, the concentration of O_V defects in the a-IGZO with moderate $P_{N/O}$ film exhibits an apparent decrease, which causes the increased E_τ of the a-IGZO TFT. Thus, the enhanced reliability of the a-IGZO TFT with moderate $P_{N/O}$ is ascribed to the suppressed V_O defects at the a-IGZO/SiO_2 interface.

Author Contributions: X.H. fabricated and measured all the TFT devices. D.Z. and W.X. designed the experiments and provided valuable discussions and suggestions. The manuscript was written by X.H., and was revised by all the authors.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **2004**, *432*, 488. [CrossRef] [PubMed]
2. Yabuta, H.; Sano, M.; Abe, K.; Aiba, T.; Den, T.; Kumomi, H.; Nomura, K.; Kamiya, T.; Hosono, H. High-mobility thin-film transistor with amorphous $InGaZnO_4$ channel fabricated by room temperature rf-magnetron sputtering. *Appl. Phys. Lett.* **2006**, *89*, 112123. [CrossRef]
3. Nomura, K.; Kamiya, T.; Yanagi, H.; Ikenaga, E.; Yang, K.; Kobayashi, K.; Hirano, M.; Hosono, H. Subgap states in transparent amorphous oxide semiconductor, In-Ga-Zn-O, observed by bulk sensitive X-ray photoelectron spectroscopy. *Appl. Phys. Lett.* **2008**, *92*, 202117. [CrossRef]

4. Kamiya, T.; Nomura, K.; Hosono, H. Origins of High Mobility and Low Operation Voltage of Amorphous Oxide TFTs: Electronic Structure, Electron Transport, Defects and Doping. *J. Disp. Technol.* **2009**, *5*, 468–483. [CrossRef]
5. Suresh, A.; Muth, J.F. Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors. *Appl. Phys. Lett.* **2008**, *92*, 033502. [CrossRef]
6. Chowdhury, M.D.; Migliorato, H.P.; Jang, J. Time-temperature dependence of positive gate bias stress and recovery in amorphous indium-gallium-zinc-oxide thin-film-transistors. *Appl. Phys. Lett.* **2011**, *98*, 153511. [CrossRef]
7. Huang, X.M.; Wu, C.F.; Lu, H.; Ren, F.F.; Xu, Q.Y.; Ou, H.L.; Zhang, R.; Zheng, Y.D. Electrical instability of amorphous indium-gallium-zinc oxide thin film transistors under monochromatic light illumination. *Appl. Phys. Lett.* **2012**, *100*, 243505. [CrossRef]
8. Kim, C.E.; Yun, I. Effects of nitrogen doping on device characteristics of InSnO thin film transistor. *Appl. Phys. Lett.* **2012**, *100*, 013501. [CrossRef]
9. Abliz, A.; Gao, Q.; Wan, D.; Liu, X.; Xu, L.; Liu, C.; Jiang, C.; Li, X.; Chen, H.; Guo, T.; et al. Effects of Nitrogen and Hydrogen Codoping on the Electrical Performance and Reliability of InGaZnO Thin-Film Transistors. *ACS Appl. Mater. Interfaces* **2017**, *9*, 10798–10804. [CrossRef] [PubMed]
10. Liu, P.T.; Chou, Y.T.; Teng, L.F.; Li, F.H.; Shieh, H.P. Nitrogenated amorphous InGaZnO thin film transistor. *Appl. Phys. Lett.* **2011**, *98*, 052102. [CrossRef]
11. Huang, X.M.; Wu, C.F.; Lu, H.; Ren, F.F.; Chen, D.J.; Zhang, R.; Zheng, Y.D. Enhanced bias stress stability of a-InGaZnO thin film transistors by inserting an ultra-thin interfacial InGaZnO:N layer. *Appl. Phys. Lett.* **2013**, *102*, 193505. [CrossRef]
12. Liu, P.T.; Chang, C.H.; Fuh, C.S.; Liao, Y.T.; Sze, S.M. Effects of Nitrogen on Amorphous Nitrogenated InGaZnO (a-IGZO:N) Thin Film Transistors. *J. Disp. Technol.* **2016**, *12*, 1070–1077. [CrossRef]
13. Raja, J.; Jang, K.; Balaji, N.; Yi, J. Suppression of temperature instability in InGaZnO thin-film transistors by in situ nitrogen doping. *Semicond. Sci. Technol.* **2013**, *28*, 115010. [CrossRef]
14. Raja, J.; Jang, K.; Balaji, N.; choi, W.; Trinh, T.T.; Yi, J. Negative gate-bias temperature stability of N-doped InGaZnO active-layer thin-film transistors. *Appl. Phys. Lett.* **2013**, *102*, 083505. [CrossRef]
15. Lee, J.M.; Cho, I.T.; Lee, J.H.; Kwon, H.I. Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in InGaZnO thin film transistors. *Appl. Phys. Lett.* **2008**, *93*, 093504. [CrossRef]
16. Seo, S.J.; Jeon, J.H.; Hwang, Y.H.; Bae, B.S. Improved negative bias illumination instability of sol-gel gallium zinc tin oxide thin film transistors. *Appl. Phys. Lett.* **2011**, *99*, 152102. [CrossRef]
17. Goto, T.; Imaizumi, F.; Sugawa, S. Improvement in the Negative Bias Illumination Stress Stability for Silicon-Ion Implanted Amorphous InGaZnO Thin-Film Transistors. *IEEE Electron Device Lett.* **2017**, *38*, 345. [CrossRef]
18. Billah, M.M.; Chowdhury, M.D.H.; Mativenga, M.; Um, J.G.; Mruthyunjaya, R.K.; Heiler, G.N.; Tredwell, T.J.; Jang, J. Analysis of Improved Performance Under Negative Bias Illumination Stress of Dual Gate Driving a-IGZO TFT by TCAD Simulation. *IEEE Electron Device Lett.* **2016**, *37*, 735. [CrossRef]
19. Ji, K.H.; Kim, J.I.; Mo, Y.G.; Jeong, J.H.; Yang, S.; Hwang, C.S.; Park, S.H.K.; Ryu, M.K.; Lee, S.Y.; Jeong, J.K. Comparative Study on Light-Induced Bias Stress Instability of IGZO Transistors with SiN_x and SiO_2 Gate Dielectrics. *IEEE Electron Device Lett.* **2010**, *31*, 1404–1406. [CrossRef]
20. Kim, E.; Jang, W.J.; Kim, W.; Park, J.; Lee, M.K.; Park, S.K.; Choi, K.C. Suppressed Instability of a-IGZO Thin-Film Transistors Under Negative Bias Illumination Stress Using the Distributed Bragg Reflectors. *IEEE Trans. Electron Devices* **2016**, *63*, 1066–1071. [CrossRef]
21. Yang, S.; Ji, K.H.; Kim, U.K.; Hwang, C.S.; Park, S.K.; Hwang, C.S.; Jang, J.; Jeong, J.K. Suppression in the negative bias illumination instability of Zn-Sn-O transistor using oxygen plasma treatment. *Appl. Phys. Lett.* **2011**, *99*, 102103. [CrossRef]
22. Jiang, Y.; Wang, Q.; Zhang, F.; Li, L.; Zhou, D.; Liu, Y.; Wang, D.; Ao, J.P. Reduction of leakage current by O_2 plasma treatment for device isolation of AlGaN/GaN heterojunction field effect transistors. *Appl. Surf. Sci.* **2015**, *351*, 1155–1160. [CrossRef]