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Dynamic Behavior of a Sliding-Mode Control Based on a Washout Filter with Constant Impedance and Nonlinear Constant Power Loads

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Abstract: Power converters (PCs) with their control techniques help regulate voltages of nodes in microgrids with different types of loads such as resistive, inductive, nonlinear, constant power, or critical loads. However, constant power loads (CPLs) affect the stability of the voltage in the output of PCs and are usually difficult to regulate with traditional control techniques. The sliding-mode control (SMC) with the washout filter technique has been recently proposed to address this issue, but studies that consider the phenomenon and parameters present in real systems are required. Therefore, this paper focuses on evaluating the dynamic behavior of an SMC based on a washout filter using three different loads: A constant impedance load (CIL), a nonlinear CPL, and a combination of CIL and CPL. The CIL considered a resistance connected to the circuit, whereas the nonlinear CPL was designed by using a buck converter with zero average dynamics and fixed-point induction control techniques (ZAD-FPIC). The tests consisted of creating some variations in the reference signals to identify the output voltage and the error that the control brings according to the different loads. Besides, this study focuses on representing the dynamic behavior of signals when loads change, considering quantization effects, system discretization, delay effects, and parasitic resistors. Additionally, bifurcation diagrams are created by changing the control parameter *k* and plotting the regulated voltage and the error produced in the output signals. To illustrate the advantages of the SMC with the washout filter technique, a comparison was made with other techniques such as the proportional-integral-derivative (PID) and conventional SMC by varying the load. The results showed that SMC with the washout filter technique was superior to the PID and the conventional SMC because it stabilizes the signal faster and has a low steady-state error. Additionally, the control system regulates well the output voltage with the three types of load and the system remains stable when changing the parameter *k* for values greater than 1, with a low error in the steady-state operation.

Keywords: DC-DC power converters; constant impedance load; constant power load; sliding-mode control; washout filter; ZAD-FPIC

1. Introduction

Renewable energy is an important source in microgrids (MGs) [1,2], as it can help provide power to end users [3]. Power converters (PCs) are used to transfer power from these sources to users and help regulate voltage and improve energy efficiency [2,4]. The use of PCs in MGs has increased in recent years [5] and some electronic devices are now used to transfer power from alternating to direct

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current (AC-DC), and from direct to direct current (DC-DC) [6,7], forming different voltage levels in the network that must be controlled. Although, many stability problems have been studied in AC systems, the PCs can create unstable events in DC systems when the load changes [7]. Thus, this dynamic behavior is of great importance as the development of MGs continues, and better analysis must be performed.

Sliding-mode control (SMC) is a specific type of variable structure control (VSC), which was studied extensively during the 1970s. Its widespread use is mainly due to its advantages over parameter variations and tolerance to disturbances [8]. The main feature of VSC is sliding motion, which is when the system state repeatedly crosses certain subspaces or sliding hyperplanes [9]. Moreover, washout filters are extensively used to control chaotic systems and have recently been used in PCs in conjunction with SMC controllers [10]. Some authors have proposed the use of SMC with washout filters [11,12] as a good option to control the output voltage regarding load variations. The idea when implementing a washout filter in a PC is to ensure some robustness under variations in the constant power load (CPL) via filtering the inductor current.

Particularly in [11], nonlinear stability analysis of a standalone DC network and an SMC based on a washout filter is used to maintain constant DC bus voltage. In this case, the authors show the behavior of the system with the controller under nonlinear load variations. Besides, in [12], an SMC with a washout filter is used to regulate the DC bus voltage under constant impedance load (CIL) and constant power load (CPL). They also determined the operating limits of the controlled system in terms of the maximum power drained by the CPL and CIL connected to the bus. In [13], the authors study stability issues in DC MGs with instantaneous CPL, as this load introduces a destabilizing effect in DC MGs that brings significant oscillations of the voltages or reaches system collapse. Some strategies, such as load shedding, addition of resistive loads, filters or energy storage directly connected to the main bus, and control methods, are applied.

Commonly, studies do not compare the control performance to different types of loads and, especially, nonlinear CPLs. CPL loads have the characteristic of negative incremental impedance, which may cause system instability during disturbances if the system is not properly controlled [14]. Hence, when feeding a CPL by a buck converter, the results show that the open-loop control is unstable in continuous conduction mode (CCM). Therefore, the system will have additional restrictions on the control in comparison to a purely resistive load [15]. Many techniques have been developed to compensate the system, e.g., damping, small-signal analysis, Lyapunov stability, linearized feedback, droop mode control, filters, vector control, *d*–*q* frame analysis, and SMC. However, the authors of [16] reveal that there are three stabilization techniques used to compensate the negative impedance of CPL: the Feeder side, intermediate circuits, and load side. On the other hand, the authors of [17] classify the compensation techniques into passive and active damping, space pole placement control, pulse adjustment control, SMC, model predictive control, and feedback linearization.

Papers found in the literature show that few studies consider phenomena and parameters present in real systems and do not consider bifurcation diagrams to evaluate the performance of the buck converter. Therefore, this paper focuses on studying the dynamic behavior of an SMC based on a washout filter to control the voltage when the load is formed by a combination of CIL and CPL. The voltage reference signal was changed to evaluate the response of the controller to different types of load. To perform the test, an electronic circuit was modeled and simulated that considers internal resistances, system discretization, quantization effects, and delay effects in order to study a more realistic circuit as in [18,19]. Finally, a numerical bifurcation was performed by changing the parameters k with the aim of visualizing the nonlinear effects of the circuit and the load. All these tests were validated by measuring the voltage in the output bus (v_c).

Contributions of this paper with respect to the literature are as follows: 1) The dynamic behavior of the SMC is evaluated with different types of load; 2) quantization, system discretization, parasitic resistors, and delay effects are modeled to obtain closer results to real circuits; 3) a buck converter with a quasi-sliding control technique is used as a CPL load, which converts it to a nonlinear CPL; 4)

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unstable zones and steady-state errors are obtained to evaluate the system stability when the control parameters are changed; 5) bifurcation diagrams for the output voltage and voltage error are used to evaluate the response of the controller in the steady-state operation under changes in the control parameter k; and 6) comparisons among the proportional–integral–derivative (PID), conventional SMC, and SMC with a washout filter are performed with variations in CIL and CPL. Therefore, the materials and methods used in this research along with the mathematical fundamentals, simulations, and simulated electronic circuit are presented in Section 2. The results, analysis, and discussion are included in Section 3, and Section 4 presents the conclusions.

2. Materials and Methods

Next, the mathematical models of the network elements and power controller are presented. Thus, the SMC that considers the washout filter is included with the detailed information needed to study the effects on the controller. Besides, an electronic circuit is modeled to simulate the effects of load changes and evaluate the effects created in the network with voltage reference variations. Finally, bifurcation diagrams are plotted to evaluate the stability of the electric circuit with different loads.

2.1. Microgrid

AC-DC and DC-DC PCs are used to transfer power to the different loads in the MG [12], as shown in Figure 1. DC-DC PCs are used to connect sources, such as photovoltaic panels and batteries, to the input bus (Bus 1). AC-DC PCs are used to connect wind generators and the power grid to the input bus (Bus 1). Furthermore, a buck converter is used to connect the system to other buses and regulate load nodes such as the DC-DC PC connected between Bus 1 and Bus 2 in Figure 1. The last PC is an SMC with a washout filter (identified in Figure 1 as PC SMC). The final stage in this circuit considers the loads as a CIL connected directly to the DC voltage and a CPL formed by a PC with zero average dynamics and fixed-point induction control techniques (ZAD-FPIC), identified in Figure 1 as PC ZAD-FPIC.

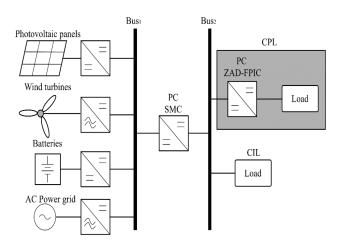


Figure 1. Simplified power network feeding direct current (DC) loads.

2.2. Simplified Model of the Network

Figure 2 shows the DC distribution network implemented to analyze the different effects of the load variation. The converter has a power source with voltage E and an internal source resistor r_s , which represent the equivalent circuit of different energy sources and their internal impedance connected to Bus 1, as shown in Figure 1. A metal–oxide–semiconductor field-effect transistor (MOSFET) works as a switch S, with an internal MOSFET resistance r_M , diode D with forward voltage diode V_{fd} , filter LC, internal resistance of inductor r_L , and resistance used to measure current r_{Med} . Finally, Bus 2 represents the output of the circuit where the load is connected (CPL and CIL).

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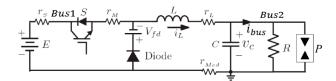


Figure 2. Circuit model of the buck power converter (PC) connected to the constant impedance load (CIL) (*R*) and constant power loads (CPLs) (*P*).

A diagram of the pulse width modulation (PWM) controller connected to the buck converter and the sensors used to measure the different input signals is presented in Figure 3. An SMC with a washout filter is used to regulate the output signal. The response to the dynamics created according to the load variation (CPL and CIL) can be regulated by this SMC.

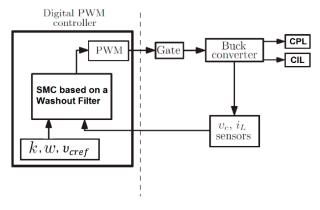


Figure 3. Block diagram of the buck converter with the pulse width modulation (PWM) controller used for the simulation.

This circuit was used to represent the mathematical and numerical models that are solved to identify the variations and response of the system. Model parameters that help represent the system are discretization, quantization, and delay effects as those obtained for real circuits.

Figure 4 shows the complete diagram implemented in MATLAB-Simulink (version R2019a, The MathWorks, Natick, MA, USA) to control the buck converter using the SMC with a washout filter. The quantization effects are included as 12 bits for the voltage in the condenser v_c and the current in the inductor i_L . A delay period was included in the numerical simulation equal to 1/Fc. The zero-order-hold block is necessary to simulate the fixed sample time and obtain v_c and i_L , and the calculation of u is explained in the following mathematical model. All parameters of the buck converter and the SMC controller are shown in Table 1.

| Parameter | Description | Value |
|-----------|-------------------------------------|-------------------------------|
| R | Resistance of the load | $20.44 \Omega, 40.092 \Omega$ |
| С | Capacitance | 938 µf |
| L | Inductance | 53.35 mH |
| r_L | Internal resistance of the inductor | $1.33~\Omega$ |
| r_{Med} | Sensor resistance | $1.007~\Omega$ |
| r_{M} | Internal resistance of the MOSFET | $0.3~\Omega$ |
| r_s | Internal resistance of the source | $0.3~\Omega$ |
| E | Input voltage | 40 V (Dual source) |
| Fc | Commutation frequency | variable |

Table 1. Parameters of the circuit used in the direct current (DC) test.

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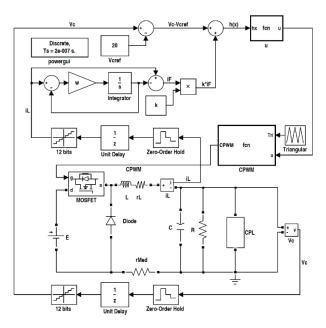


Figure 4. Diagram of the global system for the simulation.

2.3. Mathematical Model of the Controller

Then, the total current supplied by the electrical circuit is equal to the sum of the current in the CIL and the current in the CPL, as shown in Equation (1):

$$i_{bus} = \frac{v_c}{R} + \frac{P}{v_c},\tag{1}$$

where i_{bus} is the current supplied by the circuit, R is the constant resistance of the CIL, P is the active power of the CPL, and v_c is the voltage of the capacitor. The equivalent resistance of the circuit can be obtained according to the voltage and the current in the bus, as expressed in Equation (2):

$$R_{eq} = \frac{v_c}{i_{bus}}. (2)$$

2.4. Dynamics of Buck Converter (PC SMC)

The mathematical models used to represent the dynamics of a buck converter feeding the CIL and CPL are presented in Equations (3) and (4):

$$L\frac{di_L}{dt} = uE - v_c - (r_s + r_M + r_{Med} + r_L)i_L, \tag{3}$$

$$C\frac{dv_c}{dt} = i_L - \frac{v_c}{R} - \frac{P}{v_c}.$$
 (4)

In these equations, L is the inductor, C is the capacitor, v_c is the instantaneous voltage of the capacitor, and i_L is the instantaneous current of the inductor. As defined previously in the model, the term E is the voltage of the power source, r_s is the internal source resistor, r_M is the internal MOSFET resistance, r_L is the internal resistance of the inductor, and r_{Med} is the resistance used to measure current. The term R represents the constant resistance of the load connected to the bus, P is the active power of the load, and u is used to represent the switching function with values $\{0,1\}$.

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2.5. Voltage Measurement

The voltage in Bus 2 can be measured and used as an input for the SMC. This can be represented as v_m and is equal to the voltage at Bus 2 and the capacitor voltage:

$$v_m = v_c = V_{Bus2}. (5)$$

This value will change according to the regulation of the SMC with a washout filter. The final voltage magnitude depends on the voltage reference and the regulation limits allowed in the circuit.

2.6. Washout Filter

This method consists of passing the inductor current i_L through a washout filter, as shown in Figure 4. After the filter, a transfer function is used to obtain the final signal I_F or the filtered inductor current. The transfer function G_F is then used to obtain the new filtered current, as expressed in Equation (6) [12]. Herein, the term s corresponds to the Laplace expression and w is the cut-off frequency of the high-pass filter:

$$G_F(s) = \frac{I_F(s)}{I_L(s)} = \frac{s}{s+w} = 1 - \frac{w}{s+w}.$$
 (6)

After the induction current is filtered, a differential equation is created and added to the model, as expressed in Equation (7) [11,12], where z is obtained from the integration of Equation (7) [20]:

$$\frac{dz}{dt} = w(i_L - z). (7)$$

2.7. Sliding-Mode Control

The circuit shown in Figure 4 has an SMC that receives two signals: v_c , corresponding to the capacitor voltage, and I_F , which is the filtered inductor control coming from the washout filter. Then, a control law is applied to determine the final output signal, depending on the two switching stages, as shown in Equation (8) [12], where u is a scalar that depends on x and can take two values: $u^- = 0$ and $u^+ = 1$. Thus, two conditions are presented depending on the conditions of the output of the function h(x) with $x = \{i_L, v_c, z\}$:

$$u = \begin{cases} u^{-} = 0, \\ u^{+} = 1, \end{cases} if \quad h(x) > 0$$
 (8)

The system obtains the response of h(x) that is defined in Equation (9) [12]. In this equation, v_c corresponds to the capacitor voltage, v_{cref} is the voltage reference required to regulate the system, i_L is the inductor current, and z is the current difference obtained in the output of the circuit. The term k is a parameter used in the controller that multiplies the filtered current and takes a value greater than zero (k > 0). This parameter k can be adjusted in the controller to obtain the different responses of the system and will change to identify the dynamics of the system:

$$h(x) = v_c - v_{cref} + k(i_L - z) = 0.$$
 (9)

The continuous conduction mode of the system is presented considering Equations (10) and (11). First, when the switch is in the ON state, the resulting equations of the current, voltage, and z are as shown in Equation (10):

$$f^{+}(x) = \begin{bmatrix} i_{L} \\ i_{L} \\ v_{c} \\ z \end{bmatrix}_{u=1} = \begin{bmatrix} \frac{1}{L} (uE - v_{c} - (r_{s} + r_{M} + r_{Med} + r_{L}) i_{L}) \\ \frac{1}{C} (i_{L} - \frac{v_{c}}{R} - \frac{P}{v_{c}}) \\ w(i_{L} - z) \end{bmatrix}.$$
(10)

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When the switch is OFF, a vector field is presented with the new equations of the inductor current, capacitor voltage, and *z*, as shown in Equation (11):

$$f^{-}(x) = \begin{bmatrix} \stackrel{\bullet}{i_L} \\ \stackrel{\bullet}{v_c} \\ \stackrel{\bullet}{z} \end{bmatrix}_{\nu=0} = \begin{bmatrix} \frac{1}{L} \left(-v_c - (r_{Med} + r_L)i_L + v_{fd} \right) \\ \frac{1}{C} \left(i_L - \frac{v_c}{R} - \frac{P}{v_c} \right) \\ w(i_L - z) \end{bmatrix}. \tag{11}$$

2.8. Model of the CPL

The CPL considered is a buck converter, as presented in [21], where the final load is a resistance that is controlled by ZAD-FPIC techniques, which are widely used in other research [19]. This technique, proposed in [22], consists of defining a function and forcing an average value of zero at each sampling period [23]. Let us consider s(x(kT)) as a piecewise linear function of the state value and described by Equation (12) during a complete sampling period:

$$s(x(kT)) = v_c - v_{cref} + k_s (\dot{v_c} - \dot{v}_{cref}). \tag{12}$$

The mathematical description for the condition of zero average dynamics is given by (13). The piecewise function s(x(kT)) is required to obtain information from the state values v_c and i_L at the instant kT:

$$\int_{kT}^{(k+1)T} s(x(kT))dt = 0.$$
 (13)

Equation (13) is solved to obtain the duty cycle $d_{k(kT)}$ at each sampling time, which ensures the condition of zero average dynamics when applied to the system through switch S. The duty cycle was obtained in [21,22] with Equation (14) as the buck converter controlled by zero average dynamics (ZAD):

$$d_{k(kT)} = \frac{2s_1(kT) + T\dot{s}_-(kT)}{T(\dot{s}_-(kT) - \dot{s}_+(kT)}.$$
(14)

Then, the ZAD-FPIC techniques applied to the buck converter to obtain a new duty cycle are expressed in Equation (15) [24]:

$$d_{ZAD-FPIC}(kT) = \frac{d_k(kT) + Nd^*}{N+1}. (15)$$

Then, the term $d_k(kT)$ is obtained from Equation (14) and d^* can be calculated at the beginning of each period as in Equation (16):

$$d^* = d_k(kT)\big|_{steady\ state}. (16)$$

3. Results

The following results validate the nonlinear SMC based on a washout filter with the CIL (40 Ω) and CPL (10 W). For the simulation, the voltage reference and the control parameter k are changed to represent variations in the circuit. The results are presented to show the robustness of the control, the voltage regulation, and the transient response of the controller.

3.1. Regulation of DC-DC Signals

Comparisons among the circuits working with CIL, CPL, and CIL-CPL are performed, starting with the voltage regulation value $v_{cref}=32$ DC volts. The results shown below are simulated in discrete time and the parameters are given in Table 1; besides, voltage and current are measured with a sampling frequency in a fixed step equal to 5 kHz, a resolution of 12 bits, and a delay time of 1/5000 s. The chosen parameters of the LC filter are L=53 mH, C=938 μ F, and the switching frequency Fc=5 kHz, which cause a slower response time of the system; however, it maintains the voltage regulation

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within the limits with an error close to 3%. Figure 5 shows the behavior of the output voltage v_c and error for the different loads. Figure 5a shows that the voltage follows the reference signal $v_{cref} = 32 \text{ V}$ for the loads, and an overshoot of 12.5% is observed for the signal v_c when the load is CPL: 9.5% for CIL and 9% for CIL-CPL. The settling times are similar for the three signals and the steady-state errors are similar and lower than 1.5%, as shown in Figure 5b. These curves were created with the factor k = 4 and voltage reference $v_{cref} = 32 \text{ V}$.

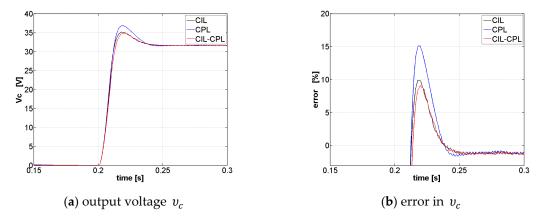


Figure 5. Simulated tests with k=4 and voltage regulation of $v_{cref}=32$ for loads CIL, CPL, and CIL-CPL.

Figure 6 shows the inductor currents for the three loads and transient behavior. The three currents have similar behavior in the transient and steady-state operations, changing only the final magnitude of the current as they vary according to the load.

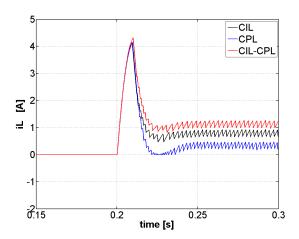


Figure 6. Inductor currents for the three loads.

The regulation of the DC-DC signals with various reference values allows for the identification of how the control system works and is a good indicator to compare and find similitude among the different loads. Figure 7a,b show the output signal v_c for the different loads plotted against time. The tests were performed considering various steps in the reference signals as $v_{cref}=10\,\mathrm{V}$ at times between 0.05 and 0.1 s; $v_{cref}=20\,\mathrm{V}$ at times between 0.1 and 0.2 s; and $v_{cref}=30\,\mathrm{V}$ at times between 0.2 and 0.3 s. These figures show that the regulation is similar for cases when the reference signal is increased or reduced. There are some small differences in the response times and the maximum peaks of the signal, having a longer settling time for the system with a CPL load. In the steady-state for the three tests, the error is lower than 4%. Figure 7b shows that the error is increased when the reference signal is close to zero. Therefore, the three tests in this research show that signals have similar regulation behaviors.

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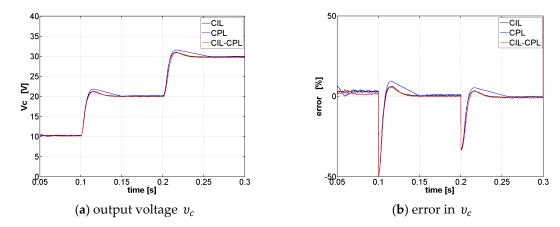


Figure 7. Behavior of the system for the three loads.

3.2. Bifurcation Diagrams

The bifurcation diagram is useful in dynamical systems because it shows the possible long-term values of a system (fixed points or periodic orbits) as a function of a bifurcation parameter. Besides, bifurcation diagrams allow the identification of operation zones and the stability limits of the system. To draw the bifurcation diagrams, the system must reach the equilibrium point, and the last values of the signal in steady-state operation are plotted. Figure 8a–c show the output signals of the circuit v_c for the three tests. These figures have been plotted with MATLAB-Simulink, considering a k between 0 and 5 to identify the behavior of the circuit and comparing the outputs for the three loads: CIL (40 Ω), CPL (10 W), and CIL-CPL.

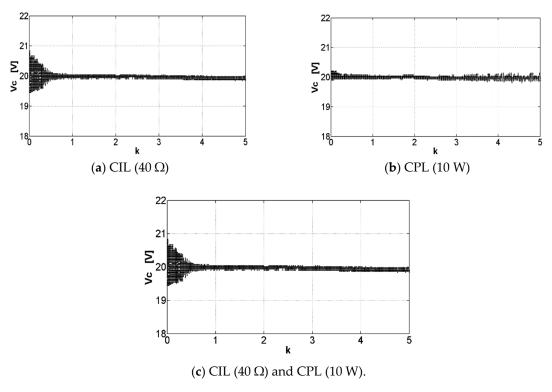


Figure 8. Bifurcation diagram of v_c vs. k.

In these figures, similar behaviors in the output voltages are observed when the parameter k is increased. For k values greater than 0.5, voltages are close to the reference signal v_{cref} . For values lower than k=0.3, the voltages are a little different in magnitude, but the values tend to the reference voltage v_{cref} .

Figure 9a–c show the errors obtained for the CIL, CPL, and CIL-CPL, respectively. The figures show that the system regulates with a greater steady-state error for all values of k. It is observed that the error is less than 2% for values of k greater than 0.5. However, the error is larger in the case where the load is CPL than for the other cases. From the figures, it is shown that a good choice of the parameter k to improve stability and regulation is a value close to 0.8.

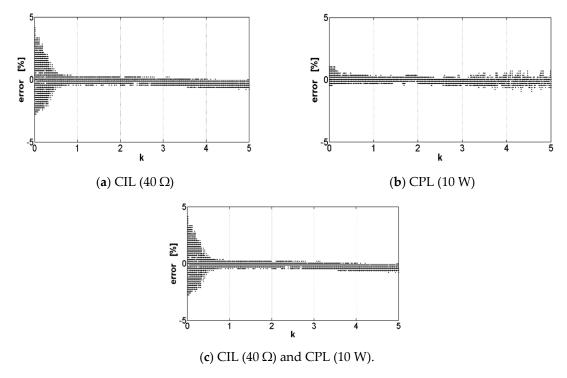


Figure 9. Bifurcation diagram of the *error* vs. *k*.

3.3. Comparison of Different Controllers

To show the advantages of the control technique used in this investigation, comparisons among PID, conventional SMC, and SMC with a washout filter are performed. The design of the PID controller and SMC, with the parameters of the buck converter, are explained in [25]. The results shown below are simulated in continuous time and some parameters have been changed with values such as $C=46~\mu\text{F}$, L=2.47~mH, and the switching frequency Fc=20~kHz. As the parameters of the LC filter are smaller, they let signals of higher frequency pass because the settling time in continuous time is much less than the settling time in discrete time (Figures 5–7), given in the previous results of this document.

Figure 10 shows the voltage v_c and error for the three controllers: PID, SMC, and SMC with the washout filter. Besides, this figure shows the response of the controllers when the loads are only CILs. The voltage and error are shown in Figure 10a,b when CIL = 10 Ω and CPL = 0 W; in Figure 10c,d when CIL = 25 Ω and CPL = 0 W; and in Figure 10e,f when CIL = 50 Ω and CPL = 0 W.

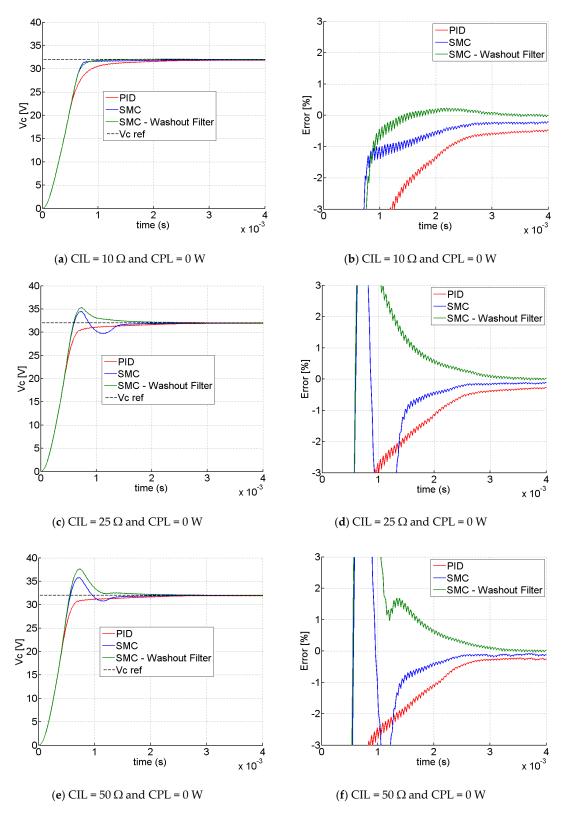


Figure 10. Voltage v_c and error for the CIL load and the three controllers: Proportional–integral–derivative (PID), sliding-mode control (SMC), and SMC with washout filter.

The settling time for the SMC with the washout filter is close to 2.5 ms; for the PID, it is 3 ms; and for the SMC, it is 2.5 ms, which show that they have similar behaviors. The highest overshoot is presented for the SMC with the washout filter with a value of 17.6%. The smallest error is presented

during the steady-state operation for the three loads when SMC with the washout filter is used, which makes it more suitable for regulating voltage signals in this type of system; however, the three controllers have steady-state errors less than 0.5% for the different load values.

Figure 11 shows the voltage behavior v_c and error for the three controllers: PID, SMC, and SMC with washout filter. Besides, Figure 11 shows the response of the controllers when the loads are CIL and CPL. The voltage and error are shown in Figure 11a,b when CIL = 25 Ω and CPL = 40 W; in Figure 11c,d when CIL = 25 Ω and CPL = 16 W; and in Figure 11e,f when CIL = 25 Ω and CPL = 8 W, respectively.

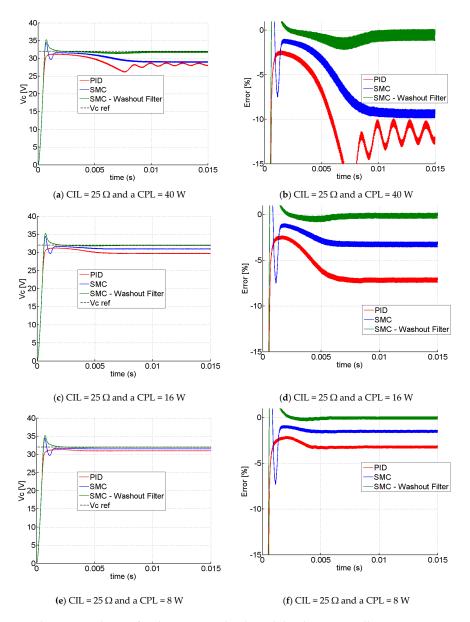


Figure 11. Voltage v_c and error for the CIL-CPL loads and the three controllers: PID, SMC, and SMC with washout filter.

The settling time for the SMC with the washout filter remains similar to that obtained previously and is close to 2.5 ms. For both the PID and conventional SMC, the value of the settling time obtained is around four times that obtained with the SMC with the washout filter. Regarding the settling time, it can be concluded that the SMC with the washout filter controller is capable of regulating the voltage faster when there are CPLs. The steady-state error for the three load variation tests shows that the SMC

with the washout filter behaves better than the other two controllers as the maximum error for the PID is close to 12%; for the conventional SMC, it is 10%; and for the SMC with the washout filter, it is less than 2% when CIL = 25Ω and CPL = 40 W. For the other load variations tested, the error for the SMC with the washout filter remains less than 1%, and for the other controllers, it is still greater than 2%.

4. Conclusions

This paper presented the nonlinear effects of an SMC based on a washout filter that considers CIL and CPL. For this purpose, an electronic circuit was modeled and simulated in MATLAB-Simulink to visualize the different nonlinear effects created when different types of loads are connected. The results show that the system regulates well the voltage with the three loads tested. The robustness of the system was checked by changing the control parameter k, obtaining a steady-state error less than 3%. Additionally, the quantization, system discretization, and delay effects present in real systems were modeled to obtain results closer to those obtained with real circuits and that can be used in future research. A buck converter with a quasi-sliding control technique was placed as a CPL load, realizing that the system does not present unstable zones and a high steady-state error, and that the steady-state error is a little greater than the other two loads when the parameter *k* changes. From the bifurcation diagrams, it was observed that when the control parameter was around 0.5, the operation was close to the limit. Therefore, it is recommended to increase this value to avoid entering the zone where the steady-state error is greater. In the comparison of the performance of the three controllers with load variations, it was observed that the three controllers regulate well the voltage at the output with CIL; however, if the load is a combination of CIL and CPL, then the only controller that regulates well the voltage signal with small setting times and low steady-state error is the SMC with the washout filter.

Further research will analyze the SMC in an MG environment, integrating the controllers with other types of PCs as DC-AC. Future work will also consider the integration of the filter with the main control of the MG and compare the control efficiency with other methods. A classification of nonlinear effects can also be performed based on a bifurcation analysis to identify the effectivity of the response of the controller and the dynamic behavior. In addition, experimental validation of the dynamic responses of the SMC with the washout filter is required to validate the benefits of the controller. Finally, theoretical and experimental research with three-phase loads and various types of motors may be controlled by using an SMC with a washout filter.

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