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Smart Fault-Tolerant Control System Based on Chaos Theory and Extension Theory for Locating Faults in a Three-Level T-Type Inverter

Kuei-Hsiang Chao *, Long-Yi Chang and Fu-Qiang Xu

Department of Electrical Engineering, National Chin-Yi University of Technology, No. 57, Sec. 2, Zhongshan Rd., Taiping Dist., Taichung 41170, Taiwan

* Correspondence: chaokh@ncut.edu.tw; Tel.: +886-4-2392-4505 (ext. 7272)

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Abstract: This study proposes a smart fault-tolerant control system based on the theory of Lorenz chaotic system and extension theory for locating faults and executing tolerant control in a three-level T-type inverter. First, the system constantly monitors the fault states of the 12 power transistor switches of the three-level T-type inverter; if a power transistor fails, the corresponding output phase voltage waveform is converted by a Lorenz chaotic system. Chaos eye coordinates are then extracted from a scatter diagram of chaotic dynamic states and considered as fault characteristics. The system then executes fault diagnosis based on extension theory. The fault characteristic value is used as the input signal for correlation analysis; thus, the faulty power transistor can be located and the fault diagnosis can be achieved for the inverter. The fault-tolerant control system can maintain the three-phase balanced output of the three-level T-type inverter, thereby improving the reliability of the motor drive system. The feasibility of the proposed smart fault-tolerant control system was assessed by conducting simulations in this study, and the results verified its feasibility. Accordingly, after the occurrence of the fault in power switches, the balanced three-phase output line voltage remained unchanged, and the quality of the output voltage was not reduced by using the integration of the proposed fault diagnosis system and fault-tolerant control system for a three-level T-type Inverter.

Keywords: chaos theory; extension theory; T-type converter; fault diagnosis; fault-tolerant control; conversion through Lorenz chaotic system; chaos eye

1. Introduction

Recent advances in renewable energy and electric vehicle technology have prompted the development of multilevel inverters [1–5]. Compared with that of a two-level inverter, the switch of a multilevel inverter is subjected to lower voltage stress and is associated with a lower output voltage change rate (dv/dt). Accordingly, multilevel inverters are suitable for applications requiring high power consumption. Such applications require a relatively high number of power transistors, thus increasing the difficulty of fault detection in inverters. The traditional fault diagnosis procedure for inverters entails the use of information (numeric or waveform) directly measured by instruments. The information is examined by on-site personnel, who subsequently conduct fault diagnosis for the inverters, repair the inverters, and replace components on the basis of their experience. However, this traditional fault diagnosis procedure is prone to erroneous fault point detections, causing unnecessary waste of labor and time for component repair and replacement [6–8]. To improve the reliability of equipment using motor drive systems, researchers have invested considerable effort in exploring fault detection mechanisms [9–19] and fault-tolerant control strategies [20–23] for multilevel inverters in order to enable early fault detection when inverter power semiconductor components fail; this can thus maintain the inverter operation and minimize damage.

Currently, primary techniques for smart fault diagnosis in inverters include model-based methods, expert systems, and machine learning systems. Although model-based methods are useful [9], they require the establishment of various fault-state models in advance. Moreover, such models should consider the values of snubber capacitance and balance resistor in inverters, which are difficult to obtain. The models comprise various parasitic elements that would inevitably require some assumptions and thus impose limitations to the general applicability of the models [10,11]. In addition, expert systems can modify themselves. Nevertheless, the entire systems should still be established by experts; therefore, such systems are associated with relatively high costs [12]. Finally, machine learning systems [13] notably mimic the neural network of the human brain. Through such neural connections, data models can be updated using backpropagation, and hidden layers can reduce the dependence of machine learning algorithms on feature engineering. However, a large body of data is required for neural network learning to make accurate judgments, and the corresponding operating time is long [14–17]. Therefore, developing new smart fault diagnosis systems with high accuracy, easy implementation, and fast response is imperative. The first author has previously used the extension theory to diagnose the type and number of fault modules in a photovoltaic module array [24]. This method measures the voltages, currents and powers of the photovoltaic module array at each moment, and then accordingly estimates the type and number of faulted modules in the photovoltaic module array. Although its fault diagnosis accuracy is very high, the input of this evaluation method must be a fixed single point value. Therefore, this method is not suitable for fault diagnosis where the input variables are continuous functions or waveforms. Based on this, we must first use another intelligent method like chaos theory to convert the three-phase voltage waveforms obtained in T-type multilevel inverters into equivalent characteristic values (chaos eye coordinates), where the fault diagnosis can be made by the extension theory.

Multilevel inverters exhibit numerous advantages, such as various control modes, relatively low transistor withstand voltage levels, low current harmonics, and high frequency conversion efficiency. Such inverters have been widely used in high-voltage and high-power applications, including high-voltage dc transmission, superconducting energy storage, and motor frequency control. However, applications, such as military equipment, power systems, steel mills, and electric vehicles have particularly high requirements for continuous equipment operation. Consequently, inverter failure during operation would engender severe economic losses and even casualties. Improving inverter system reliability is thus imperative. Fault-tolerant control is among the primary methods for improving inverter system reliability. However, after prolonged use, multilevel inverters may break down because of switch damage induced by overcurrent (or high temperature) operation [18], component aging, and drive circuit failure. Multilevel inverter systems must thus be equipped with fault detection mechanisms and fault-tolerant control capabilities to ensure continued operation in failure events [8,20,21]. The fault-tolerant control strategies proposed in [22,23] showed that the maximum renewable energy capture can be achieved. However, these methods are only applicable to power systems. However, the purpose of the fault-tolerant control system for multilevel inverters is to ensure continued inverter operation in the event of power transistor failure. Therefore, to maintain the three-phase balance of the output voltage of the inverter, the power transistor switching state and the phase angle of the reference voltage in the pulse width modulation (PWM) control mechanism must be modified simultaneously. However, this process would increase the difficulty of designing and controlling the fault tolerance of a multilevel inverter in a failure event. In addition, the maximum output voltage amplitude of current fault-tolerant control systems is only 0.577 times that achieved under normal operation [6].

This study proposes a smart fault-tolerant control system for locating faults in a three-level T-type inverter; the system is based on an artificial intelligence algorithm incorporated with chaos theory [25] and extension theory [26]. First, the output phase voltage waveform observed during an event of power transistor failure is converted according to the dynamic states of Lorenz chaotic system; chaos eye coordinates are extracted from a scatter diagram of chaotic states and used as feature values

for fault detection. Extension theory is applied to locate a faulty power transistor. Subsequently, an external backup power transistor (leg) and 3 three-pole ac semiconductor switches (triode AC, TRAIC) are used for fault-tolerant control to maintain the three-phase balanced line voltage output, thereby maintaining the normal voltage amplitude if any power semiconductor switch of the inverter fails. Figure 1 illustrates the overall architecture of the proposed fault-diagnosis and fault-tolerant control system.

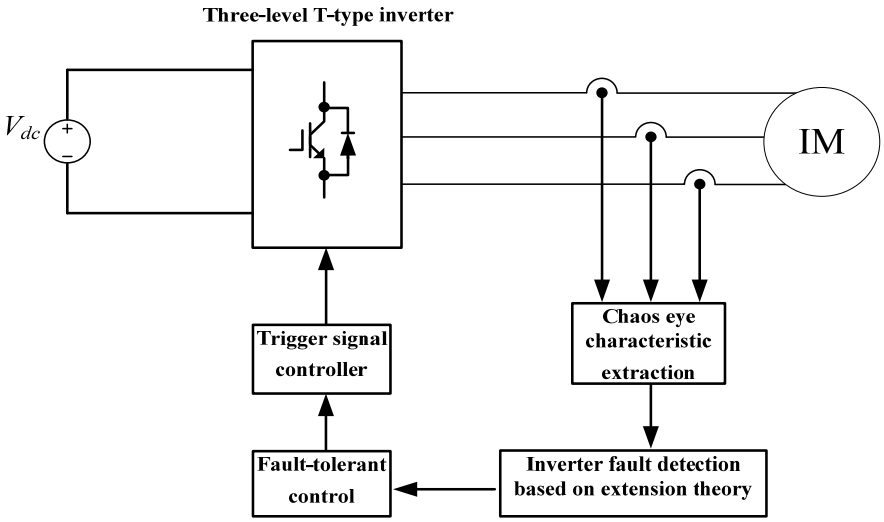


Figure 1. The architecture of fault-tolerant control system for a three-level T-type inverter.

This paper is organized as follows. In Section 2, the concepts of Chaos and Extension theory are described in detail, and how to use them for fault diagnosis of a three-level T-type inverter is explained. Then, the simulation is made in Section 3 to demonstrate the effectiveness of the proposed fault diagnosis method based on Chaos and Extension theory. Final, in Section 4, the fault-tolerant control in the event of any power switch failure in the three-level T-type inverter is analyzed, and then the simulation is used to prove its feasibility.

2. Materials and Methods

2.1. Fault Characteristics of Three-Level Inverter

To explore inverter fault diagnosis, this study considered a three-level T-type inverter, as shown in Figure 2. The faults of such an inverter can be divided into three types: Short-circuit fault, open-circuit fault, and an erroneous trigger signal. A short-circuit fault occurs when switching elements break down, due to excessive voltages across the switch. Moreover, an open-circuit fault occurs when switches cannot be activated, due to the lack of trigger signals for the power transistor. Finally, an erroneous trigger signal occurs when switching elements receive incorrect trigger signals.

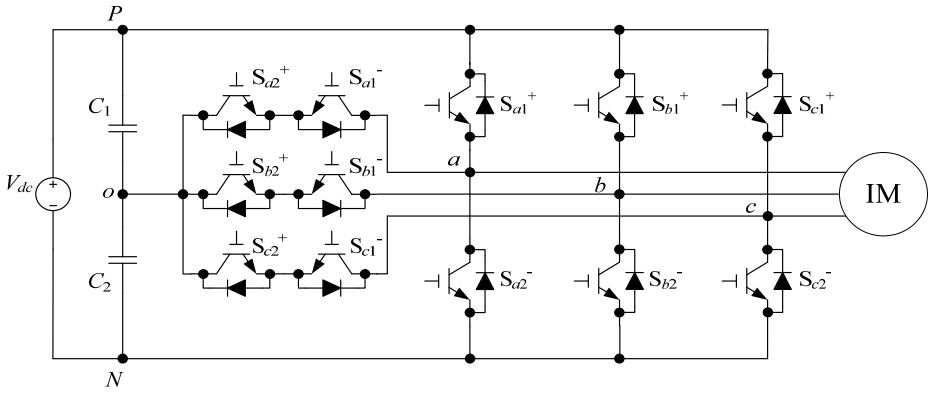


Figure 2. The architecture of three-level T-type inverter.

This study established a simulation environment for the three-level T-type inverter by using PSIM software and monitored the failure of the inverter switches constantly. Consider, for example, an output voltage frequency of 60 Hz. The simulated waveform for a normally operating inverter should exhibit a three-phase balanced structure, and the output voltage waveform of each phase is presented in Figure 3. The voltage waveforms of the three phases have the same shape and size, and the phase difference between them is 120°, which is an inherent characteristic of a three-phase balanced structure. This balanced structure would be distorted in the event of inverter switch failure. For example, if the inverter switch $S_{a1}{}^{+}$ fails, the waveform of the *a*-phase output voltage (v_{ao}) is distorted (Figure 4). Similarly, if the inverter switch $S_{b2}{}^{-}$ or $S_{c1}{}^{+}$ fails, the waveforms of the phase voltage v_{bo} and v_{co} would substantially differ from those observed under normal inverter switch operation. According to these observations, the output voltage waveform would be distorted when a fault occurs in an inverter.

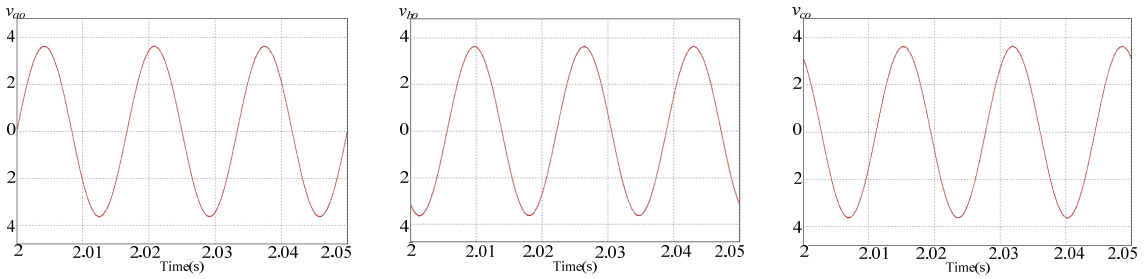


Figure 3. The output voltage waveforms of three phases of inverter operating at output voltage frequency of 60 Hz and under conditions of normal switch operation: (**a**) Phase voltage v_{ao}; (**b**) phase voltage v_{bo}; (**c**) phase voltage v_{co}.

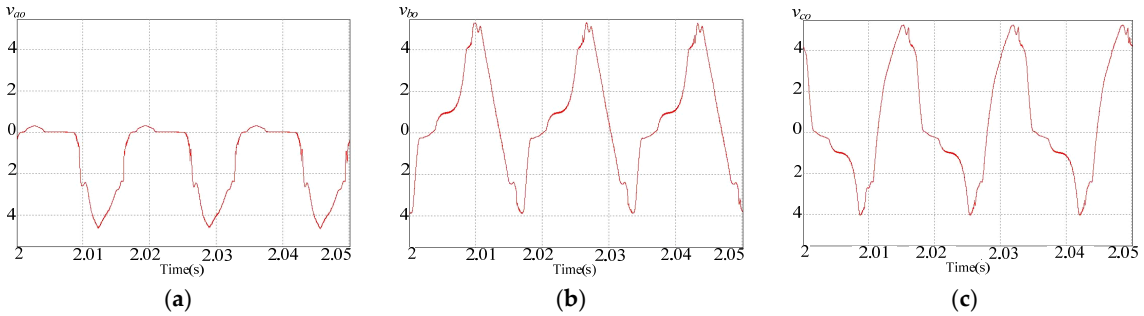


Figure 4. The output voltage waveform of three phases of inverter operating at 60 Hz and under conditions of faulty $S_{a1}{}^{+}$ operation: (**a**) Phase voltage v_{ao}; (**b**) phase voltage v_{bo}; (**c**) phase voltage v_{co}.

2.2. Theory of the Lorenz Chaotic System

A Lorenz chaotic system is considered in the proposed system [25], which is presented in Equation (1).

$$S_{cs} = \left\{ \begin{array}{l} \dot{x}_1 = \alpha(x_2 - x_1) \\ \dot{x}_2 = \beta x_1 - x_1 x_3 - x_2 \\ \dot{x}_n = x_1 x_2 - \gamma x_3 \end{array} \right\}, \quad (1)$$

where x represents the initial value of the system and can be used as the input value to be tested. α, β, and γ represent adjustment coefficients.

The three-phase voltage waveforms shown in Figures 3 and 4 are measured with voltage sensors. At the same time, the sampling time is 5 us and 10,000 data have been obtained within 0.05 s and then input into the Lorenz chaotic system in Equation (1). The adjustment coefficients α, β, and γ in Equation (1) are set to 10, 28, and 8/3, respectively. Through the aforementioned Lorenz chaotic system, $\dot{x}_1$, $\dot{x}_2$, and $\dot{x}_3$ can be obtained. In the proposed system, $\dot{x}_1$ and $\dot{x}_2$ are used to generate a chaotic states scatter diagram, as illustrated in Figure 5, with the two centroid points in the scatter diagram serving as chaos eyes. The coordinates of the chaos eyes can serve as feature values for inverter fault diagnosis.

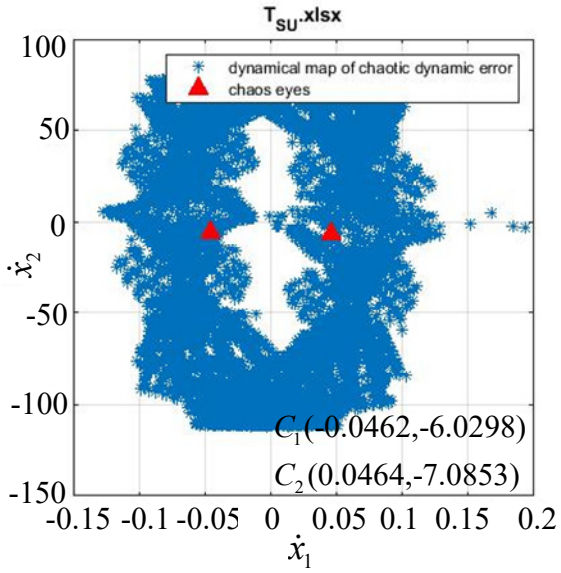
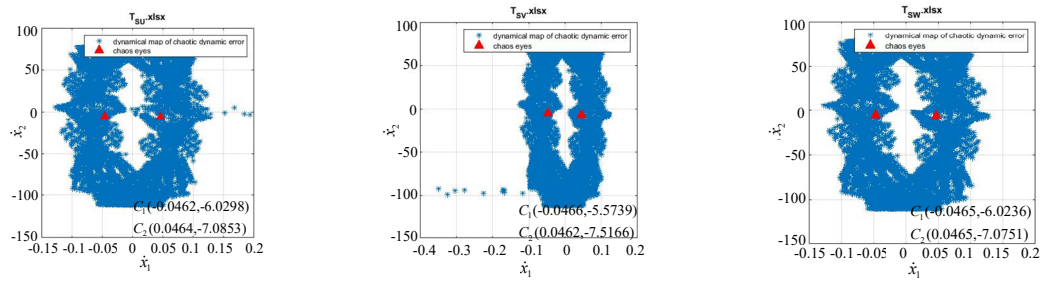


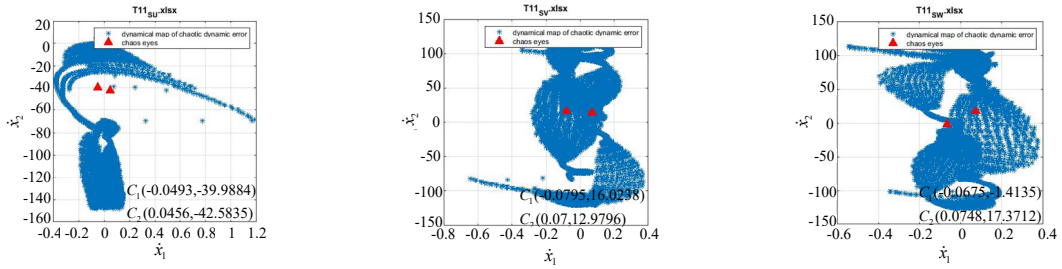
Figure 5. Chaotic states scatter diagram and corresponding chaos eyes.

For the conditions described in Figures 3 and 4, the corresponding waveforms can be converted through the Lorenz chaotic system to yield the chaotic scatter states diagrams displayed in Figures 6 and 7, respectively. The chaos eye coordinates in Figure 6a are C_1 (−0.0462, −6.0298) and C_2 (0.0464, −7.0853), whereas those in Figure 7a are C_1 (−0.0493, −39.9884) and C_2 (0.0456, −42.5835). After the occurrence of a fault, the Y-axis coordinates of the chaos eye are considerably different from those (v_{ao}) observed before the fault; thus, ${S_{a1}}^+$ can be suspected to be faulty. The proposed system can consider values of voltage waveforms of equal frequencies as the input for fault detection. After the use of the Lorenz chaotic system to convert the waveforms, the chaos eye coordinates (C_1 and C_2) in the resulting chaotic states scatter diagrams can be considered as the fault characteristic values. However, because of the failure of other transistors, chaos eye coordinates of v_{ao} observed before the occurrence of a fault might differ from those observed after the occurrence of the fault. The chaos eye coordinates are not fixed values; instead, they are distributed in a range. Therefore, the extension method is used for fault diagnosis to locate a fault in transistor switches.



(**a**) (**b**) (**c**)

Figure 6. Chaotic scatter diagrams of each phase voltage of the inverter operating at 60 Hz and under normal switch operation: (**a**) Phase voltage v_{ao}; (**b**) phase voltage v_{bo}; (**c**) phase voltage v_{co}.



(**a**) (**b**) (**c**)

Figure 7. Chaotic scatter diagrams of each phase voltage of the inverter operating at 60 Hz and under conditions of a faulty ${S_a1}^+$: (**a**) Phase voltage v_{ao}; (**b**) phase voltage v_{bo}; (**c**) phase voltage v_{co}.

2.3. Inverter Fault Diagnosis Based on Extension Theory

In 1983, the Chinese scholar Wen Cai proposed extension theory. The concept is to investigate the extension and contradictions of a matter from qualitative and quantitative perspectives. Matter element theory and extension mathematics constitute the two core components of extension theory. Matter element theory primarily describes the extension and transformation characteristics of matter elements, whereas extension mathematics comprises the core concepts of extension set and correlation function for calculation [26]. Extension theory expresses the information of matter through the matter element model and illustrates the relationship between matter quality and quantity through matter element transformation. Subsequently, the effects of quality and quantity on the matter are investigated using the correlation function to demonstrate the degree of influence of matter characteristics.

2.3.1. Concept of Extension Matter

In extension theory, a matter-element R contains three fundamental elements: matter name (N), matter characteristic (C), and values of matter characteristic (V). The model can be mathematically represented as follows:

$$\mathrm{R} = (\mathrm{N}, \mathrm{C}, \mathrm{V}), \tag{2}$$

where R is the basic element describing the matter (i.e., the matter element); N, C, and V are three elements that constitute the matter element. N represents the name of the matter, C represents the characteristic of the matter, and V represents the characteristic value of the matter. In extension matter element theory, if the matter element characteristic is not a single item, it is represented by x characteristics and x corresponding characteristic values. Accordingly, the characteristic can be

expressed in vector form as $C = [c_1, c_2, \ldots, c_x]$, and the corresponding characteristic value can be expressed as $V = [v_1, v_2, \ldots, v_x]$. Therefore, Equation (2) can be rewritten as follows.

$$R = \begin{bmatrix} R_1 \\ R_2 \\ \vdots \\ R_x \end{bmatrix} = \begin{bmatrix} N, & c_1 & v_1 \\ & c_2 & v_2 \\ & \vdots & \vdots \\ & c_x & v_x \end{bmatrix}. \tag{3}$$

If the characteristic value is in a certain interval, the interval is defined as a classical domain and is included in a neighborhood domain. Assume the following intervals: $F_0 = <a, b>$, $F = <d, e>$, and $F_0 \in F$; point f is any point in the interval F. Therefore, the matter element corresponding to $F_0 = <a, b>$ can be expressed as follows:

$$\begin{aligned} R_0 &= (F_0, C_i, V_i) \\ &= \begin{bmatrix} F_0, & c_1, & < a_1, b_1 > \\ & c_2, & < a_2, b_2 > \\ & \vdots & \vdots \\ & c_x, & < a_x, b_x > \end{bmatrix}, \end{aligned} \tag{4}$$

where C_i is the characteristic of F_0, and V_i is the characteristic value of C_i (i.e., its classical domain). The matter element R_F corresponding to F is presented in Equation (5), where C_j is the characteristic value of F and V_j is the characteristic value of C_j (i.e., its neighborhood domain).

$$\begin{aligned} R_F &= (F, C_j, V_j) \\ &= \begin{bmatrix} F, & c_1, & < d_1, e_1 > \\ & c_2, & < d_2, e_2 > \\ & \vdots & \vdots \\ & c_x, & < d_x, e_x > \end{bmatrix}. \end{aligned} \tag{5}$$

2.3.2. Distance and Position Value

Classical mathematics explores the distance relationship between points, and extension theory describes the relationship between a point and an interval in the real domain, as expressed in the following equation:

$$\Phi(f, F_0) = \left| f - \frac{v_a + v_b}{2} \right| - \frac{v_b - v_a}{2}. \tag{6}$$

In addition to considering the relationship between a point and an interval, the relationship between a point and two intervals or between intervals should be considered. Therefore, if $F_0 = <v_a, v_b>$ and $F = <v_d, v_e>$ are assumed to constitute two intervals in the real domain, and F_0 is in F, the position values of point f, F_0, and F can be expressed as follows:

$$D(f, F_0, F) = \begin{cases} \Phi(f, F) - \Phi(f, F_0) & , f \notin F_0 \\ -1 & , f \in F_0 \end{cases}. \tag{7}$$

2.3.3. Correlation Function

The correlation function, derived by dividing the distance by the position value, can be expressed as follows:

$$K(f) = \frac{\Phi(f, F_0)}{D(f, F_0, F)}. \tag{8}$$

If $f = (v_a + v_b)/2$, the correlation function has a maximum value and is called an elementary correlation function (Figure 8). In addition, if $K(f) < -1$, point f is outside the interval F. If $K(f) > 0$, point f is within the interval F_0. If $-1 < K(f) < 0$, point f is within the extension domain.

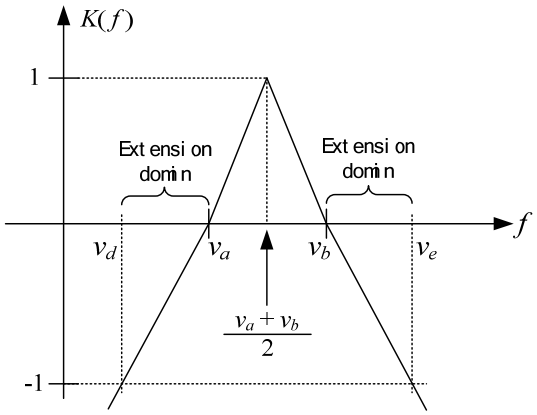


Figure 8. Schematic of the elementary correlation function.

The fault diagnosis steps involved in the extension method are described as follows.

Step 1. For each transistor failure, the chaos eye coordinates C_1 and C_2 on the chaos scatter diagram are used to establish the matter element model.

$$R_g = (F, C, V_p) = \begin{bmatrix} F_0 & C_1 & \langle x_1, y_1 \rangle \\ & C_2 & \langle x_2, y_2 \rangle \end{bmatrix}, g = 1, 2, \cdots, 12 \tag{9}$$

Step 2. The chaos eye coordinates of the faulty transistor to be determined, namely C_1 and C_2, are input into the model, and the resulting matter element model can be expressed as follows:

$$R_{new} = \begin{bmatrix} F_{new} & C_1 & V_{new1} \\ & C_2 & V_{new2} \end{bmatrix} \tag{10}$$

Step 3. The characteristics (C_1 and C_2) and their corresponding weights W_1 and W_2 (representing the relative importance of the characteristics) are determined. Here, $W_1 = W_2 = 0.5$.

Step 4. The degree of correlation between the fault categories of characteristics to be tested is calculated.

$$\lambda_g = \sum_{j=1}^{2} W_j K_{gj}, g = 1, 2, \cdots, 12 \tag{11}$$

Step 5. The largest correlation value of each fault category derived from the calculation represents the fault category to which a fault characteristic belongs. Therefore, the faulty transistor can be determined according to the category.

3. Simulation Results

To identify faulty power transistors, fault states were divided into nine categories in this study: Failure of $S_{a1}{}^{+}$; $S_{a2}{}^{-}$; $S_{b1}{}^{+}$; $S_{b2}{}^{-}$; $S_{c1}{}^{+}$; $S_{c2}{}^{-}$; ($S_{a1}{}^{-}$ or $S_{a2}{}^{+}$); ($S_{b1}{}^{+}$ or $S_{b2}{}^{+}$); and ($S_{c1}{}^{+}$ or $S_{c2}{}^{+}$). The principles underlying the categorization are described as follows. When $S_{a1}{}^{-}$ or $S_{a2}{}^{+}$ is faulty, the current path and voltage waveform are considered to be the same; thus, $S_{a1}{}^{-}$ and $S_{a2}{}^{+}$ are categorized under the same category. The same principle applies to the categories $S_{b1}{}^{+}$ or $S_{b2}{}^{+}$ and $S_{c1}{}^{+}$ or $S_{c2}{}^{+}$. Table 1 lists the fault categories.

Table 1. Power transistor fault categories.

Fault State	Category
Switch $S_{a1}{}^{+}$ fails	F_1
Switch $S_{a1}{}^{-}$ or $S_{a2}{}^{+}$ fails	F_2
Switch $S_{a2}{}^{-}$ fails	F_3
Switch $S_{b1}{}^{+}$ fails	F_4
Switch $S_{b1}{}^{-}$ or $S_{b2}{}^{+}$ fails	F_5
Switch $S_{b2}{}^{-}$ fails	F_6
Switch $S_{c1}{}^{+}$ fails	F_7
Switch $S_{c1}{}^{-}$ or $S_{c2}{}^{+}$ fails	F_8
Switch $S_{c2}{}^{-}$ fails	F_9

Table 2 presents the feature values of the chaos eyes for each phase under the switch failure state at an operating frequency of 60 Hz. The data in Table 2 were used as inputs in the established fault diagnosis system to execute fault detection. Tables 3–5 present the fault detection results, indicating that all faults could be correctly detected by the system. Consider, for example, the category F_2 (Table 2): The output weight determined for F_2 was the highest weight value (0.861617) (Table 3); thus, the fault was correctly identified to belong to F_2. To demonstrate the robustness of the proposed diagnostic system against interference, erroneous (±5%) test samples were considered at an operating frequency of 60 Hz, and the corresponding fault detection results are presented in Tables 6–8. The results indicated that after the consideration of errors, the proposed system could still correctly detect the fault category. Therefore, regardless of whether accurate or erroneous test data are used, the proposed system can correctly detect the fault category.

Table 2. Feature values of chaos eyes under various fault states (inverter frequency = 60 Hz).

Phase	Fault Category	C_1 *X* axis	C_1 *Y* axis	C_2 *X* axis	C_2*Y* axis
a-phase chaos eye feature value	F_1	−0.049	−39.988	0.046	−42.584
	F_2	−0.046	32.789	0.049	30.448
	F_3	−0.068	−1.429	0.075	17.557
	F_4	−0.074	−36.222	0.067	−11.218
	F_5	−0.079	15.843	0.069	13.017
	F_6	−0.07	−24.913	0.08	−31.164
	F_7	−0.06	−8.153	0.057	−4.901
	F_8	−0.08	15.631	0.07	13.255
	F_9	−0.052	−6.24	0.051	−6.531
b-phase chaos eye feature value	F_1	−0.08	−0.08	−0.08	−0.08
	F_2	−0.07	−0.07	−0.07	−0.07
	F_3	−0.049	−0.049	−0.049	−0.049
	F_4	−0.045	−0.045	−0.045	−0.045
	F_5	−0.067	−0.067	−0.067	−0.067
	F_6	−0.075	−0.075	−0.075	−0.075
	F_7	−0.052	−0.052	−0.052	−0.052
	F_8	−0.058	−0.058	−0.058	−0.058
	F_9	−0.053	−0.053	−0.053	−0.053
c-phase chaos eye feature value	F_1	−0.068	−0.068	−0.068	−0.068
	F_2	−0.075	−0.075	−0.075	−0.075
	F_3	−0.08	−0.08	−0.08	−0.08
	F_4	−0.069	−0.069	−0.069	−0.069
	F_5	−0.049	−0.049	−0.049	−0.049
	F_6	−0.046	−0.046	−0.046	−0.046
	F_7	−0.052	−0.052	−0.052	−0.052
	F_8	−0.052	−0.052	−0.052	−0.052
	F_9	−0.058	−0.058	−0.058	−0.058

Table 3. Fault detection results under the failure of different switches in *a*-phase (inverter frequency = 60 Hz).

Fault Category	Output Weight Value			Detection Result
	F_1	F_2	F_3	
F_1	**0.782085**	−0.564565	−0.591532	F_1
F_2	−0.544865	**0.861617**	−0.629411	F_2
F_3	−0.037735	−0.378546	**0.553326**	F_3

Table 4. Fault detection results under the failure of different switches in *b*-phase (inverter frequency = 60 Hz).

Fault Category	Output Weight Value			Detection Result
	F_4	F_5	F_6	
F_4	**0.780133**	−0.549192	−0.594745	F_4
F_5	−0.572378	**0.872429**	−0.648071	F_5
F_6	−0.225007	−0.346686	**0.701689**	F_6

Table 5. Fault detection results under the failure of different switches in *c*-phase (inverter frequency = 60 Hz).

Fault Category	Output Weight Value			Detection Result
	F_7	F_8	F_9	
F_7	**0.813761**	−0.569932	−0.600617	F_7
F_8	−0.549737	**0.884781**	−0.62921	F_8
F_9	−0.253144	−0.351958	**0.521521**	F_9

Table 6. Fault detection results under the failure of different switches in *a*-phase and addition of ±5% erroneous data (inverter frequency = 60 Hz).

Fault Category	Error Percentage	Output Weight Value			Detection Result
		F_1	F_2	F_3	
F_1	5%	**0.227338**	−0.577322	−0.589176	F_1
F_1	−5%	**0.563368**	−0.512827	−0.593788	F_1
F_2	5%	−0.554998	**0.442223**	−0.617735	F_2
F_2	−5%	−0.514244	**0.598609**	−0.653885	F_2
F_3	5%	0.0491609	−0.39636	**0.37029**	F_3
F_3	−5%	−0.124961	−0.361071	**0.709824**	F_3

Table 7. Fault detection results under the failure of different switches fail in *b*-phase and addition of ±5% erroneous data (inverter frequency = 60 Hz).

Fault Category	Error Percentage	Output Weight Value			Detection Result
		F_4	F_5	F_6	
F_4	5%	**0.225285**	−0.581416	−0.59255	F_4
F_4	−5%	**0.565218**	−0.498222	−0.59684	F_4
F_5	5%	−0.555554	**0.510485**	−0.629454	F_5
F_5	−5%	−0.542088	**0.536848**	−0.665188	F_5
F_6	5%	−0.147346	−0.362908	**0.727323**	F_6
F_6	−5%	−0.30369	−0.331795	**0.639154**	F_6

Table 8. Fault detection results under the failure of different switches in *c*-phase and addition of ±5% erroneous data (inverter frequency = 60 Hz).

Fault Category	Error Percentage	Output Weight Value			Detection Result
		F_7	F_8	F_9	
F_7	5%	**0.281603**	−0.581739	−0.598714	F_7
F_7	−5%	**0.51428**	−0.517926	−0.602419	F_7
F_8	5%	−0.551061	**0.455688**	−0.617525	F_8
F_8	−5%	−0.522304	**0.586427**	−0.654039	F_8
F_9	5%	−0.17552	−0.367097	**0.50828**	F_9
F_9	−5%	−0.330461	−0.336816	**0.514661**	F_9

4. Fault-Tolerant Control of Three-Level T-Type Inverter

Most applications have particularly high requirements for equipment reliability. Accordingly, the reliability of inverter systems can be improved by equipping such systems with fault-tolerant control mechanisms that can enable them to maintain a stable output voltage. Figure 9 presents the architecture of the three-level T-type inverter proposed in this study. Compared with conventional three-level T-type inverters, the proposed inverter includes two additional insulated gate bipolar transistors and 3 three-pole ac semiconductor switches (Triode AC, TRIAC). The spare leg comprises the insulated gate bipolar transistors (IGBT) $S_x{}^+$ and $S_x{}^-$, which can be used to replace those in the faulty phase to maintain circuit operation. The 3 three-pole ac semiconductor switches T_a, T_b, and T_c connect the spare legs and *a*-, *b*-, and *c*-legs. When a fault occurs, the spare leg is connected with the faulty leg so that the spare leg can replace the function of the faulty leg, thus achieving fault tolerance.

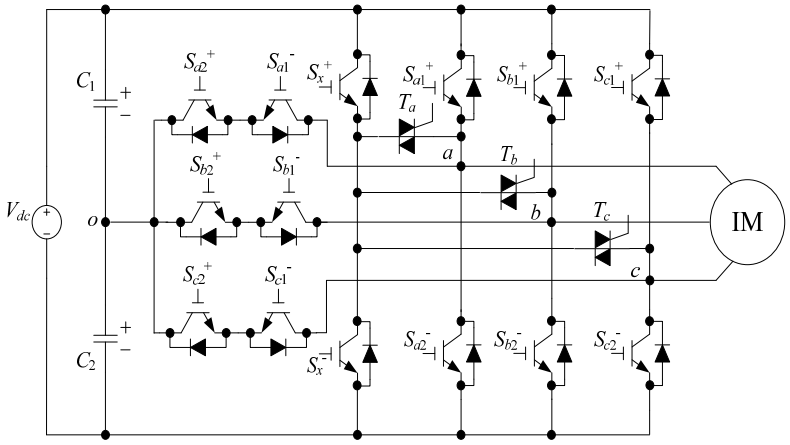


Figure 9. The architecture of proposed three-level T-type inverter.

4.1. Fault-Tolerant Control Analysis

The proposed fault-tolerant control system deactivates the *a*-phase half-bridge switches ($S_{a1}{}^+$ and $S_{a2}{}^-$) when an open-circuit fault occurs in $S_{a1}{}^+$ or $S_{a2}{}^-$. The *b*-phase, *c*-phase, and neutral-point switches still operate normally, and switch T_a in the three three-pole ac semiconductor switches are activated to replace the faulty *a*-phase leg with the spare leg. The spare leg adopts the switching mode of the original *a*-phase leg to maintain the three-phase balanced output voltage. If an open-circuit fault occurs in $S_{b1}{}^+$ or $S_{b2}{}^-$, the *b*-phase half-bridge switches ($S_{b1}{}^+$ and $S_{b2}{}^-$) are deactivated. The *a*-phase, *c*-phase, and neutral-point switches still operate normally, and switch T_b in the three three-pole ac semiconductor switches are activated to replace the faulty *b*-phase leg with the spare leg. The spare leg adopts the switching mode of the original *b*-phase leg to maintain the three-phase balanced output voltage. Similarly, if an open-circuit fault occurs in $S_{c1}{}^+$ or $S_{c2}{}^-$, the *c*-phase half-bridge switches ($S_{c1}{}^+$ and $S_{c2}{}^-$) are deactivated. The *a*-phase, *b*-phase, and neutral-point switches still operate normally, and

switch T_c of the three three-pole ac semiconductor switches are activated to replace the faulty *c*-phase leg with the spare leg. The spare leg adopts the switching mode of the original *c*-phase leg to maintain the three-phase balanced output voltage. Consider, for example, the occurrence of an open-circuit fault in $S_{a1}{}^{+}$, $S_{b2}{}^{-}$, and $S_{c1}{}^{+}$; the corresponding switching states induced by the fault-tolerant control system for the three-level inverter are shown in Figures 10–12, respectively.

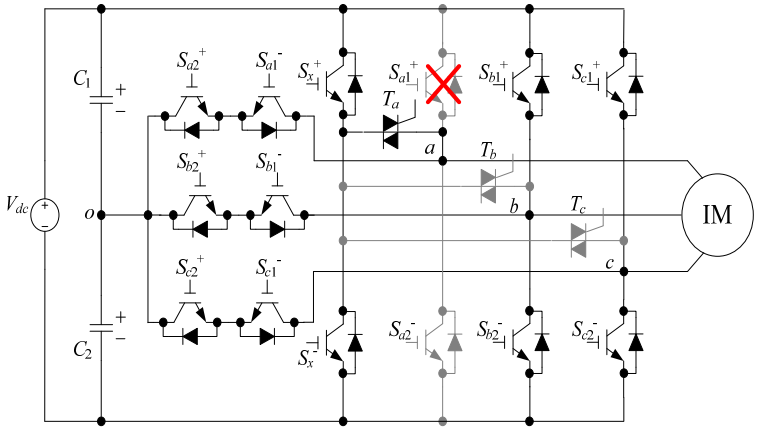


Figure 10. Tolerant control state when an open-circuit fault occurs in inverter switch $S_{a1}{}^{+}$.

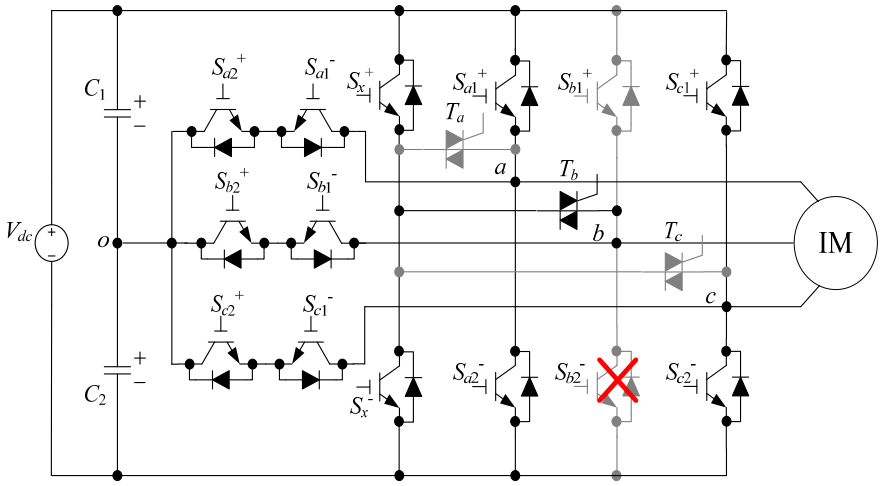


Figure 11. Tolerant control state when an open-circuit fault occurs in inverter switch $S_{b2}{}^{-}$.

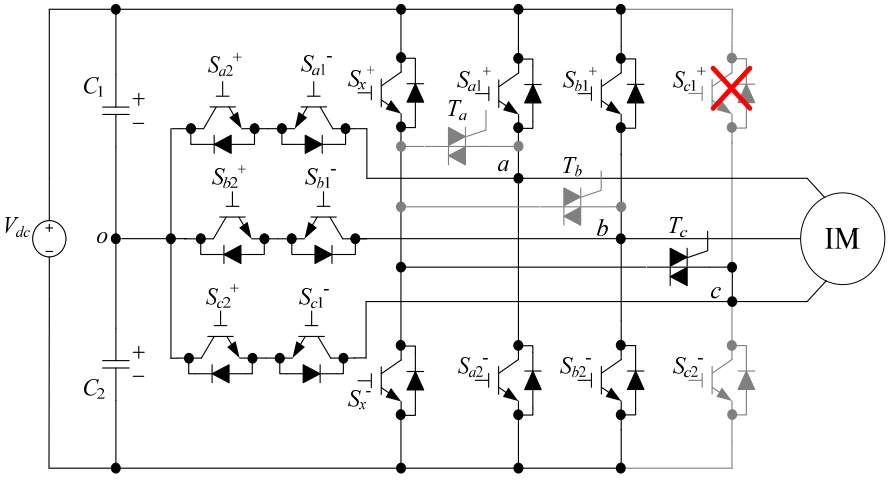


Figure 12. Fault-tolerant control state for an open-circuit fault occurring in $S_{c1}{}^{+}$.

4.2. Fault-Tolerant Control Simulation

This study conducted a simulation of fault-tolerant control by using PSIM software. In the simulation, an open-circuit fault was considered to occur in $S_{a1}{}^{+}$, $S_{b2}{}^{-}$, and $S_{c1}{}^{+}$. The simulation results revealed changes in the output line voltage under three conditions, namely conditions of normal inverter operation, faulty switch operation, and fault-tolerant control execution. As shown in Figure 13, at 0.06 s, an open-circuit fault occurred in switch $S_{a1}{}^{+}$ and distorted the three-phase output line voltage. The fault-tolerant control system was launched at 0.12 s. The *a*-phase half-bridge switches ($S_{a1}{}^{+}$ and $S_{a2}{}^{-}$) were deactivated, but the *b*-phase, *c*-phase, and neutral-point switches still operated normally. Switch T_a in the 3 three-pole ac semiconductor switches was activated to replace the faulty *a*-phase leg with the spare leg, and the spare leg adopted the switching mode of the original *a*-phase leg to maintain a balanced three-phase output voltage. As shown in Figure 13, after the execution of the fault-tolerant control system, the three-phase output line voltage remained to be five levels. Accordingly, after the occurrence of the fault, the balanced three-phase output line voltage remained unchanged, and the quality of the output voltage was not reduced.

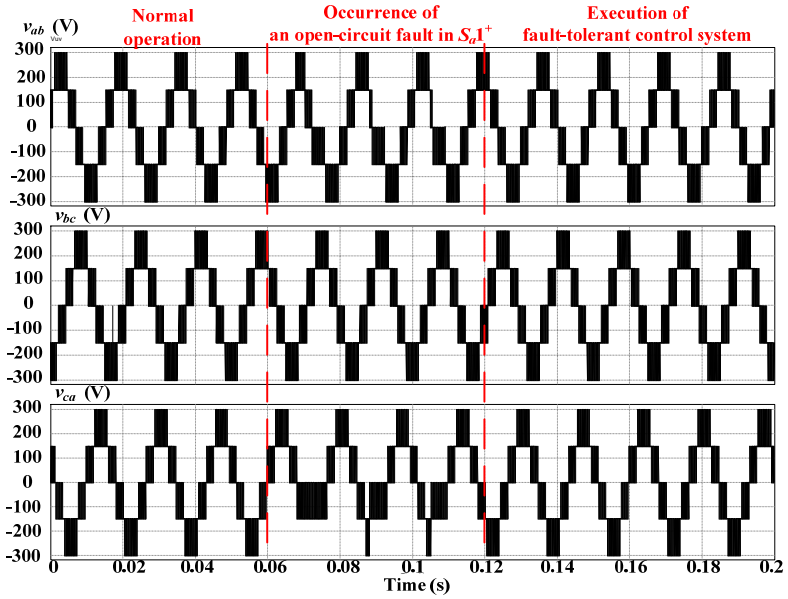


Figure 13. The output voltage of $S_{a1}{}^{+}$ after the occurrence of an open-circuit fault and the activation of fault-tolerant control.

As presented in Figure 14, at 0.06 s, an open-circuit fault occurred in switch $S_{b2}{}^{-}$ and distorted the three-phase output line voltage. The fault-tolerant control system was launched at 0.12 s. The *b*-phase half-bridge switches ($S_{b1}{}^{+}$ and $S_{b2}{}^{-}$) were deactivated, but the *a*-phase, *c*-phase, and neutral-point switches still operated normally. Switch T_b of the 3 three-pole ac semiconductor switches was activated to replace the faulty *b*-phase leg with the spare leg, and the spare leg adopted the switching mode of the original *b*-phase leg to maintain a balanced three-phase output voltage. After the launching of the fault-tolerant control system, the three-phase output line voltage remained to be five levels. Hence, after the occurrence of the fault, the balanced three-phase output line voltage remained unchanged, and the quality of the output voltage was not reduced.

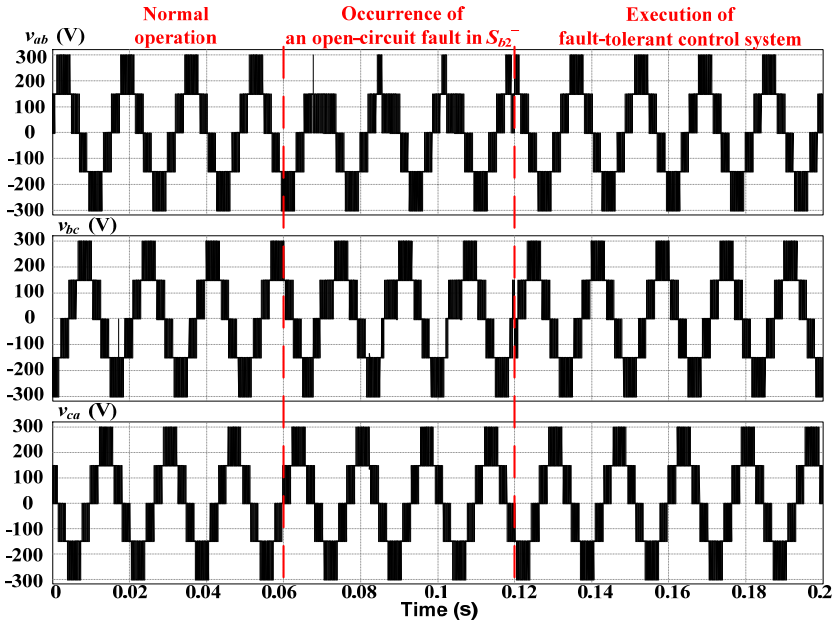


Figure 14. The output voltage of $S_{b2}{}^-$ after the occurrence of an open-circuit fault and the activation of fault-tolerant control.

As illustrated in Figure 15, at 0.06 s, an open-circuit fault occurred in switch $S_{c1}{}^+$ and distorted the three-phase output line voltage. The tolerant control system was launched at 0.12 s. The *c*-phase half-bridge switches ($S_{c1}{}^+$ and $S_{c2}{}^-$) were deactivated, but the *a*-phase, *b*-phase, and neutral-point switches still operated normally. Switch T_c of the 3 three-pole ac semiconductor switches was activated to replace the faulty *c*-phase leg with the spare leg, and the spare leg adopted the switching mode of the original *c*-phase leg to maintain the balanced three-phase output voltage. After the launching of the fault-tolerant control system, the three-phase output line voltage remained to be five levels. Accordingly, after the occurrence of the fault, the balanced three-phase output line voltage remained unchanged, and the quality of the output voltage was not reduced.

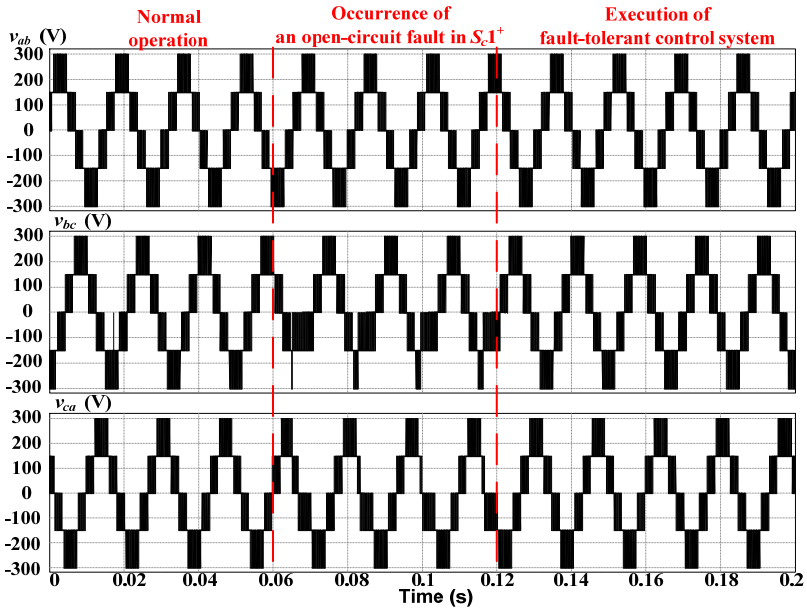


Figure 15. The output voltage of $S_{c1}{}^+$ after the occurrence of an open-circuit fault and the activation of fault-tolerant control.

As shown in Figure 13, at 0.06 s, an open-circuit fault occurred in switch S_{a1}^{+} and distorted the output line voltage v_{ab} and $v_{ca.}$ The fault-tolerant control system was launched at 0.12 s. As shown in Figure 13, after the execution of the fault-tolerant control system, the three-phase output line voltage waveforms remained to be five levels. Accordingly, after the occurrence of the fault, the balanced three-phase output line voltage remained unchanged, and the quality of the output voltage was not reduced. The same results are obtained by using the proposed fault-tolerant control system for an open-circuit fault occurred in switch S_{b2}^{-} and S_{c1}^{+}. As shown in Figures 14 and 15, when the occurrence of the fault, by using the proposed fault-tolerant control system, the balanced three-phase output line voltage still remained unchanged, and the quality of the output voltage was not reduced.

The fault-tolerant control system can replace the faulty leg of any switch with a spare leg. Thus, after the occurrence of a fault, the three-phase output voltage is unaffected and a loading reduction is not required. The operating mode of the fault-tolerant control system is simple. Therefore, if a fault occurs, apart from changing the switching state of the switches, it is not necessary to adjust the phase angle of the reference voltage signal in a pulse width modulation (PWM) mechanism to maintain a balanced three-phase system. The proposed fault-tolerant control system can prevent economic losses and even casualties caused by faults and can substantially increase system utilization rates and expand system applications. In order to make the process of the proposed fault-tolerant control clearer, use the flow chart, shown in Figure 16, to explain.

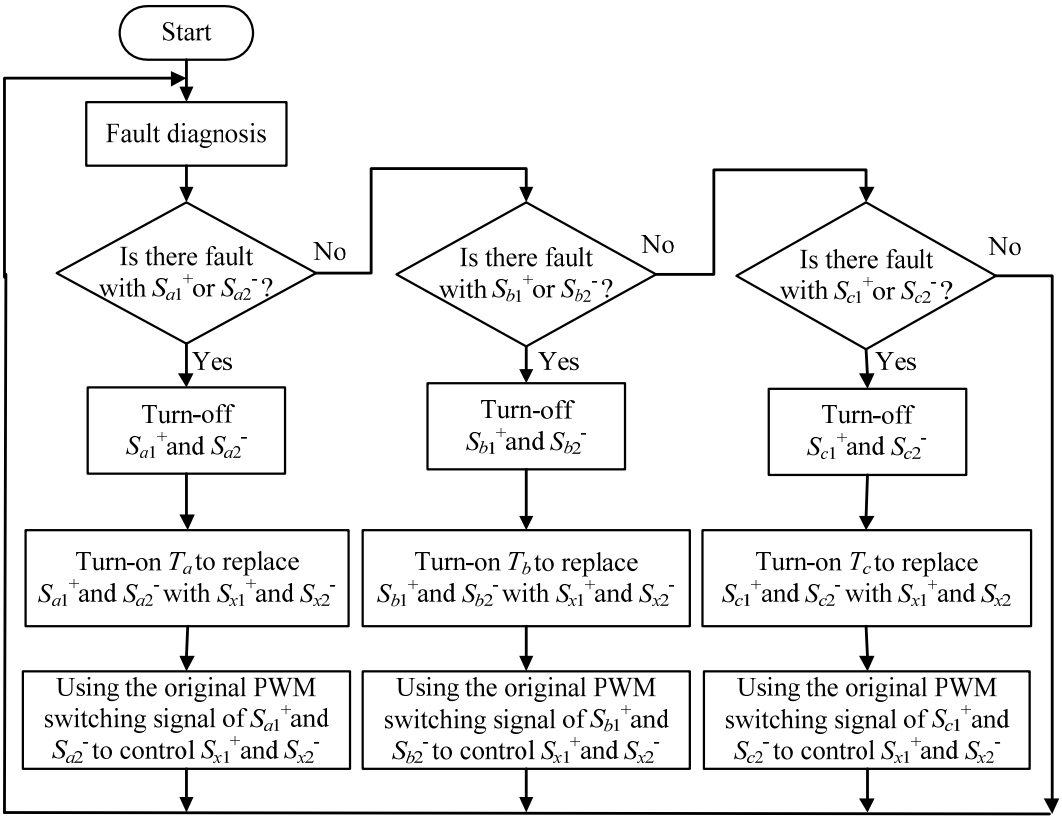


Figure 16. The flow chart of the proposed fault-tolerant control system in case of any power switch fault.

5. Conclusions

This study proposes a fault-tolerant diagnosis system based on chaos theory and extension theory for locating a faulty power transistor in a three-level T-type inverter. The proposed system not only obviates the necessity of learning but also has the capability of generating fault tolerance. Therefore, it can reduce the influence of interference signals. In addition, the proposed system can perform control procedures immediately after any inverter switch fails, thus providing continuous power supply to

and improving the power supply reliability of the three-level T-type inverter. The test results showed that the proposed fault diagnosis method can detect open-circuit faults in 12 power transistor switches by using only low-cost voltage sensors, and the final accuracy rate is 100%, demonstrating that the proposed fault diagnosis method has a good effect on three-level T-type inverters. The results also indicated that after the consideration of errors, the proposed fault diagnosis system could still correctly detect the fault category. Therefore, regardless of whether accurate or erroneous test data are used, the proposed system can correctly detect the fault category. After the failure of any switch, the proposed fault-tolerant control system can still control the output line voltage and maintain the three-phase balance; this thus verifies the feasibility of the proposed system. Therefore, the proposed fault-tolerant control system can prevent economic losses and even casualties caused by faults and can substantially increase system utilization rates and expand system applications.

Author Contributions: The conceptualization was proposed by K.-H.C., who also was responsible for writing-review and editing this paper. L.-Y.C. completed the formal analysis of the fault detection based on chaos theory and extension theory. F.-Q.X. carried out the data curation, software program and experimental validation. K.-H.C. completed the formal analysis of tolerant control and was in charge of project administration.

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Conflicts of Interest: The authors of the manuscript declare that there is no conflict of interest with any of the commercial identities mentioned in the manuscript.

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