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Improved Operation of the Step-Up Converter with Large Voltage Gain and Low Voltage on Capacitors

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Abstract: This work proposes an improvement for a recently proposed converter. The discussed converter is the so-called low-voltage in capacitors (LVC). It offers a larger voltage gain compared to the standard step-up or boost converter while operating with a relatively low voltage in their capacitors (lower than the voltage at the output port). The improvement consists of a modification in the pulse width modulation (PWM) scheme. The new modulation scheme allows for a reduction in the voltage ripple at the output port, which means an improvement in the power quality. The LVC converter contains two transistors, but it was proposed to operate with a single switching signal. The new PWM scheme is based on two switching signals with the same duty cycle (same waveform and same average time in high) but 180° of phase shift among them. The PWM scheme significantly affects the voltage ripple at the converter's output port. The voltage ripple reduction at the converter's output port is achieved without increasing the transistor switching frequency and without modifying the circuit parameters (capacitance in capacitors or inductance in inductors). The article starts by introducing the converter. Then, it presents its mathematical model, including the calculation of the voltage ripple at its output port. The experimental results performed on the LCV in both the former and the proposed operation prove the reduction in the voltage ripple, and the comparison also includes the traditional boost converter.

Keywords: step-up converter; low voltage in capacitors converter; PWM power conversion

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1. Introduction

Power electronics is the field related to the electrical energy conversion through electronic converters; the power conversion can be from alternating current (ac) to direct current (dc), from dc to ac, from ac to ac, or dc–dc. An example of a dc-to-dc (or just dc–dc) converter can be voltage regulators in mobile electronics devices, i.e., a device may be powered by a batterie, but its voltage is not constant (it decreases while discharging with time), and a power converter or regulator is fed with this decreasing voltage and used to provide a constant output voltage to feed other electronic circuits, whilst it keeps the power in electronics circuits at an adequate level [1–3].

It may be worth mentioning that the power converter cannot increase the amount of energy. This is because they usually regulate the voltage in an interchange of current; for example, receiving 4 V with 0.5 A can change it to 1 V with 2 A, approximately keeping the power constant. In practice, there are power losses inside the power converter, and the input power is slightly higher than the output power [2–4].

Another example of power conversion is the conversion of energy from renewable sources into feed appliances or to grid-tie converters which can push the generated power into the utility grid.

Some renewable energy sources, such as photovoltaic (PV) panels and fuel cell (FC) stacks, generate a dc voltage whose amplitude may change due to external conditions, however, the generated voltage is usually lower, and alternative current (ac) is also usually

required to feed the domestic appliances or push the power into the utility grid. Those renewable energy sources are important, but their output voltage (usually in the range of tens of volts) may be excessively low for feed inverters (dc–ac converters) to feed electric appliances. For example, a dc–dc converter may be used to step up the voltage from PV panes and FC stacks to feed the traditional H-bridge inverter, producing an ac voltage that can feed electric appliances.

This article focuses on the dc–dc power conversion, which means changing the amplitude of a dc voltage in an interchange of the current. There are well-known traditional converters, such as the standard boost converter depicted in Figure 1 [4]. It is made of one inductor, one capacitor, and two switches; one of the switches must be a transistor, and the other may be a transistor or a diode (depending on the power flow or synchronous rectification requirements). The boost converter can increase the voltage level from the input to output. The ratio of the voltage at the output port divided by the voltage at the input port is called voltage gain. Evidently, in the boost converter, the voltage gain is larger than the unity. However, as the voltage gain becomes larger or the duty cycle (or duty ratio) approaches one, the efficiency of the converter decreases [4,5]. As a result, practical converters using the boost topology usually increase the input voltage up to four to five times (or a duty ratio of 0.8) [5].

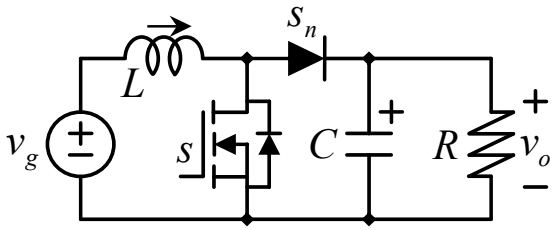

Figure 1. The standard step-up or boost topology.

The power electronics industry is seeking to create high-gain converters for scenarios where the voltage gain is excessively high for a standard boost converter, such as generating electricity from renewable energy sources.

There are various ways to attain a high voltage gain, including using magnetic coupling in either transformer-based converters or coupled-inductor-based converters [6–9]. These are plausible solutions, but in applications where electrical isolation is not required, it may be preferable to avoid magnetic coupling elements since transformers and coupled inductors may be expensive, and it may not be easy to find the appropriate element (with the desired parameters) off-the-shelves. Furthermore, transformer-based topologies are relatively complex compared with transformer-less topologies. On the other hand, transformer-less converters are usually manufactured with what we call "components off-the-shelves". This means that they are commercially available (most of the time, transformers must be designed and manufactured for a particular application).

Other methods for achieving high voltage gain in the literature include charge pump topologies, which are converters made by semiconductors and capacitors (without inductors) which can attain a large voltage gain with a lightweight [10,11]. There are also hybrid topologies of multiplier converters. In other words, dc–dc converters made by the combination of a traditional converter and charge pumps, also called voltage multiplier converters [12–15], are a kind of circuit that might use a traditional converter with a diode capacitor voltage multiplier to increase their voltage gain. Another solution is the use of quadratic converters [14–17], converters whose voltage gain is a quadratic function of their duty cycle (the terms duty ratio or duty cycle and voltage gain will be further explained).

These are the reason why the development of non-isolated large voltage-gain dc–dc converters is a very active research field. One of the recent contributions in the field of high-voltage gain converters was the proposition of the low-voltage in capacitors (LVC) converter. Initially introduced in [18], it is a converter whose main advantage over other high voltage-gain converters is that their capacitors sustain a low voltage compared to

the output voltage. On the other hand, the traditional boost converter and other similar converters require at least one capacitor to sustain the output voltage, which is the largest voltage in a step-up converter. Moreover, the output capacitor usually stores a high amount of energy since the stored energy in a capacitor is proportional to the square of its voltage. Therefore, it would be desirable to develop boost converters in which capacitors block a voltage lower than the output voltage, which is the advantage of the LVC converter [18].

The LVC converter has two capacitors in series with the input power source to provide the output port, which reduces its voltage rating. The converter was introduced in [18] with the traditional single switching-function pulse width modulation (PWM) scheme.

The study in [18] presented the LVC converter as an advancement over another high-gain converter [19]. It also compared the LVC with two similar converters and found that it used less stored energy in capacitors while still meeting the output voltage ripple requirements. Reducing the stored energy in capacitors is desirable as the capacitor size is proportional to the energy they store [20–22].

This work explores a different operation of the LVC converter with a different PWM scheme, which consists of two switching signals (instead of one) shifted in phase 180°. The PWM scheme affects the voltage ripple at the converter's output port. The results presented in this article demonstrate that the LVC converter operating with the proposed scheme has a reduced voltage ripple at its output port (compared with the previous operation), while using the same capacitance in capacitors and other parameters (inductance in inductors, switching frequency, etc.). This article briefly introduces the LVC converter first on the former operation. Then, the converter dynamic mathematical model is presented, including calculating the voltage ripple at the converter output port in the proposed and previous operations. Finally, the proposal is verified through experimental results.

2. The LVC Converter in Their Traditional Operation

This section describes the converter under study, also called the low-voltage capacitor (LVC) converter, which in this operation, we call the "traditional operation", as introduced in [18]. The topology comprises two capacitors (C_1, C_2), two inductors (L_1, L_2), and four semiconductor devices. Semiconductor devices in switched mode power supplies are used as open or closed devices (not in their linear mode); in this case, they are two transistors (s_a, s_b) and two diodes (s_{an}, s_{bn}). The converter schematic is depicted in Figure 2.

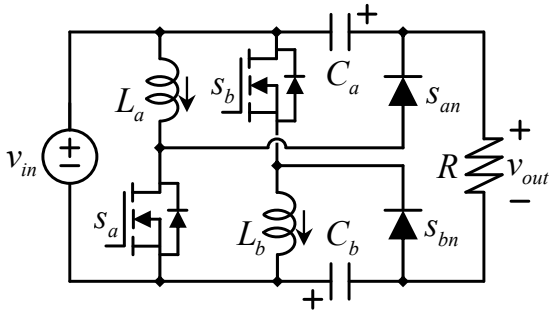

Figure 2. LVC converter topology schematic.

The converter has two capacitors that sustain a voltage smaller than the output voltage. This is their main advantage, as introduced in [18], in contrast to other converters in which at least one capacitor sustains the output voltage. The voltage output is the sum of the voltage from the capacitors and the input voltage, as seen in Figure 2.

$$v_{out} = v_{in} + v_{Ca} + v_{Cb} \tag{1}$$

Figure 3 shows the same LVC converter with a different way of drawing the schematic. In this case, the draw is on the way of double dual topology. Therefore, the fact that the output voltage is equal to the combination of the capacitor's voltage and the input voltage is more evident in this figure.

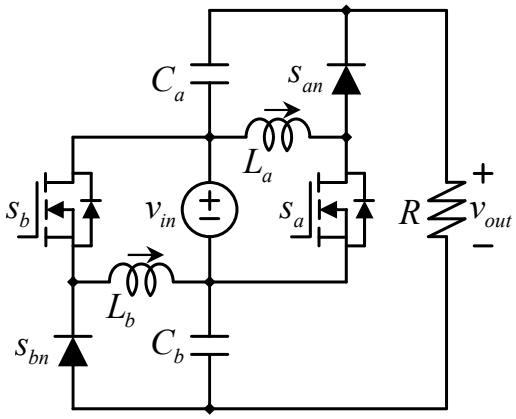

Figure 3. LVC converter topology schematic drawn in a vertical manner.

The traditional operation considers both transistors to have the same switching function, which means both transistors open and close at the same time; this leads to an operation with two equivalent circuits or switching states (in the continuous conduction mode (CCM)); those switching states are shown in Figure 4.

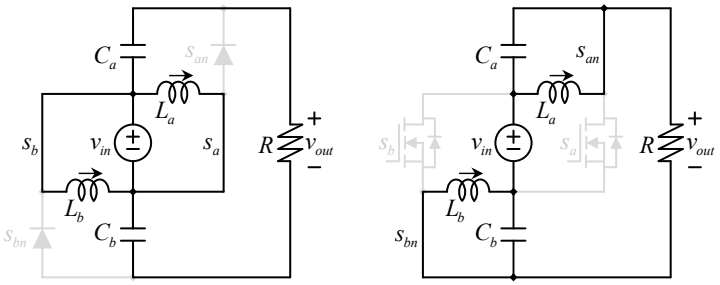

Figure 4. Equivalent circuits or switching states of the LVC converter in the traditional operation: (**a**) Transistors on; and (**b**) transistors off.

2.1. Mathematical Model in the Traditional Operation

The converter's mathematical model in the traditional operation was introduced in [18]. It was obtained through the averaging technique with the circuits in Figures 3 and 4 [4,18]. The averaging technique is a method used to simplify complex circuits by reducing them to their average behavior over a certain time period. This is achieved by considering the circuit's average values for current and voltage instead of their individual variations and then representing it with a simplified equivalent circuit. The dynamical model presented in [18] is (2)–(5).

$$L_a \frac{di_{La}}{dt} = dv_{in} - (1-d)v_{Ca} \tag{2}$$

$$L_b \frac{di_{Lb}}{dt} = dv_{in} - (1-d)v_{Cb} \tag{3}$$

$$C_a \frac{dv_{Ca}}{dt} = (1-d)i_{La} - i_{out} \tag{4}$$

$$C_b \frac{dv_{Cb}}{dt} = (1-d)i_{Lb} - i_{out} \tag{5}$$

where the output current i_{out} can be calculated in terms of the output voltage (1) and the load resistance R as (6).

$$i_{out} = \frac{v_{out}}{R} \tag{6}$$

The model which was previously introduced in [18] is a fourth-order nonlinear model. From the dynamic model, the equilibrium operation or steady state can be obtained. In order to do so, we must consider the small ripple approximation [4].

By taking into account that the state variables in Equations (2)–(5) are at equilibrium, where their derivatives (with respect to the time) are equal to zero, we can determine the voltage across the capacitors and the current through the inductors in a steady state, resulting in (7)–(10)

$$V_{Ca} = \frac{D}{1-D} V_{in} \tag{7}$$

$$V_{Cb} = \frac{D}{1-D} V_{in} \tag{8}$$

$$I_{Lb} = \frac{1}{(1-D)} \frac{V_{out}}{R} \tag{9}$$

$$I_{La} = \frac{1}{(1-D)} \frac{V_{out}}{R} \tag{10}$$

The output voltage V_{out}, can be expressed from (1), (7), and (8), as (11).

$$V_{out} = V_{in} \frac{1+D}{1-D} \tag{11}$$

The converter has a voltage gain larger than the traditional boost converter (for the same duty cycle), which is an advantage, as described in [18]. However, their main advantage can be corroborated by (7) and (8), as the voltage across the capacitors is lower than the output voltage (11), making it an additional advantage over other state-of-the-art converters.

The energy stored in the capacitors can be expressed using Equation (12).

$$E_C = \frac{C V_C^2}{2} \tag{12}$$

Since the capacitor's stored energy is a function of its voltage squared, a relatively small reduction in the voltage results in a significant reduction in the stored energy, which is an advantage since the volume of the capacitor is proportional to its stored energy [14–16].

The selection of inductors and capacitors is performed with the traditional method based on the voltage ripple for capacitors and current ripple for inductors [4], as introduced in [18]; this can be summarized as (13)–(16).

$$L_a = \frac{V_{in}}{2\Delta i_{La}} D T_S \tag{13}$$

$$L_b = \frac{V_{in}}{2\Delta i_{Lb}} D T_S \tag{14}$$

$$C_a = \frac{I_{out}}{2\Delta v_{Ca}} (1-D) T_S \tag{15}$$

$$C_b = \frac{I_{out}}{2\Delta v_{Cb}} (1-D) T_S \tag{16}$$

Reference [18] also describes the selection of semiconductors and the real gain of the converter considering losses. The traditional method also considers both inductors as equal $L_a = L_b$ and both capacitors as also equal $C_a = C_b$.

2.2. Voltage Ripple at the Output Port in the Traditional Operation

The voltage ripple at the output port is the main variable of the present work since the objective of the proposed operation is to maintain the converter operating as in the traditional mode with the advantage of reducing the output voltage ripple. The ideal

output voltage is a constant (pure DC) signal, but in duty cycles different from 0.5, a small ripple is present due to the switching action. The ripple may be reduced by increasing the capacitance of capacitors or the switching frequency, but the aim of this work is to maintain the capacitance of capacitors as equal to the traditional operation (and also with the switching frequency of transistors) and reduce the output voltage ripple with capacitors of the same size.

The selection of capacitors (15) and (16) involves the capacitors' voltage ripples Δv_{ca} and Δv_{cb}. From Equations (15) and (16), the voltage ripple in the capacitors can be expressed using Equations (17) and (18).

$$\Delta v_{Ca} = \frac{I_{out}}{2C_a}(1-D)T_S \tag{17}$$

$$\Delta v_{Cb} = \frac{I_{out}}{2C_b}(1-D)T_S \tag{18}$$

The voltage ripple at the output port results in the simultaneous charging and discharging of the capacitors. If the capacitors are assumed to have equal capacitance, $C_a = C$, and $C_b = C$, then the voltage ripple at the output port can be calculated by adding (17) and (18), leading to Equation (19). Let us recall that this expression is valid for the former operation and considering capacitors of equal capacitance.

$$\Delta v_{out} = \frac{I_{out}}{C}(1-D)T_S \tag{19}$$

We will compare this expression against their value in the proposed operation.

3. The Proposed Operation of the LVC Converter

In the former operation, transistors switch synchronously; they close and open at the same time, which means that they have the same switching function and the same duty cycle. The duty cycle d (or D in steady state) is defined as the time in which a transistor remains closed multiplied by the switching frequency f_S (or divided over the switching period T_S). The switching period (inverse of the switching frequency) can be divided into two different times: the time a transistor remains closed (DT_S), and the time a transistor remains open $(1-D)T_S$. The proposed operation does not intend to change the converter's duty cycle but to have the same duty cycle of transistors with a different switching function.

The proposed change consists of using two switching signals (instead of one) based on the two-phase interleaved PWM, similar to that used in the interleaved buck or boost. Both switching signals with equal duty ratios are shifted in phase by 180°; the phase shift is produced with two carrier signals (triangular) which shifted 180°. We can call s_a and s_b to the two switching signals and s_{atri} and s_{btri} to the triangular carriers. This PWM scheme can be generated with two comparators, as shown in Figure 5. The triangular carrier signals have an amplitude of one. This produces the duty cycle that can be represented with a dc signal of the same magnitude as the intended duty ratio.

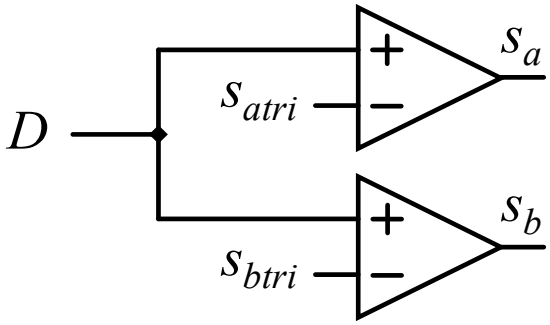

Figure 5. Two switching signals' PWM generator with two ideal comparators.

The former operation, based on a single switching signal, has two equivalent circuits (as can be seen in Figure 3). In the proposed operation, since transistors have a different switching function, all four combinations of two digital signals may be present, which means that the set $\{s_a, s_b\}$ may take values of {0, 0}, {0, 1}, {1, 0}, or {1, 1}. Figure 6 shows the equivalent circuits of the converters according to this set of possible values for the switching functions.

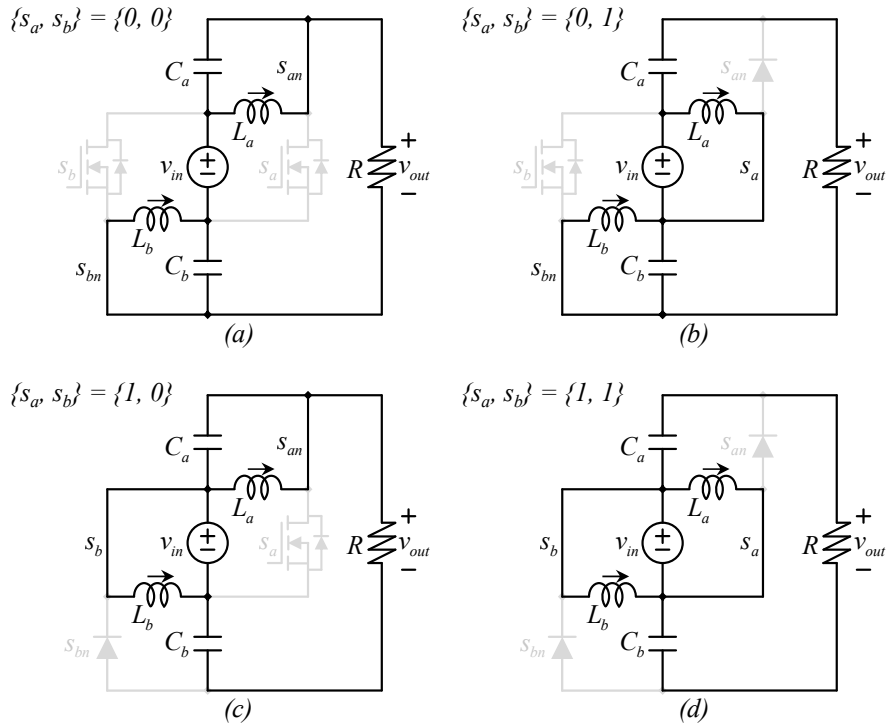

Figure 6. Switching states of the converter with two switching signals (**a**) $\{s_a, s_b\}$ = {0, 0}; (**b**) $\{s_a, s_b\}$ = {0, 1}; (**c**) $\{s_a, s_b\}$ = {1, 0}; and (**d**) $\{s_a, s_b\}$ = {1, 1}.

The number of equivalent circuits increases from two to four. Nonetheless, during the operation, the number of equivalent circuits increases from two to three, and in the particular case in which $D = 0.5$, the converter only has two equivalent circuits. We can expect that the duty ratio may change due to disturbances on either the input voltage or the output current since the duty ratio is used to compensate for those perturbations.

We can classify the operation in three situations, namely the instance in which the duty cycle is larger than 0.5 ($D > 0.5$), the instance in which $D < 0.5$, and the particular instance in which the duty cycle is exactly 0.5. The waveforms related to the two switching signals' PWM are shown in Figure 7. Those signals are generated with the logic of Figure 3.

Figure 7a shows the PWM generator in which the duty cycle is $D = 0.4$, and Figure 7d shows the corresponding waveforms of the operation in Figure 7a. The switching signal s_a and the triangular carrier signal s_{atri} are black in color while that corresponding to s_b is in dark gray. We can see that this example corresponds to the situation in which $D < 0.5$, and in this situation, sometimes $s_a = 1$ while $s_b = 0$, and other times we have the opposite situation, $s_a = 0$ while $s_b = 1$, and may also have both signals as low ($s_a = 1$ while $s_b = 0$), which resembles a dead-time in the firing signals. In this operating condition, the simultaneous switching of signals does not coincide at any time.

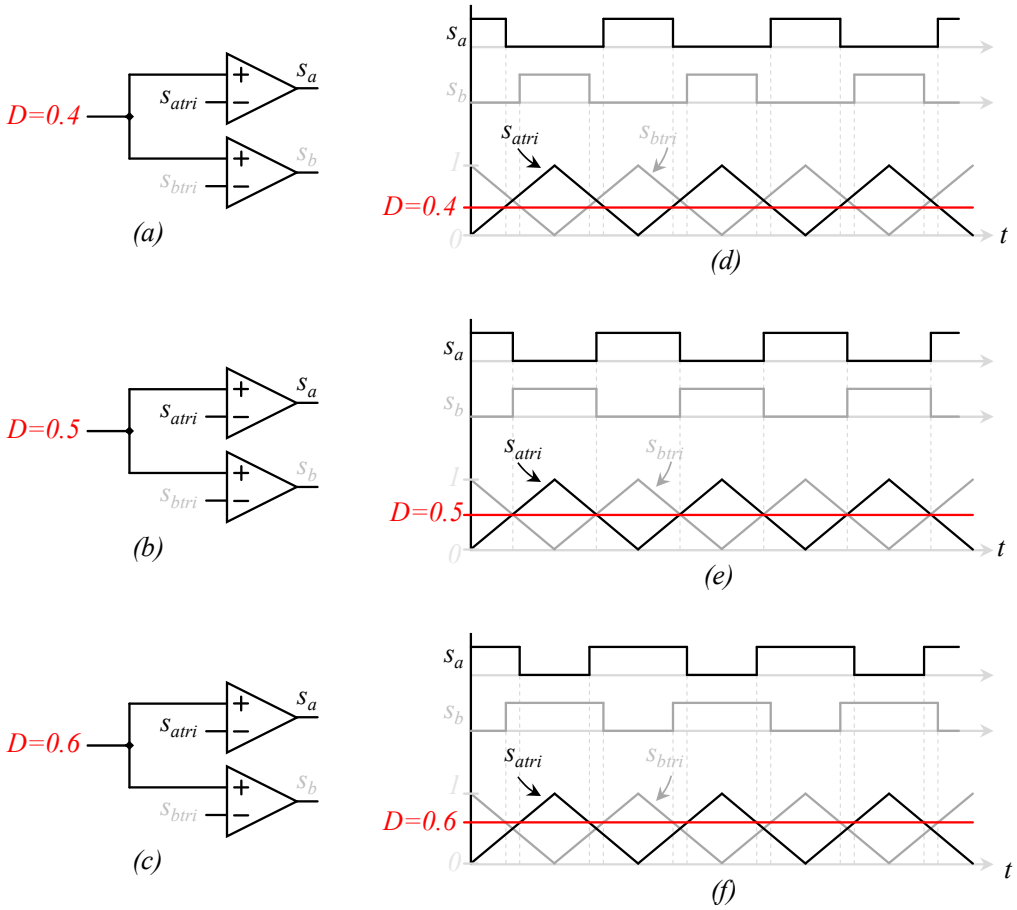

Figure 7. PWM generator with different duty cycles: (**a**) $D = 0.4$; (**b**) $D = 0.5$; (**c**) $D = 0.6$, and important waveforms of the PWM generator with the aforementioned duty cycles (**d**) $D = 0.4$; (**e**) $D = 0.5$; and (**f**) $D = 0.6$.

Figure 7b shows the PWM generator in which the duty cycle is $D = 0.5$, whilst the corresponding waveforms of this operation points are shown in Figure 7e. We can see that this example corresponds to the particular situation in which the duty cycle is exactly 0.5, and in this situation, sometimes $s_a = 1$ while $s_b = 0$, and other times we have the opposite situation, $s_a = 0$ while $s_b = 1$. In this operating condition, the simultaneous switching of signals does not coincide at any time.

Figure 7c shows the PWM generator in which the duty cycle is $D = 0.6$, whilst the corresponding waveforms of this operation point are shown in Figure 7f. This example corresponds to the situation in which $D > 0.5$, and in this situation, sometimes $s_a = 1$ while $s_b = 0$, and other times we have the opposite situation, $s_a = 0$ while $s_b = 1$, and may have both signals as high ($s_a = 1$ while $s_b = 1$), which resembles overlapping in the firing signals. We can also see that both firing signals (s_a and s_b) are not low at the same time (at any time).

Despite the combinations of firing signals, the interleaved PWM does not change the duty cycle, and as we can see from Figure 6, as the voltage in the inductors only depends on their transistor's state. Similarly, the current through the capacitors only depends on their respective transistors' states. This means that the previously derived mathematical model still represents the converter behavior, which is at least the dynamic and the steady state value of the state equations, but there is a difference, which is the output voltage ripple calculation.

Voltage Ripple at the Output Port with the Proposed Operation

The proposed operation has the advantage of having a lower voltage ripple at the output port of the converter compared to the traditional operation. In the traditional operation, both transistors switch on and off at the same time, causing both capacitors to charge or discharge at the same time, resulting in the voltage ripples adding up. However, the proposed operation has states in which one capacitor is being charged by its respective inductor while the other is being discharged by the output current, leading to a slower change in output voltage. This happens when one transistor is closed while the other one is open (see Figure 6).

The voltage ripple at the output port can be calculated in different equivalent circuits; let us calculate it during the time when one capacitor is being charged, and the other is being discharged, which occurs for a certain amount of time depending on the duty cycle. The voltage ripple at the output port can be expressed as (20), taking into account that both capacitors are equal and both inductors have the same current (see (9) and (10)). In Equation (20), there is a component (negative) which makes the voltage decrease, while the other component (positive) makes the voltage increase, a difference which results in a kind of cancellation of the derivative of the output voltage.

$$\Delta v_{outN} = \begin{cases} \frac{(1-D)T_S}{2}\left(\frac{I_L - 2I_{out}}{C}\right) & if \quad D > 0.5 \\ \frac{DT_S}{2}\left(\frac{I_L - 2I_{out}}{C}\right) & if \quad D < 0.5 \end{cases} \tag{20}$$

4. Comparison with a Design Example and Experimental Results

Experimental results were obtained with: (i) the traditional boost converter; (ii) the LVC converter working in the former operation, and (iii) the LVC converter working in the proposed operation. The same operating condition was reproduced with the three converters for comparison purposes. The results (as will be shown) demonstrate that the proposed operation leads to a lower voltage ripple at the output port with the same components and operating conditions.

Let us first discuss the traditional boost converter's parameters to have a better idea of the capacitor's difference. We can imagine that we use two capacitors in a series of the same capacitance (the capacitances are C_1 = 10 µF and C_2 = 10 µF). The inductor is L = 250 µH, the switching frequency was chosen as f_S = 20 kHz, and the duty cycle of the boost converter for the comparison is D = 0.8. The input voltage is Vin = 15 V. The load resistance is R = 200 Ω. The switches used were the TPH3212PS GaN-FET for all devices.

The duty cycle was chosen to have the same voltage gain that the LVC converter would have when D = 0.6. It is essential to mention that the split of the capacitors does not affect their stored energy and then the total volume. Figure 8 shows the schematic diagram of the boost converter, and Figure 9 shows some key waveforms of the operation.

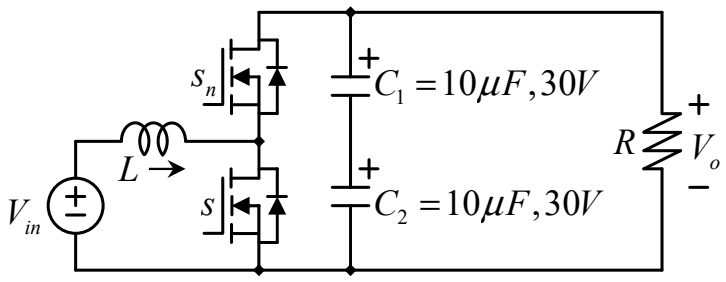

Figure 8. Schematic of the traditional boost converter.

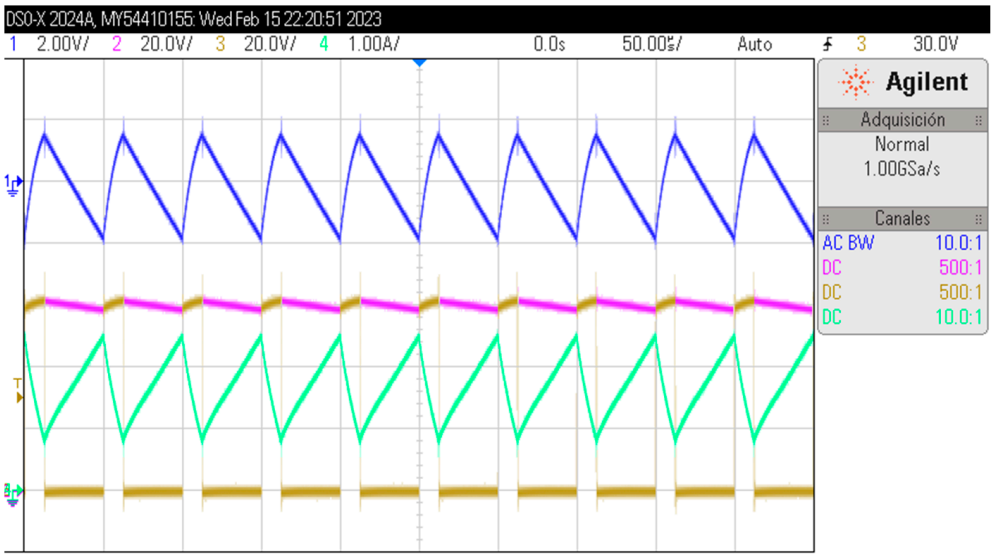

Figure 9. Signals in the traditional boost from the bottom to the top, the switch voltage (gold), the inductor current (green), the output voltage (purple), and a zoom in the output voltage ripple (blue).

The voltage at the switch s_a is depicted in dark gold color at 20 V per division (see Figure 9); it seems like a square signal whose peak is at approximately 60 V (the same as the output voltage). The input voltage is 15 V, and the output voltage is 60 V. If we have only one capacitor, the output capacitor must also block the output voltage (60 V), in the case of the split capacitors, each of them blocks 30 V. The green triangular waveform is the inductor current at $1A$ per division. The pink signal is the output voltage at 20 V per division, and the blue signal is the zoom in the output voltage ripple, basically the output voltage with ac coupling and a zoom-in at 2 V per division.

The parameters of the LVC converter are inductors L_1 and L_1 are L_1 = 250 µH, L_2 = 250 µH, capacitors are C_1 = 10 µF, and C_2 = 10 µF, the switching frequency f_S = 20 kHz, and the duty cycle D = 0.6. The input voltage is Vin = 15 V. The load resistance is R = 200 Ω. Figure 10 shows the schematic diagram of the LVC converter.

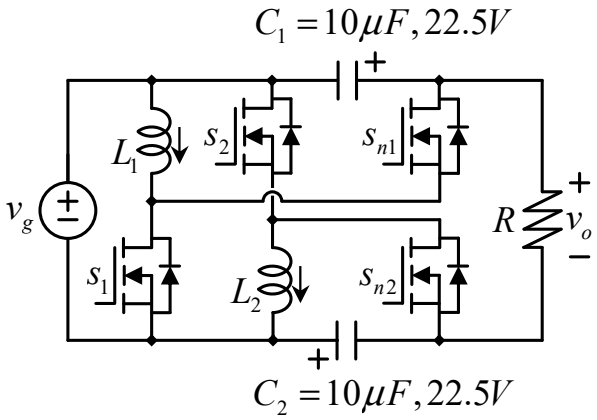

Figure 10. Schematic of the LVC converter used for the experimental results.

Figure 11 shows some key waveforms of the LVC converter in the traditional operation, while Figure 12 shows the same waveforms for the proposed operation.

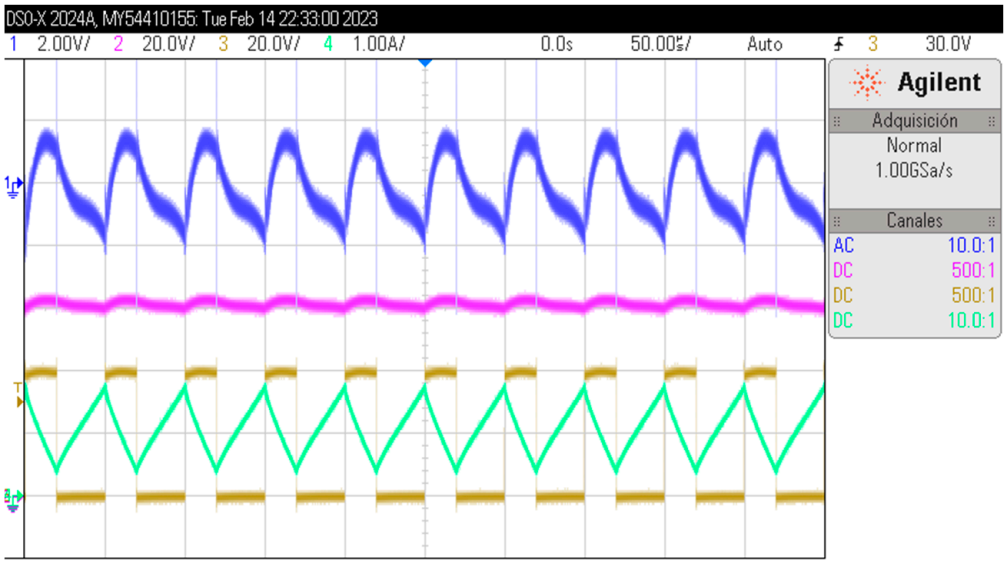

Figure 11. Signals in the traditional operation, from the bottom to the top, the switch voltage (gold), the inductor current (green), the output voltage (purple), and a zoom in the output voltage ripple (blue).

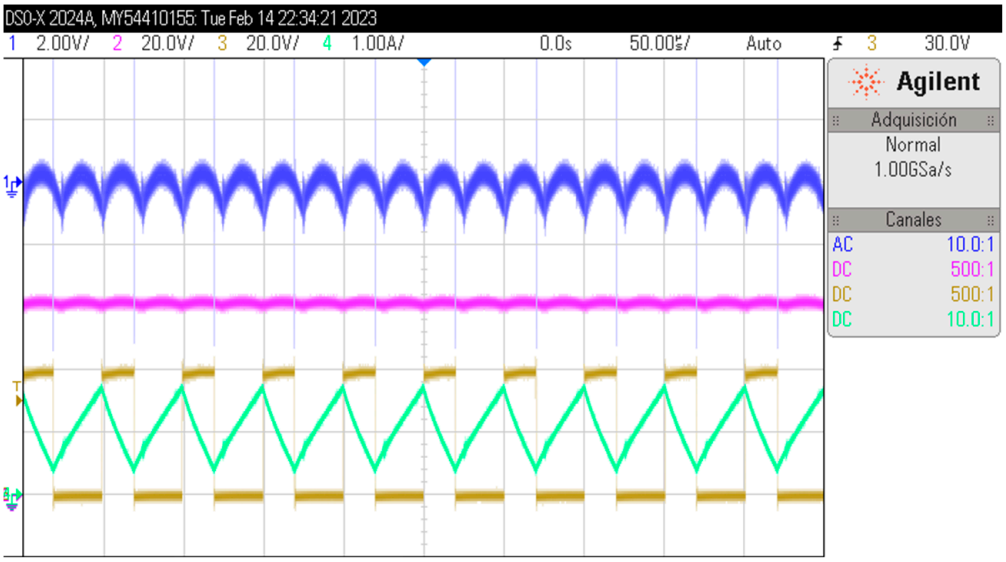

Figure 12. Signals in the proposed interleaved PWM operation, where the voltage ripple at the output port (blue signal) is evidently smaller, from the bottom to the top, the switch voltage (gold), the inductor current (green), the output voltage (purple), and a zoom in the output voltage ripple (blue).

The colors and resolution of the signals are equal to the boost converter. In dark gold color (see Figures 11 and 12), the voltage at the switch s_a is depicted at 20 V per division; this seems like a square signal with its peak at approximately 40 V. The input voltage is 15 V, and the output voltage is 60 V, the voltage blocked by transistors when they are open is also smaller than the output voltage, which is another advantage over other step-up topologies, in which transistors must be rated to block the output voltage. Devices always require a larger voltage to have a security margin, but this is usually a percentage of their real voltage; for example, if 100% of safety margin is chosen, transistors in this converter would be rated to 80 V (to block 40 V), but in a converter in which they block 60 V, we would need 120 V devices. The green triangular waveform is the inductor L_1 current at $1A$ per division. It can be seen that their average current is at approximately $1A$; this signal was also used as the trigger for the oscilloscope. The pink signal is the output voltage at 20 V

per division, which is at approximately 60 V, and the blue signal is the zoom in the output voltage ripple, as the output voltage has ac coupling and a zoom-in at 2 V per division.

Compared to the boost converter, the voltage across the switches and capacitors is smaller. The LVC converter has the advantage of requiring less stored energy in capacitors. For example, instead of capacitors of 30 V, it requires capacitors of 22.5 V. Nonetheless, the output voltage ripple in the LVC converter and the boost converter is quite similar and it is a bit smaller in the LVC converter, but its main advantage is the output voltage reduction. However, it can be observed that the LVC converter with the proposed operation has a significantly smaller output voltage ripple than the LVC in the traditional operation, and is also smaller than the boost converter.

The ripple reduction factor can be established at approximately 50% since the output voltage ripple in the LVC with the proposed operation is at approximately 0.9 V, while the output voltage ripple of the boost converter and the LVC converter is at approximately 1.8 V.

The only disadvantage of the proposed operation is that it requires two comparators in the microcontroller, while the traditional operation requires only one. If the comparison is made by software, this will result in two times the operations compared to the traditional version.

Figure 13 shows a photograph of the experimental setup, which was made based on the bidirectional boos (half-bridge) evaluation board TDHBG1200DC100-KIT from the Transphorm brand, and modifications were performed to achieve the proposed topology with two half-bridge modules.

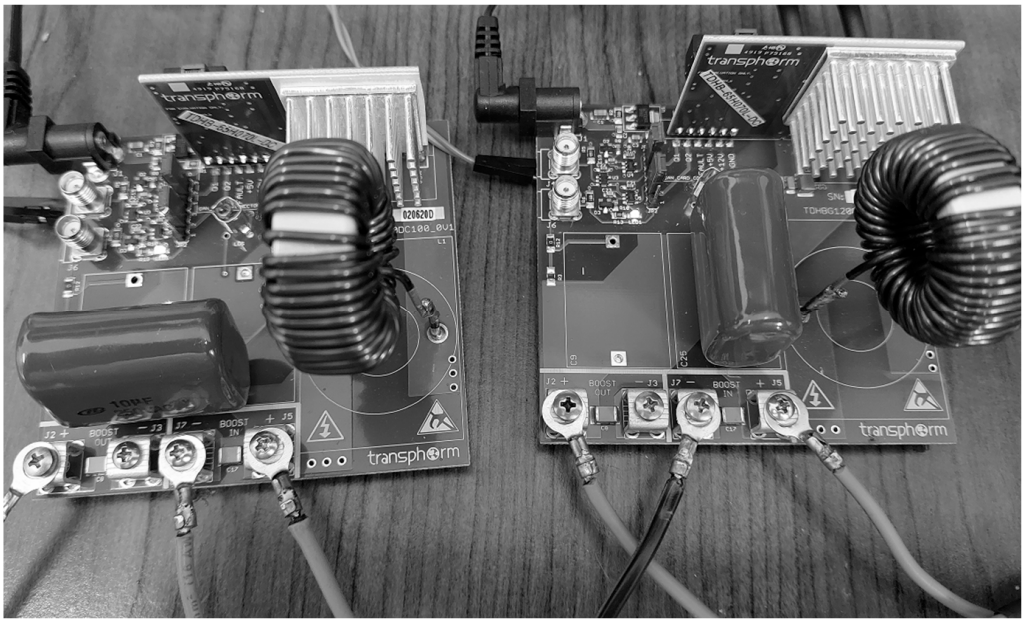

Figure 13. Photograph of the experimental setup.

Numerical Comparison of Losses

Finally, the losses of the three converters were calculated for comparison purposes. Table 1 shows the parameters used for this purpose.

Table 1. Parameters for losses calculation.

Parameter (Equal for All)	Value
Inductance of inductors	$L = L_1 = L_2 = 250$ µH
Inductors equivalent series resistance	$L_{esr} = 50$ mΩ
Capacitance of capacitors	$C_1 = C_2 = 10$ µF
Capacitors equivalent series resistance	$C_{esr} = 5$ mΩ
Switches on-resistance	$S_{on\text{-}res} = 85$ mΩ
Switches switching time (wors selected)	$S_{time} = 100$ nS
Switching frequency	$f_S = 20$ kHz

Table 2 shows the losses in the LVC with the proposed operation, and no significant losses were observed in the LVC converter with the former and the proposed operation, and then the comparison was made with the traditional boost vs. the LVC converter in the proposed operation.

Table 2. Losses of the LVC converter in the proposed operation.

Losses	Value
Inductor L_1	90.3 mW
Inductor L_2	90.3 mW
Capacitor C_1	4 mW
Capacitor C_2	4 mW
S_1 switching losses	53.8 mW
S_1 conduction losses	92.1 mW
S_{1n} switching losses	---
S_{1n} conduction losses	61.4 mW
S_2 switching losses	53.8 mW
S_2 conduction losses	92.1 mW
S_{2n} switching losses	---
S_{2n} conduction losses	61.4 mW

From the comparison, we can see that although the proposed converter has more switches, they split the current among them, and the conduction losses are proportional to the square of the current. Furthermore, their reduced voltage helps reduce the power losses in each transistor. Something similar happened with the inductor. The current split among L_1 and L_2 helped reduce the losses compared to having a single inductor. However, the difference in power losses is relatively low; the main advantage of the LVC converter in the proposed operation is the significant reduction in the voltage ripple at the output port without increasing the stored energy in the capacitors or any other parameter.

Table 3 shows the losses in the boost converter in the described operating point.

Table 3. Losses of the traditional boost converter.

Losses	Value
Inductor L	221.1 mW
Capacitor C_1	7.4 mW
Capacitor C_2	7.4 mW
S_1 switching losses	231.5 mW
S_1 conduction losses	281.9 mW
S_{1n} switching losses	---
S_{1n} conduction losses	94.0 mW

5. Conclusions

This work proposes an improvement operation for a recently proposed converter. The low-voltage in capacitors (LVC) converter offers a high voltage gain while operating with low voltage in their capacitors (lower than at the output). The improvement consisted of a modification in the pulse width modulation (PWM) scheme that allows a reduction

in the voltage ripple at the output port without modifying the circuit parameters. The LVC converter contains two transistors, and it was proposed that these were operated with a single switching function. The new PWM scheme consists of two switching signals with a phase shift among them of 180°, such as the interleaved converter. Compared to the previous operation, the converter presents a smaller voltage ripple at the output port (without changing the capacitors or the switching frequency). The converters' mathematical model was presented, and the experimental results proved the advantage of the proposed operation in reducing the voltage ripple at the output port. As a future work, the authors may have developed two converters with different capacitors but the same output voltage ripple to evaluate the percentage of stored energy (or volume) that the converter requires in the proposed operation to achieve the same output voltage ripple as in the former operation.

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