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Atomic Layer Deposited SiO_X-Based Resistive Switching Memory for Multi-Level Cell Storage

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Abstract: Herein, stable resistive switching characteristics are demonstrated in an atomic-layer-deposited SiO_X-based resistive memory device. The thickness and chemical properties of the Pt/SiO_X/TaN stack are verified by transmission electron microscopy (TEM) and X-ray photoemission spectroscopy (XPS). It is demonstrated that much better resistive switching is obtained using a negative set and positive reset compared to the opposite polarity. In addition, multi-level switching is demonstrated by changing the compliance current (CC) and the reset stop voltage, and potentiation and depression are emulated by applying pulses to achieve a synaptic device. Finally, a pulse endurance of 10,000 cycles and a retention time of 5000 s are confirmed by modulating the pulse input and reading voltage, respectively.

Keywords: memristor; resistive switching; synaptic devices; silicon oxide

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1. Introduction

For non-volatile memory (NVM) applications, resistive random-random access memory (RRAM) has several advantages, such as a simple metal–insulator–metal (MIM) structure, superior storage capacity with small component size, fast switching speed, low power consumption, non-volatility, multi-level data storage ability, and long retention time [1–7]. In particular, RRAM has the potential to implement multiple conductive levels in one cell, thereby facilitating a high storage density by the implementation of multiple bits in the NVM [8–10], and has made possible the quasi-analog modulation of synaptic weight in the artificial neural network (ANN) [11–17]. Furthermore, RRAM can solve the various disadvantages of dynamic random-access memory (DRAM) and flash memory. For instance, DRAM has volatile characteristics when processing data quickly [18], whereas flash memory is non-volatile but exhibits slow data processing and requires high voltage operation [19].

Due to the above-mentioned advantages, RRAM has been used to implement a neuromorphic computing architecture [11–17]. The importance of neuromorphic computing architecture begins with solving the bottleneck problem caused by the use of a data bus for data exchange in the von Neumann architecture. This problem has emerged in recent years due to the increased amount of data to be processed in artificial intelligence (AI) development. The neuromorphic computing architecture can solve this problem by imitating the human brain structure in order to process data in parallel with low power consumption. While various novel resistance-based memory devices are attracting attention for the implementation of the neuromorphic computing architecture, including phase-change random-access memory (PRAM) [20] and magnetic random-access memory (MRAM) [21], the RRAM devices are particularly attractive due to their above-mentioned advantages.

To obtain reliable resistive switching characteristics with small variation, the thickness of the RRAM device should be uniform. In this respect, the self-limiting process of atomic

layer deposition (ALD) enables the fabrication of thin films with very exact thicknesses and is especially suitable for the vertical RRAM structure [22]. In the present work, the multi-level cell (MLC) characteristics of an ALD-fabricated Pt/SiO_X/TaN device are examined via I-V curves and pulse modulation. In addition, the thickness of the stack device is estimated via transmission electron microscopy (TEM). Further, the MLC characteristics are observed by varying the compliance current (CC) and reset stop voltage in direct-current (DC) sweep mode, and high endurance is demonstrated by the pulse response.

2. Experiments

The RRAM samples were fabricated using the following procedures. A 100-nm thick TaN bottom electrode was deposited by reactive sputtering onto the SiO_2/Si substrate. The SiO_x was deposited via the following sequential ALD protocol: di-isopropylaminosilane (SiH_3N $(C_3H_7)_2$, DIPAS), 0.8 s; N_2 purge, 15 s; ozone (O_3) 0.5 s; N_2 purge, 15 s, with a total of 40 cycles at a stage temperature of 450 °C. Finally, a 100-nm thick Pt top electrode was deposited via e-beam evaporation with a shadow mask containing a pattern of circles with a diameter of 100 µm. The chemical and material characteristics of the ALD-deposited SiO_X film were examined via X-ray photoelectron spectroscopy (XPS). The electrical characteristics of the RRAM cells were measured and recorded using a semiconductor parameter analyzer (Keithley 4200-SCS and 4225-PMU ultrafast module) in the voltage sweep and pulse modes with the bottom electrode grounded and a bias applied to the top electrode.

3. Results and Discussion

A schematic diagram of the Pt/SiO_X/TaN RRAM structure is presented in Figure 1a, where multiple Pt electrodes are separated from each other to provide independent memory cells while the insulating SiO_X film covers the entire TaN surface. The TEM image in Figure 1b reveals a thickness of ~6 nm for the amorphous SiO_X layer. The interface of SiO_x on the TaN layer is rather rough even though SiO_x was deposited by ALD. The XPS core level Si 2p spectrum of the SiO_X film is presented in Figure 2a. Here, the peak centered at a binding energy of 103.7 eV corresponds to the non-stoichiometric Si–O bond [23]. Meanwhile, the O 1s spectrum in Figure 2b exhibits two peaks centered at 530.87 eV and 533.02 eV [23]. A further peak corresponding to the non-stoichiometric Si–O bond was also observed at higher binding energy.

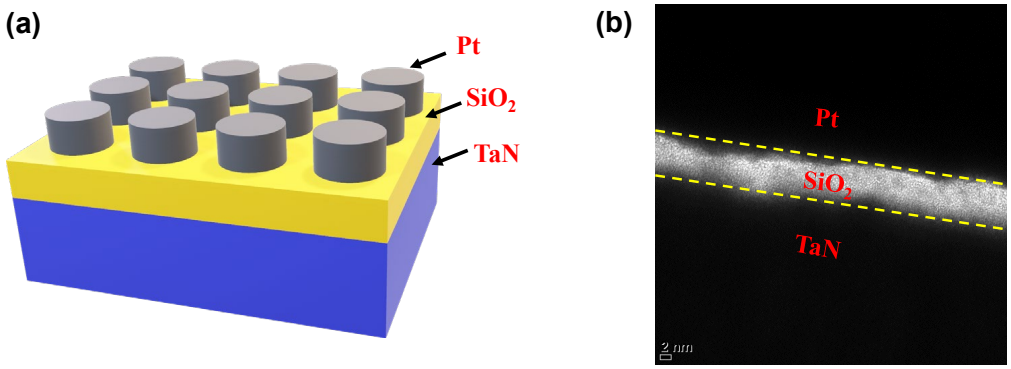

Figure 1. A schematic diagram (**a**) and cross-sectional TEM image (**b**) of the Pt/SiO_X/TaN RRAM device.

The resistive switching characteristics of the device in the DC sweep mode according to operation polarity are presented in Figure 3. In the positive forming process (Figure 3a), the I-V curve reveals reverse filament formation (RFF) during the first switching. This indicates that conducting filaments with sufficient defects are initially formed in the SiO_X, and these can be ruptured upon application of a bias. The ruptured filament can reform with a sudden rise in current during the set process, but the subsequent reset process does not occur fluently because the Pt electrode does not contain enough oxygen. By contrast, stable bipolar resistive switching is achieved by using a negative set and positive reset voltage, as shown in Figure 3b. Here, the set process is accompanied by a sharp rise in current within

a set voltage range of −0.61 V to −1.02 V, thus indicating the formation of conducting filaments in the SiO_X layer. Subsequently, the reset process begins at ~0.92 V, and the current gradually decreases over a wide voltage range. This indicates that the filament is only gradually ruptured, which is suitable for voltage-controlled MLC applications. The detailed switching and conduction mechanisms of SiOx-based RRAM were explained by previous literature [24,25].

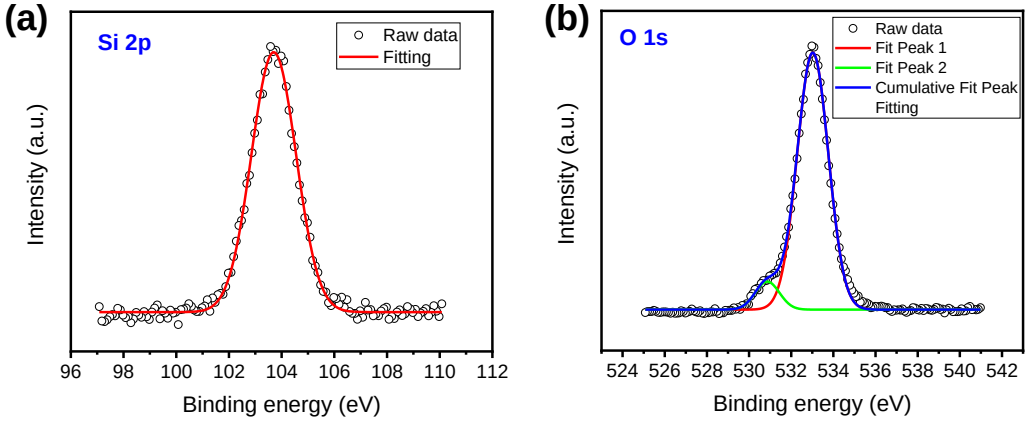

Figure 2. The XPS core level spectra of the ALD deposited SiO_X film: (**a**) Si 2p; (**b**) O 1s.

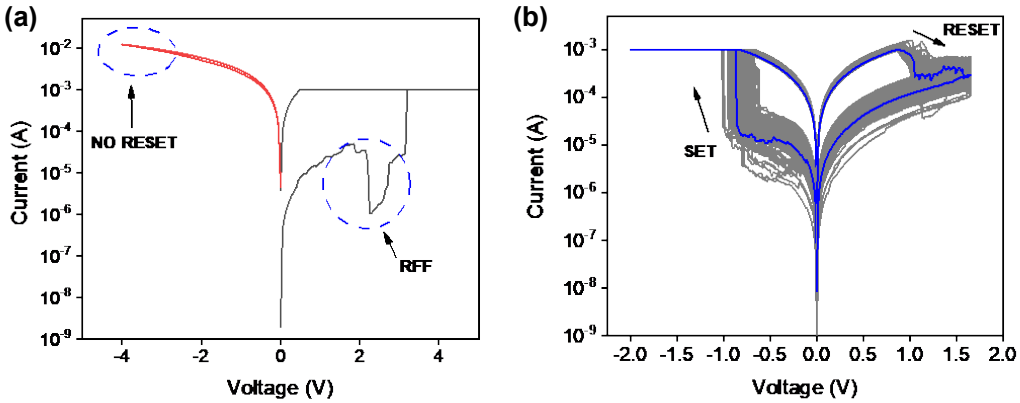

Figure 3. The I-V characteristics of the Pt/SiO_X/TaN RRAM device under (**a**) positive set and negative reset operation, and (**b**) negative set and positive reset operation.

The MLC characteristics of the Pt/SiO_X/TaN RRAM device are implemented by varying the compliance current and the reset stop voltage, as shown in Figure 4. Thus, in Figure 4a, the compliance current is increased from 0.1 to 1.0 mA in increments of 0.1 mA, and the currents in both the low and high resistance states are seen to increase with increasing compliance current. This demonstrates that the size of the conducting filament can be successfully controlled by modulating the compliance current.

The bipolar resistive switching (set/reset) characteristics obtained by controlling the compliance current only are presented in Figure 4b. Here, the low-resistance state is effectively changed by changing the compliance current, but no obvious change is observed in the high-resistance state. Meanwhile, the I-V curves obtained by varying only the reset stop voltage for the same compliance current are presented in Figure 4c. Here a significant variation in the high resistance state is observed according to the reset stop voltage. The MLC characteristics are then further demonstrated for practical memory operation by the application of multiple sets and reset pulses of −0.81 V and +1 V (Figure 4d). To minimize the read disturbance, a read voltage of 0.2 V was used to obtain the conductance values. Thus, while there is some variability, the conductance exhibits an overall increase with 50 negative pulses and an overall decrease with 50 positive pulses. Thus,

it is possible to increase and decrease the conductance of the RRAM device by imitating the potentiation and depression processes that strengthen and weaken the connections between biological synapses. This MLC process is, therefore, suitable for hardware-based neuromorphic systems.

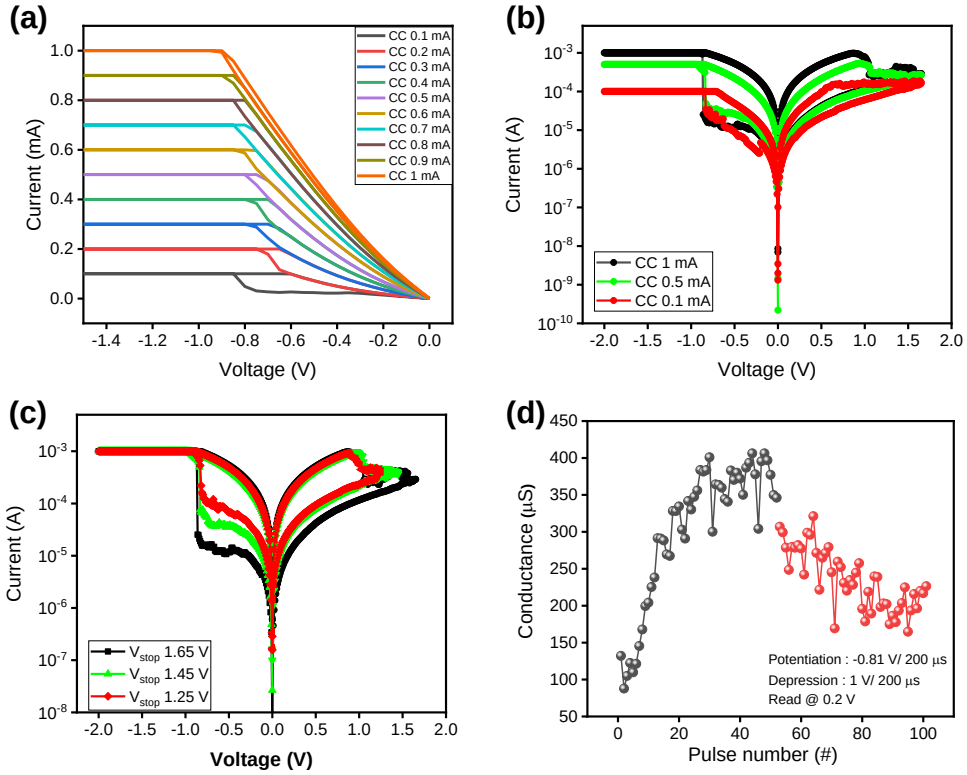

Figure 4. The MLC characteristics of the Pt/SiO_X/TaN RRAM device: (**a**) plots of the low-resistance current with various compliance currents; (b and c) controlling the bipolar resistive switching via (**b**) the compliance current and (**c**) the reset stop voltage; (**d**) potentiation (black) and depression (red) by the application of negative and positive pulses, respectively.

Finally, the stable endurance and retention characteristics of the Pt/SiO_X/TaN RRAM device for reliable non-volatile memory applications are demonstrated in Figure 5. The conductance values of the high and low resistance states during cyclic application of the set (−3 V) and reset (4 V) pulses, with a read voltage of −1 V, are presented in Figure 5a. Here, good pulse endurance is demonstrated for up to 10,000 cycles with an on/off ratio of about 4. The time-dependent data-retention properties are indicated in Figure 5b, where the high and low resistance states were obtained by a DC sweep. Here, both resistance states are maintained without significant degradation for 5000 s, thereby demonstrating that the Pt/SiO_X/TaN device has non-volatile memory properties.

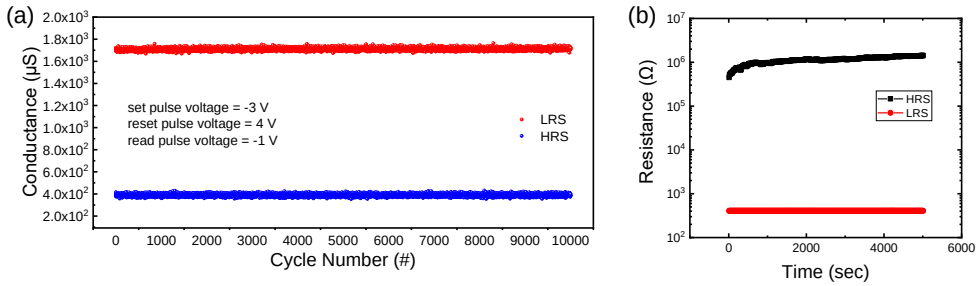

Figure 5. (**a**) Pulse endurance and (**b**) and retention properties of the Pt/SiO_X/TaN RRAM device.

4. Conclusions

Herein, the resistive switching of an atomic-layer-deposited (ALD) SiO_X-based resistive random-random access memory (RRAM) device was demonstrated for mutli-level cell (MLC) storage. The thickness and chemical properties of the device were investigated by transition electron microscopy (TEM) and X-ray photoelectron spectroscopy (XPS), respectively. Bipolar resistive switching was shown to occur more easily under a negative set and positive reset operation than in the opposite polarity due to oxygen exchange in the TiN layer. For MLC, the compliance current and reset stop voltage were used to control the low and high resistance values. In addition, for neuromorphic applications, potentiation and depression were demonstrated by pulse application. Finally, the retentions of the high and low resistance states were verified for 5000 s and 10,000 cycles of alternating current (AC) endurance.

Author Contributions: J.S., G.N. and S.K. (Sungjoon Kim) conducted the electrical measurements and process, and Y.L. and D.C. wrote the manuscript; J.J. and S.K. (Sungjun Kim) supervised the study. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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