



Supporting Information



Figure S1. Molecule structures of the small molecule organic semiconductor and the high-k polymer semiconductor binder used for the blend.



Figure S1. Square root and logarithmic scale transfer curves of both geometries types for the two behaviour of the transistors: a) lineal region, b) saturation region including the threshold voltage extraction procedure representation.



Figure S2. Experimental transfer characteristics for Corbino and interdigitated geometries normalized to Channel Dimension (CD) for V_{DS}= -2 V.



Figure S3. Experimental output characteristics of interdigitated geometry devices where gate voltage (V_{GS}) were swept by -10 V from -30 V to 10 V. The channel length is 10 μ m.



Figure S4. Output characteristics of the Corbino TFT for the two drain-bias conditions: a) inner circle as source and outer ring as drain, b) inner circle as drain and outer ring as source.



Figure S5. Turn on voltage of both geometries from the curve transfer curve with V_{DS} = -20 V. Central mark the median, box limits indicates the 25th and 75th percentiles, whiskers extend to 5th and 9th percentiles.