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NBTI and Power Reduction Using an Input Vector Control and Supply Voltage Assignment Method

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Received: 5 June 2017; Accepted: 13 August 2017; Published: 19 August 2017

Abstract: As technology scales, negative bias temperature instability (NBTI) becomes one of the primary failure mechanisms for Very Large Scale Integration (VLSI) circuits. Meanwhile, the leakage power increases dramatically as the supply/threshold voltage continues to scale down. These two issues pose severe reliability problems for complementary metal oxide semiconductor (CMOS) devices. Because both the NBTI and leakage are dependent on the input vector of the circuit, we present an input vector control (IVC) method based on a linear programming algorithm, which can co-optimize circuit aging and power dissipation simultaneously. In addition, our proposed IVC method is combined with the supply voltage assignment technique to further reduce delay degradation and leakage power. Experimental results on various circuits show the effectiveness of the proposed combination method.

Keywords: negative bias temperature instability; leakage power; input vector control; supply voltage assignment; linear programming

1. Introduction

As technology scales, reliability issues have become a vital concern in Very Large Scale Integration (VLSI) design. Among these reliability issues, performance degradation induced by negative bias temperature instability (NBTI) is one of the primary failure mechanisms when the feature size approaches the 65 nm scale [1]. NBTI occurs when positive-channel Metal Oxide Semiconductor (pMOS) transistors are negatively biased ($V_{gs} = -V_{dd}$), which causes a shift in the threshold voltages (V_{th}). Meanwhile, under the actual alternating current (AC) stress condition, when the stress voltage is removed periodically ($V_{gs} = 0$), the magnitude of the V_{th} partially recovers toward its initial value. However, the recovery phase can only partially compensate for the NBTI effect [2]. Therefore, the threshold voltage of a pMOS transistor will increase over time, and this results in degradation of circuit performance. Once the critical path delay exceeds the limit, the circuit begins to fail.

Another critical issue for VLSI design is excessive power consumption as the density of a device is dramatically increased. Traditionally, dynamic power is the main source of the total power of a device. However, as the supply and threshold voltage for VLSI circuits decreases, the leakage power dramatically increases [3]. According to the International Technology Roadmap for Semiconductors (ITRS), leakage power will contribute to over 50% of the total power in next-generation processors [4]. Excessive power dissipation will reduce the service life of an electronic system and result in some potential reliability problems, especially for those devices that require the battery to supply power, such as mobile phone and wireless sensor networks [5].

Both NBTI-induced delay degradation and excessive leakage power will significantly reduce the operational lifetime of VLSI circuits; therefore, many researchers have proposed different NBTI and/or leakage reduction methods from different levels of design abstraction. Power gating [6], internal

node control [7,8], circuit-aging sensors [9], adaptive body bias and supply voltage techniques [10], and input vector control (IVC) [11,12] are some representative methods. Among these methods, IVC is commonly used because of its low overhead in terms of performance and area cost. IVC was proposed initially to reduce the leakage power of complementary metal oxide semiconductor (CMOS) devices. It is based on the well-known transistor stacking effect: A CMOS gate's leakage current dramatically varies with the input vector applied to the gate [13]. Additionally, not every practical application requires the underlying hardware to perform at the highest speed all of the time; circuits often periodically switch between active and standby mode, and the standby time is often longer than the active time [7]. Therefore, the concept of IVC is to find the minimum leakage vector (MLV) that can reduce the leakage power when the circuit is in standby mode.

In addition to leakage power, the NBTI effect is also dependent on an input vector. Therefore, IVC can also be applied to alleviate the NBTI effect on a VLSI circuit. Similar to leakage power reduction, the idea of IVC in NBTI mitigation is to find the minimum degradation vector (MDV) that can help the pMOS transistors in the circuit stay in a recovery phase as long as possible. However, in a real circuit, there exists logic interdependency between different gates, and we cannot control all of the pMOS transistors in a recovery state. Moreover, experimental results show that the recovery state can only partially alleviate the NBTI effect. Therefore, a circuit will still endure severe NBTI-induced delay degradation using IVC only, especially a large circuit. In an application where timing is critical, some supplemental methods need to be implemented together with IVC to guarantee the performance of the circuit. Wang et al., proposed two kinds of gate replacement methods, and combined them with an IVC approach to reduce the leakage power and NBTI effect simultaneously [7]. Bild et al., proposed a combination method of internal node control (INC) and IVC, and also proposed a linear-time heuristic that can quickly determine the near-optimal placements for INC selection [14]. Lin et al. proposed a transmission gate (TG) insertion method, and applied an integer linear programming (ILP) formulation to select the location for TG insertion [15]. Experimental results have demonstrated that compared with IVC only, the above methods can improve the controllability of the state of the internal gates significantly, leading to better NBTI mitigation and leakage reduction. However, these methods will change the structure of the device and bring in extra power and area penalties.

Recently, some kinds of adaptive method have been proposed to mitigate the aging effect of CMOS devices. These methods will adjust the working parameters of the devices, such as frequency, body bias voltage, and supply voltage, according to the aging rate. Kumar et al., proposed the use of adaptive body bias (ABB) and adaptive supply voltage (ASV) to guarantee the performance of a CMOS circuit. They also proposed a hybrid approach with ABB and synthesis to mitigate the aging effect [16]. Lee et al., proposed a method to find a set of supply and body biasing voltage values, and apply them to circuit clusters in a standard cell-based design, which can minimize the total power consumption while satisfying the circuit performance requirement [17]. Zhang et al. proposed a scheduled voltage scaling technique, which increases the supply voltage gradually to compensate for NBTI-induced degradation [18]. In [19], the authors proposed an adaptive method to tune the parameters of a digital system, such as supply voltage and clock frequency, over its lifetime in the presence of circuit aging. They also proposed three kinds of control policies to tune the operating parameters of the system. Chen et al., proposed a supply voltage assignment method to co-optimize power consumption and NBTI effect for the CMOS devices [10]. Among these methods, supply voltage assignment (SVA) is commonly used because of its easy implementation, and we also use SVA to compensate for NBTI-induced delay degradation in this paper.

However, to our knowledge, no references have analyzed the impact of an input vector on the implementation process of the SVA method, and combined the SVA and IVC methods together to reduce the NBTI effect and power dissipation. As discussed before, SVA can effectively compensate for performance degradation by increasing the supply voltage (V_{dd}) of the circuit. However, a high V_{dd} will also result in an increase of power consumption, as well as an accelerated aging process. Because both the NBTI effect and leakage power are dependent on the input vector in standby mode, the circuit

designer should find the optimal input vector that can reduce NBTI and leakage simultaneously. However, the impacts of the input vector on delay degradation and leakage power are not in a same direction; the optimal input vector for minimizing the postaging delay may not be the best one to minimize the leakage power and vice versa. In order to solve this problem, a novel NBTI and leakage co-optimization algorithm based on an ILP formulation is proposed in this paper. This method can consider these two issues simultaneously and find the optimal input vector that can provide a balanced tradeoff between performance and power. Then, the globally best input vector is used when the circuit is in standby mode, and SVA is applied as a subsequent method to further mitigate NBTI effect while reducing the power dissipation at the same time.

The remainder of this paper is organized as follows. In Section 2, basic NBTI-induced delay degradation and power computation models are introduced. The procedure for our proposed co-optimization ILP formulation and the combination of the SVA and IVC methods are described in Section 3. A verification of the effectiveness of the proposed method is presented in Section 4. Finally, conclusions are presented in Section 5.

2. Preliminaries

2.1. NBTI-Induced Transistor Aging

An effective prediction of circuit performance aging depends on an accurate NBTI model; however, NBTI's physical mechanism is still a subject of debate, and different models have been proposed. In general, the Reaction Diffusion (R-D) model and the Trapping Detrapping (T-D) model are two widely accepted physical theories to explain the NBTI effect [20]. The R-D model involves the breaking of Si-H bonds in Si-SiO_2 and the generation of interface traps. The change of threshold voltage (ΔV_{th}) follows a power law function of aging time [11]. In comparison, the T-D model involves a charge trapping/detrapping, and ΔV_{th} follows a logarithmic function of the stress time [21]. Recent work reveals that there exists a significant amount of permanent degradation from the NBTI effect, and a new kind of Hydrogen Release (H-R) model has been proposed which can explain this phenomenon [22,23]. In the H-R model, hydrogen is assumed to release from the gate side of the oxide to migrate towards the channel, which in turn increases ΔV_{th}. The H-R model can explain the depassivation of Si-H bonds and the passivation of channel dopants, as well as the sensitivity of the permanent component to the H concentration introduced during fabrication. The authors also claim that the reaction-limited model is a special case of the H-R model [22]. Different models can explain the NBTI effect and match the experimental data under different measurement conditions. For example, the R-D model has been verified to be effective for a moderate to very long stress time [24]. In contrast, the T-D model is capable of predicting ultrafast measurement data more precisely; moreover, the T-D model can also capture the aging variability of the NBTI effect [21,25,26].

Regardless of the argument for NBTI's mechanism, some features about the NBTI effect are widely known and accepted. For example, NBTI increases with an increase in negative stress gate bias; therefore, the NBTI-induced ΔV_{th} is dependent on the actual workload of the circuit. In addition, NBTI increases at an elevated temperature and shows Arrhenius T activation; NBTI recovers quickly after the stress is removed, and measured ΔV_{th} and related parameters are sensitive to measurement delay [24]. In this paper, we will not cast our focus on NBTI's physical model but on a method to alleviate NBTI-induced performance degradation while reducing power dissipation to the greatest extent. Since the R-D model can describe the NBTI effect for a long period of stress time, in this paper, we use the R-D-based long-term predictive model for NBTI. In our future work, we will discuss the effectiveness of our proposed method when using the other popular NBTI models.

The long-term NBTI model for calculating the threshold voltage shift for the pMOS transistor is expressed as follows [11]:

$$|\Delta V_{th}| = \left(\sqrt{K_V^2 \times T_{clk} \times \alpha} / (1 - \beta_t^{1/2n}) \right)^{2n} \quad (1)$$

$$\beta_t = 1 - \left(2\xi_1 \times t_e + \sqrt{\xi_2 \times C \times (1-\alpha) \times T_{clk}}\right) / \left(2t_{ox} + \sqrt{C \times t}\right) \quad (2)$$

$$K_V = (q \times t_{ox}/\varepsilon_{ox})^3 \times K^2 \times C_{ox} \times (V_{gs} - V_{th}) \times \sqrt{C} \times e^{2E_{ox}/E_0} \quad (3)$$

where T_{clk} is the period of a single stress and recovery cycle, $\xi_1 = 0.9$ and $\xi_2 = 0.5$ are two constants, t_{ox} is the oxide thickness, t_e either equals t_{ox} or the diffusion distance of hydrogen at the initial stage of recovery, n is a time exponent and is equal to $1/6$ for an H_2 diffusion model, q is the electron charge, $K = 8 \times 10^4$, C_{ox} is the oxide capacitance per unit area, $E_{ox} = V_{gs}/T_{ox}$, $C = 1/T_0 \exp(-E_a/kT)$, the temperature T is set to 300 K, $E_a = 0.49$ eV, $T_0 = 10^{-8}$, and $E_0 = 0.335$ V/nm. Note that ΔV_{th} is strongly dependent on the input signal duty cycle (α), which reflects the fraction of time that the transistor spends in the stress state over one cycle. Moreover, the circuit often periodically switches between the active and standby modes. Since our goal is to analyze the impact of the NBTI effect over the total lifetime of the circuit, both active and standby periods must be considered. Therefore, an AC NBTI model should be considered with the equivalent duty cycle. In this paper, we calculate a circuit's overall duty cycle in this manner. When the pMOS transistor is in the recovery phase in standby mode, the duty cycle (α) for this transistor is

$$\alpha = c \times R_{AS}/(R_{AS} + 1) \quad (4)$$

where c is the transistor duty cycle in the active period, and R_{AS} represents the ratio between the active and standby modes. In addition, if the transistor is in the stress phase in the standby mode, then the duty cycle (α) for this transistor is

$$\alpha = (c \times R_{AS} + 1)/(R_{AS} + 1). \quad (5)$$

Another important issue that should be considered in the NBTI model is the stacking effect when multiple transistors are connected in series. Because the influence of the stacking effect on the NBTI effect has been discussed in detail in Ref. [27], it will not be discussed here.

2.2. Path-Based NBTI Model

The propagation delay of a logic gate D_g is dependent on many factors, such as load capacitance, input transition time, and the V_{th} of an internal transistor. In this paper, we assume that the delay of a complex gate is proportional to the delay of a standard inverter gate, and the delay of a logic gate can be modeled similar to the alpha-power law of an inverter [28], which is shown as:

$$D_g = C_L \times V_{dd}/I_D = A/(V_{gs} - V_{th})^{\mu} \quad (6)$$

where V_{dd} is the supply voltage, I_D is the drain current, C_L is the load capacitance, V_{gs} is the voltage between the gate and source terminals, A is a technology-dependent factor, and μ is a measure of velocity saturation. In order to analyze the NBTI effect, it is necessary to acquire the relationship between the gate delay increase (ΔD_g) and the ΔV_{th}. Therefore, we use the one-order Taylor series expansion of Equation (6) to express the function relationship between ΔV_{th} and ΔD_g.

$$\Delta D_g = \frac{\mu \times D_g}{V_{gs} - V_{th0}} \times \Delta V_{th} \quad (7)$$

where V_{th0} is the transistor's original threshold voltage, and D_g is the fresh delay of the gate. Equation (7) shows that there exists a linear relationship between ΔD_g and ΔV_{th}. In order to measure the error of Equation (7), we conduct HSPICE simulation on some basic gates with a predictive technology modeling (PTM) 65 nm model [11], e.g., an NAND and NOR gate, and the error is below 2% which can meet our requirement.

2.3. Cell-Based Leakage Power Model

In recent years, as the supply/threshold voltage for CMOS circuits continues to scale down, leakage power is becoming a significant fraction of total power dissipation. In current CMOS technologies, there are three main sources for leakage current: the source/drain junction current, the gate direct tunneling current, and the sub-threshold current [3]. Among these leakage current sources, the sub-threshold current I_{sub} is substantially larger than the other leakage current components. I_{sub} is due to the diffusion current of the minority carriers in the channel for an metal oxide semiconductor (MOS) device operating in weak inversion mode, and can be calculated as follows [3]:

$$I_{sub} = K_1 \left(1 - e^{-\frac{V_{ds}}{V_{th}}}\right) e^{\frac{(V_{gs} - V_{th} + \eta V_{ds})}{\lambda V_{th}}} \tag{8}$$

where K_1 and λ are technology dependent parameters, and η is the drain-induced barrier lowering coefficient. Equation (8) shows that I_{sub} is dependent on the V_{th} of the transistor, and the V_{th} increase induced by the NBTI effect can decrease the leakage current for the gate. The leakage power change induced by NBTI over time is not considered in this paper, and we extract the leakage power for each gate with all possible input vectors at the starting time of the circuit, which is the maximum value. Then, these leakage power values are stored in a look-up table for a later ILP formulation process.

Finally, the dynamic power of the circuit can be calculated using Equation (9):

$$P_{\text{dyn}} = \frac{1}{2} f \sum_{i=1}^{N} \alpha_i C_i V_{dd}^2 \tag{9}$$

where f is the clock frequency, α_i is the switching probability of gate i, C_i is the capacitance load of gate i, and N is the total number of gates in the circuit [10].

3. Methodology

In this paper, we propose a combination method of input vector control and supply voltage assignment to reduce delay degradation as well as power dissipation. First, a co-optimization ILP formulation is constructed that considers both the NBTI and leakage reduction requirement. The result of this ILP formulation is the global optimal input vector that can provide a balanced tradeoff between performance and power. Then, the input vector is used when the circuit is in standby mode. Afterwards, the SVA method is applied to further mitigate the NBTI effect while minimizing the power dissipation simultaneously. The flow of the proposed method can be described as Figure 1.

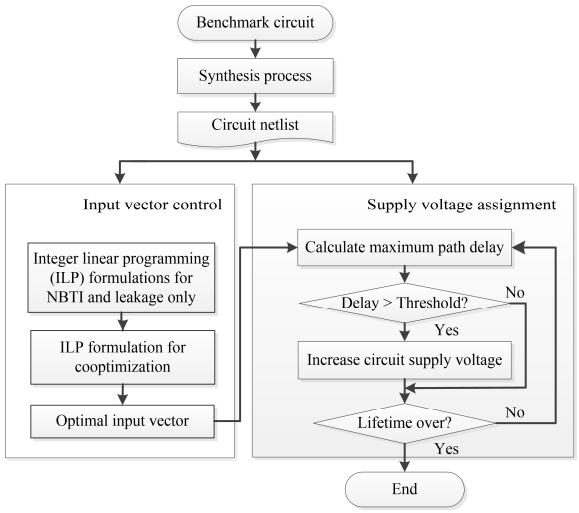


Figure 1. The flow of the proposed input vector control (IVC) and supply voltage assignment (SVA) combination method. NBTI, negative bias temperature instability.

3.1. ILP Formulation for NBTI Mitigation and Leakage Reduction Only

ILP is a kind of mathematical optimization approach consisting of an objective function and a set of linear constraints in a specific format, as follows [29,30]:

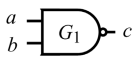
$$\begin{array}{l} \min \mathbf{C}^T\mathbf{X} \\ s.t.\ \mathbf{UX} \leq \mathbf{b} \text{ and } \mathbf{EX} = \mathbf{d} \end{array}. \quad (10)$$

In Equation (10), **X** represents the optimization variables, which is the binary state (0/1) of the circuit node, **C**, **d**, and **b** are vectors of coefficients, and **U** and **E** are matrixes of coefficients. The ILP solvers can be applied to find the optimal value for Equation (10). At present, most of the commercial ILP solvers, such as CPLEX and LINGO, use a branch-and-bound (B&B) algorithm to solve binary integer programming problems [31]. The B&B algorithm searches for an optimal solution by solving a series of linear programming (LP)-relaxation problems, in which the binary integer requirement on the variables is replaced by the weaker constraint $0 \leq x \leq 1$. Then, the algorithm implements the following steps: Search for a binary integer feasible solution; Update the best binary integer feasible point found so far as the search tree grows; Verify that no better integer feasible solution is possible by solving a series of linear programming problems. Compared to the random Monte Carlo simulation and heuristic method, an ILP formulation can find the global best solution. However, the ILP formulation is proved to be an NP-complete problem and could potentially search all 2^n binary integer vectors, where n is the number of variables; some constrains, such as the maximum run-time and number of iteration, should be applied. In this paper, the complexity of the ILP formulation for NBTI mitigation and leakage reduction are not high; therefore, all the problems can be solved in a reasonably short time.

3.1.1. ILP Formulation for NBTI Mitigation

For each path, the NBTI-induced delay degradation is calculated by summing all the delay increases of the gate along that path. Therefore, the ILP formulation for NBTI mitigation is to minimize the total delay increase by considering all the postaging delay in the critical and vulnerable critical path; that is, minimizing the maximum postaging delay in all paths so that the circuit's performance will be maintained to the greatest extent.

Suppose $\mathbf{X} = \{x_i,\ i = 1 \ldots N\}$ is a vector of variables which represents the state (0/1) of each node in standby mode, where N is the number of nodes. Then, the duty cycle, the V_{th} increase, and the delay degradation corresponding to node i and its connected gate can be expressed by a linear function of x_i and an ILP formulation which is compatible with Equation (10) can be generated using a pseudo-Boolean function. For instance, to an NAND gate, its input vector combination and corresponding delay increase is shown in Figure 2.



a	b	Delay increase
0	0	D_{00}
0	1	D_{01}
1	0	D_{10}
1	1	D_{11}

Figure 2. The input vector combination and corresponding delay increase for an NAND gate.

In Figure 2, a and b are the input nodes of an NAND gate, D_{ab} is the delay increase when the input signal value is ab, and D_{ab} is extracted by HSPICE simulation. Then, the NBTI-induced delay increase for the NAND gate can be expressed as:

$$\begin{aligned} \text{Objective function} &= \Delta D \\ &= \overline{a}\overline{b}D_{00} + \overline{a}bD_{01} + a\overline{b}D_{10} + abD_{11} \\ &= (1-a)(1-b)D_{00} + (1-a)bD_{01} \\ &\quad + a(1-b)D_{10} + abD_{11} \end{aligned} . \tag{11}$$

By applying the Boole–Shannon expansion, we can modify Equation (11) into:

$$\begin{aligned} \Delta D =& D_{00} + (D_{10} - D_{00})a + (D_{01} - D_{00})b \\ &+ (D_{00} + D_{11} - D_{01} - D_{10})ab \end{aligned} . \tag{12}$$

In order to express the object function in an ILP-compatible format, it has to be linearized. Since in a NAND gate, $c = 1 - (ab)$, the above equation can be rewritten as:

$$\begin{aligned} \Delta D =& (2D_{00} + D_{11} - D_{01} - D_{10}) + (D_{10} - D_{00})a \\ &+ (D_{01} - D_{00})b - (D_{00} + D_{11} - D_{01} - D_{10})c \end{aligned} . \tag{13}$$

With the same approach, the objective function for an INV and an NOR gate can also be obtained, which is shown in Table 1.

Table 1. ILP objective function for delay degradation of logic gates.

Gate	Logic Function	Objective Function
INV	$b = 1 - a$	$\Delta D = D_0 b + D_1 a$
NAND	$c = 1 - (ab)$	$\Delta D = (2D_{00} + D_{11} - D_{01} - D_{10}) + (D_{10} - D_{01})a + (D_{01} - D_{00})b - (D_{00} + D_{11} - D_{01} - D_{10})c$
NOR	$c = 1 - (\overline{a}\overline{b})$	$\Delta D = (D_{01} + D_{10} - D_{11}) + (D_{11} - D_{01})a + (D_{11} - D_{10})b - (D_{01} + D_{10} - D_{00} - D_{11})c$

Next, the logic circuit functionality should be transformed into a set of linear constraints, so that a reasonable ILP minimization result can be obtained. Table 2 illustrates the set of constraints for basic gates.

Table 2. ILP compatible logic constrains for basic gates [27].

Gate	Logic Constrains
INV	$a + b = 1$
NAND	$c \leq 2 - a - b; c \geq 1 - a; c \geq 1 - b$
NOR	$c \geq 1 - a - b; c \leq 1 - a; c \leq 1 - b$

It should be noted that, in this paper, three kind of logic gates (INV, NAND, and NOR gates) are exploited to synthesize the target circuit. Additionally, when some other kinds of gates (AND, OR, etc. gate) are required in the synthesis process, the Virtual Gate (VG) insertion technique can be used in the ILP formulation, which adds the virtual cells into the circuit to acquire ILP-compatible models [32].

Because of the possible critical path reordering effect induced by NBTI, both the critical and vulnerable critical paths are chosen in the Potential Critical Path (**PCP**) set in analyzing the postaging circuit delay. Supposing that there are L paths in a circuit, the original timing information of each path can be obtained using the static timing analysis (STA) tool. A sorting procedure is carried out for these L paths according to their original delay. If T_i is the largest delay for all the paths, then the **PCP** set is defined as follows:

$$\mathbf{PCP} = \{p_i | D(p_i) \geq 0.9 \times T_i, i = 1, 2, \ldots, M\} \tag{14}$$

where $D(p_i)$ is the original delay of path p_i without considering the NBTI effect, and M is the number of path in the **PCP** set. Then, the objective function in an ILP formulation can be described as:

$$\min D = \max_{i=1}^{M} \left(D(p_i) + \sum_{g_{ij} \in p_i} \Delta D(g_{ij}) \right) \tag{15}$$

where g_{ij} is the jth gate in path p_i, and $\Delta D(g_{ij})$ is the delay increase of gate g_{ij} due to the NBTI effect. In order to linearize the "max" operation, Equation (15) can be rewritten as:

$$\begin{aligned} &\min D \\ &s.t. \quad D \geq \left(D(p_i) + \sum_{g_{ij} \in p_i} \Delta D(g_{ij}) \right), \forall i \end{aligned} \tag{16}$$

The result of the ILP minimization in Equation (16) is the minimal postaging circuit delay as well as the input vector corresponding to the minimal circuit delay increase, which can be applied in standby mode.

3.1.2. ILP Formulation for Leakage Reduction

The ILP formulation for leakage reduction is similar to that for NBTI mitigation. The same linear constrain sets in Table 2 can be exploited to represent logic functionality of the circuit. Different from the path-based ILP formulation for NBTI mitigation, the objective function in the ILP formulation for leakage reduction is generated by accumulating all of the leakage powers of the gates. Firstly, the leakage power of each gate is described as a linear function of the variables, which represent the input state of the gate, as shown in Table 3.

Table 3. ILP objective function for leakage power of logic gates.

Gate	Objective Function
INV	$P = P_0 b + P_1 a$
NAND	$P = (2P_{00} + P_{11} - P_{01} - P_{10}) + (P_{10} - P_{01})a + (P_{01} - P_{00})b - (P_{00} + P_{11} - P_{01} - P_{10})c$
NOR	$P = (P_{01} + P_{10} - P_{11}) + (P_{11} - P_{01})a + (P_{11} - P_{10})b - (P_{01} + P_{10} - P_{00} - P_{11})c$

where P_{ab} is leakage power of the gate when the input signal value is ab. Then, we can sum all of the leakage powers of the gates and obtain the objective function in ILP formulation as follows:

$$\min P_{\text{lkg}} = \sum_{k=1}^{G} P_{\text{lkg}}(g_k) \tag{17}$$

where G is the total number of gates in the circuit.

3.2. Supply Voltage Assignment

In order to guarantee the circuit's performance, a supply voltage assignment is applied together with IVC to reduce NBTI-induced delay degradation. The basic idea of SVA is shown in Figure 3.

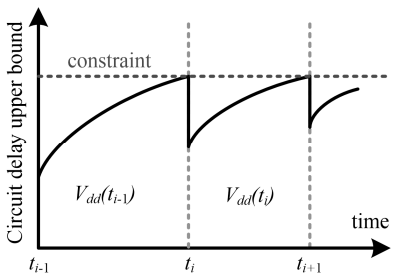


Figure 3. The basic principle of supply voltage assignment.

Figure 3 shows that, different from the guardband method, which selects a high voltage at the start of a circuit's lifetime, an SVA will increase the V_{dd} gradually to reduce the power dissipation and slow down the aging process. By estimating the delay degradation in different periods of a circuit's lifetime, the controller can determine whether the circuit has aged enough and the propagation delay has exceeded the allowed timing constrain, at which point the controller will increase V_{dd} to guarantee that no timing errors will occur. This procedure will repeat until the end of the circuit's lifetime.

3.3. Minimum NBTI Vector Selection Considering Power Effect

The SVA method can alleviate NBTI-induced delay degradation by increasing the supply voltage of the circuit. However, increasing V_{dd} will also result in the increase of dynamic power as well as static power. From Equation (9), we can find that there exists a quadratic relationship between dynamic power dissipation and supply voltage. In addition, the leakage power of the circuit will also increase exponentially with a supply voltage increase. Figure 4 illustrates the leakage power dissipation for an NAND2 gate under different combinations of input signal and supply voltage.

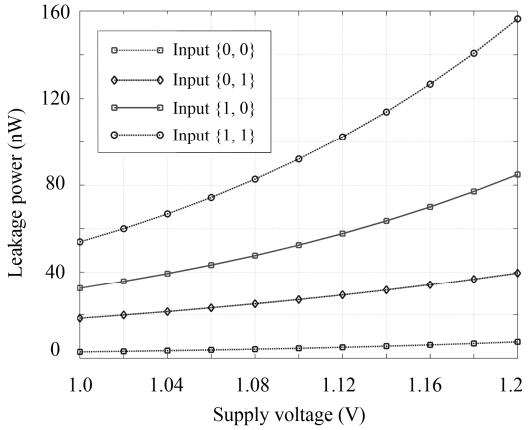


Figure 4. Leakage power change of an NAND gate under different supply voltage.

Figure 4 shows that the leakage power of the NAND gate will increase greatly when the supply voltage increases. Moreover, the high supply voltage will also accelerate the aging process of a pMOS transistor in the logic circuit. Using the PTM 65 nm model, we have obtained the relationship between the V_{th} change for a pMOS transistor and supply voltage ($V_{gs} = -V_{dd}$) in ten years by HSPICE simulation. The result is shown in Figure 5.

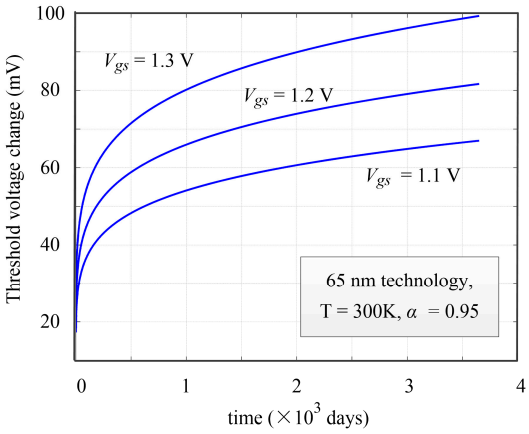


Figure 5. Threshold voltage change for a positive-channel Metal Oxide Semiconductor (pMOS) transistor with different V_{gs}.

Figures 4 and 5 show that although increasing V_{dd} can compensate for the NBTI-induced delay degradation, a high V_{dd} will also result in high power dissipation and a fast aging process. In order to slow down the V_{dd} adjustment speed for SVA, the circuit designer should find the input vector in standby mode which could reduce the NBTI effect on the circuit. In addition, the leakage power which corresponds to that input vector should also be controlled to be as low as possible when the V_{dd} is in the initial state, so that the total power dissipation during the circuit's lifetime will be reduced. Therefore, the input vector should park the circuit in a state which corresponds to the minimum NBTI effect, as well as the minimum leakage power. However, the impacts of the input vector on delay degradation and leakage power are not in a same direction; the optimal input vector for minimizing the postaging delay may not be the best one to minimize the leakage power and vice versa. Wang et al. proposed a probability-based (PB) method to find the best input vector that has the minimum NBTI effect and/or leakage for the circuit [33]. However, the PB method is based on heuristic and random simulations, so the computation cost is high and the result may not be the optimal. Firouzi et al. presented an IVC method based on LP to co-optimize the NBTI and leakage in standby mode [27]. They have specified the constrain of one issue and managed to find the minimum value for another issue. Their method is effective when using IVC alone, however, since IVC is often combined with other methods to further reduce NBTI and leakage, the approach to choosing the optimal input vector for the subsequent method has not been discussed in detail.

In this paper, we have proposed a simple form of co-optimization criterion function. First, we normalize the degradation and leakage to their potential minimum result obtained by ILP formulations for NBTI mitigation and leakage reduction only, respectively. Then, the sum of these two parts is minimized. It should be noted here that the ILP formulation for NBTI mitigation in Equation (16) is a path-based process, and the potential distribution range for postaging delay (the maximum propagation delay on all critical paths after aging) with different input vectors is smaller than the range for leakage power. So, if we build a co-optimization ILP formulation for postaging delay and leakage power minimization, the ILP solver will be biased to finding the input vector that can obtain the minimum leakage power, and the NBTI mitigation result will not be satisfactory. In order to solve this problem, the delay degradation is substituted for the postaging delay in the ILP formulation, and the ILP formulation for NBTI mitigation is modified as Equation (18):

$$\begin{aligned} &\min \Delta D \\ &s.t. \quad \Delta D \geq \left(D(p_i) + \sum_{g_{ij} \in p_i} \Delta D(g_{ij}) - D_0 \right), \forall i \end{aligned} \tag{18}$$

where D_0 is the maximum propagation delay on all paths in the initial state. Then, the co-optimization ILP formulation can be described as Equation (19):

$$E = \Delta D / \Delta D_{min} + P_{\text{leak}} / P_{\text{leak},min} \tag{19}$$

where ΔD is the delay degradation during the circuit lifetime, and P_{leak} is the leakage power. ΔD_{min} and $P_{\text{leak},min}$ are the results obtained by ILP formulation in Equations (18) and (17), respectively. Because ΔD is defined as difference between the largest original delay and the largest postaging delay in the entire path set, $\Delta D / \Delta D_{min}$ and $P_{\text{leak}} / P_{\text{leak},min}$ have the same order of magnitude. Then, we can obtain the global best input vector which can consider the NBTI effect and leakage power simultaneously, using the co-optimization ILP formulation in Equation (19). We name the ILP formulation for NBTI mitigation only, the ILP formulation for leakage reduction only, and our proposed co-optimization ILP formulation as IVC #1, IVC #2, and IVC #3, respectively, in the following section. In Figure 6, we compare the degradation and leakage reduction results of the above three IVC methods in ten years on c880 and c3540 circuits.

In Figure 6, the x-axis and y-axis represent ten years of NBTI-induced delay degradation and leakage power, respectively, for each input vector when the circuit uses that input vector in standby

mode. Point A (the rectangular point) and B (the triangle point) correspond to the result obtained by ILP formulation for NBTI mitigation and leakage reduction only, respectively. Point C (the asterisk point) represents the result of our proposed co-optimization method. The delay degradation and leakage power minimization results of the three ILP formulations are also compared with the results of Monte Carlo (MC) simulations. The iteration number for MC simulation is 100,000. We can see that compared with the MC simulation, the IVC #1 and IVC #2 methods can minimize the delay degradation and leakage power, respectively. However, the input vector obtained by the ILP formulation for a single effect cannot simultaneously reduce NBTI and leakage. When the degradation is minimized, the leakage is relatively high, and vice versa. In comparison, the input vector obtained by the proposed co-optimization ILP formulation can provide a balanced tradeoff between NBTI and leakage. Both specifications are near the potential optimal result, so it can then be combined with the SVA method to save more power during the circuit's lifetime. The effectiveness of our proposed IVC and SVA combination method will be discussed in the next section.

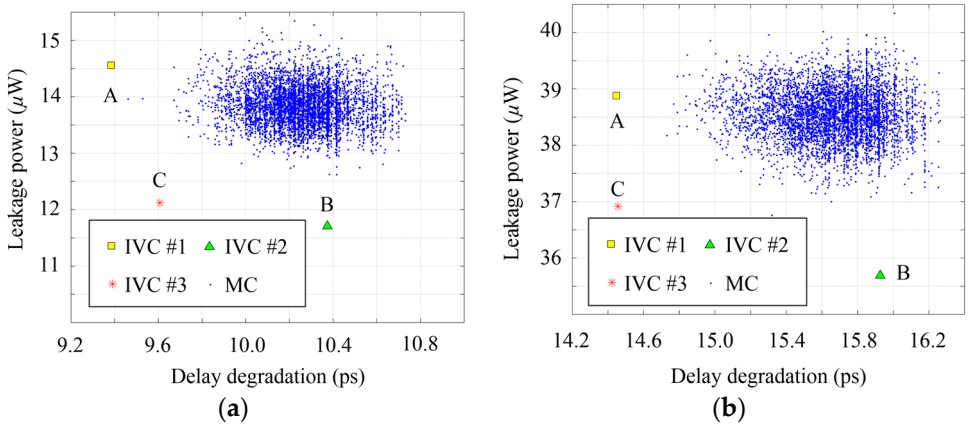


Figure 6. Degradation and leakage minimization result by different ILP formulations. (**a**) c880 circuit; (**b**) c3540 circuit.

4. Experiment and Discussion

4.1. Experimental Setting

The efficiency of the proposed IVC and SVA combination method is evaluated on selected ISCAS'85 and ISCAS'89 benchmark circuits. The circuits are synthesized by the Synopsys Design Compiler tool, and the synthesized netlists contain only INV, NAND, and NOR gates. The delay and power information of these basic gate cells is extracted by HSPICE simulation with the PTM 65 nm transistor model. Some key parameters are: $|V_{dd}| = 1.1$ V, $|V_{th}| = 0.18$ V for both nMOS and pMOS transistors, $T = 300$ K, $t_{ox} = 1.2$ nm, and T_{clk} in Equation (1) is 0.01 s. The circuit lifetime is set to be ten years. The timing constrains of each circuit are chosen as the postaging delay at a ten-day time node. According to Equations (1)–(6), the NBTI-induced delay degradation is dependent on many parameters. Therefore, the related parameters in calculating the timing constrain are set as follows: the duty cycle in active mode is set to be 0.95, as in the maximum dynamic stress (MDS) method [9]; the input vector in standby mode is selected using an ILP formulation for NBTI mitigation only; and the R_{AS} is set to be 1:9. By the above method, we can obtain the specific timing constrains for each circuit. In order to obtain the switching probability for each gate in Equation (9), which is necessary to calculate the dynamic power, we implement a 30,000 times logic simulation to generate different input patterns for the circuit and count to the number of switching activities for each gate to obtain the probability. The ILP problems are solved by LINGO 11.0 software [34]. All the experiments are implemented in C++ platform on a DELL T7500 workstation, with Intel Xeon E5620 2.4 GHz (two quad-core processors), 2 GB RAM, and the 64-bit operating system of Windows 7 Enterprise.

4.2. Result and Discusion

First, we compare the NBTI and leakage reduction results of different IVC methods. We define P_{leak} and P_{dyn} as the average leakage power and average dynamic power during the overall lifetime of the circuit, respectively. In the first step, three kinds of ILP formulations are constructed and their corresponding optimal input vectors are found. Then, the corresponding delay degradation ΔD and leakage power P_{leak} for these input vectors in ten years is calculated, and the result is shown in Table 4.

Table 4. NBTI and leakage reduction results using different kinds of ILP formulations.

Circuit	ΔD (ps)			P_{leak} (μW)		
	IVC #1	IVC #2	IVC #3	IVC #1	IVC #2	IVC #3
c432	10.68	11.85	10.8	6.24	5.69	5.90
c880	9.38	10.37	9.6	14.56	11.71	12.12
c1908	12.33	13.11	12.45	17.65	15.72	15.95
c2670	8.48	8.81	8.48	27.2	22.95	23.28
c3540	14.45	15.93	14.47	38.88	35.69	36.92
c5315	13.65	14.72	13.78	64.04	55.29	55.7
c7552	16.77	21.27	16.93	81.86	72.48	75.44
s5378	6.2	6.55	6.22	47.24	40.50	41.17
s9234	8.01	8.15	8.01	64.97	57.32	57.34
s13,207	12.01	12.83	12.03	100.84	82.66	83.19
Avg.	−0.69%	8.32%		13.15%	−2.01%	

The delay degradation ΔD that corresponds to the input vector obtained by the IVC #1, IVC #2, and IVC #3 methods is shown in column two to four, respectively. The corresponding leakage power P_{leak} of these three IVC methods is shown in column five to seven, respectively. From Table 4, we can obtain the following conclusions: first, IVC #1 and IVC #2 can find the optimal ΔD or P_{leak} minimization result, respectively. However, because only one issue is considered in generating the co-optimization ILP formulation, the reduction result for the other issue is not satisfactory. The proposed ILP formulation considers both effects, and can reduce ΔD and P_{leak} at the same time. For instance, compared with IVC #1, our proposed IVC #3 method can achieve a 13.15% improvement in P_{leak} reduction at the cost of a 0.69% ΔD increase on average. On the other hand, compared with IVC #2, our proposed method can decrease ΔD by 8.32% on average, at the cost of a 2.01% increase in leakage power.

As shown in Table 4, the results of the three ILP formulations are different tradeoffs between NBTI and leakage. In the following section, we combine these different IVC methods with the supply voltage assignment, which is a subsequent method after the input vector is determined. In most modern systems, the devices will periodically switch between the active and standby mode, and the circuit's delay degradation is dependent on the ratio between the active and standby modes (R_{AS}) according to Equations (1)–(6). In some industrial applications, the circuit works under a predefined routine, and the R_{AS} is a fixed value during its lifetime. However, the R_{AS} value in some other applications will change randomly. In order to simplify the experimental setting, we assume that the R_{AS} is fixed, and analyze the NBTI and power reduction results of the combination method when R_{AS} is set to different values. In our future work, we will further analyze the results of our proposed method when the R_{AS} changes randomly.

First, we use three kinds of ILP formulation IVC #1, IVC #2, and IVC #3 to determine the input vector that satisfies the NBTI minimization, leakage minimization, and co-optimization requirements, respectively. Then, the input vector is used in standby mode and the ratio between the active mode and the standby mode is assumed to be 0.1. Afterwards, an SVA method that uses the input vector obtained by IVC #1, IVC #2, and IVC #3, respectively, is applied to compensate for the NBTI-induced performance degradation. The V_{dd} update cycle for the SVA method is five days, and the resolution for V_{dd} adjustment is 20 mV. The above process is repeated until the end of the circuit's lifetime. Then, the average leakage and dynamic power of the circuit in ten years is calculated. The results are shown in Table 5.

In Table 5, the P_{leak} of SVA combined with IVC #1, IVC #2, and IVC #3 is shown in column two, four, and six, respectively. The P_{dyn} of SVA combined with these three IVC methods is shown in column three, five, and seven, respectively. Table 5 illustrates that, first, the P_{dyn} of the SVA + IVC #1 method is the lowest because its aging rate is less severe than that for the SVA + IVC #2 and SVA + IVC #3 methods, and the V_{dd} increase is the slowest. However, for most circuits, the P_{leak} of SVA is the highest when the input vector found by IVC #1 is used. This is because the P_{leak} that corresponds to the input vector obtained by IVC #1 is far higher than that corresponding to the other two ILP formulations when the circuit is in the initial state. Although the leakage power increase is the slowest for SVA + IVC #1, its total leakage power is still the highest at the end of the lifetime. Second, the P_{dyn} of SVA + IVC #2 is the highest because its corresponding input vector will bring in the most severe NBTI-induced aging, and in turn the frequency of V_{dd} adjustment is the highest. Third, our proposed co-optimization ILP formulation has considered both NBTI and leakage, and it can find the input vectors that help SVA save 13.82% and 2.49% more leakage power on average than IVC #1 and IVC #2, respectively. In addition, because the NBTI-induced delay degradation that corresponds to our proposed ILP formulation is near optimal, its corresponding P_{dyn} is close to the P_{dyn} of SVA + IVC #1 and is lower than the P_{dyn} when the input vector found by IVC #2 is used. Fourth, different from dynamic power, the analysis for the P_{leak} of the SVA method is a complex process when using different input vectors. For instance, in the c432 circuit, the input vector obtained by IVC #2 can help SVA save more leakage power than the input vector found by IVC #1. In contrast, the situation is the opposite for c7552 circuit. Figure 7 illustrates the change of the leakage power for the c432 and c7552 circuits at each 2-year time interval during the lifetime.

Table 5. Leakage and dynamic power of SVA combined with different ILP formulations (R_{AS} = 0.1).

Circuit	SVA + IVC #1 (μW)		SVA + IVC #2 (μW)		SVA + IVC #3 (μW)	
	P_{leak}	P_{dyn}	P_{leak}	P_{dyn}	P_{leak}	P_{dyn}
c432	9.24	17.86	8.06	18.28	7.95	17.90
c880	19.73	41.28	16.91	42.26	16.67	41.51
c1908	23.80	49.39	21.82	50.03	21.61	49.51
c2670	36.10	77.78	31.34	78.63	30.98	77.78
c3540	51.99	101.21	50.39	103.4	49.39	101.23
c5315	86.02	195.08	77.18	198.46	75.08	195.59
c7552	108.11	278.26	110.46	294.95	100.16	278.71
s5378	63.53	117.32	56.18	118.94	55.46	117.43
s9234	89.62	152.26	79.78	154.48	78.22	153.20
s13,207	138.88	204.41	117.46	207.18	115.67	204.49
Avg.	13.82%	−0.22%	2.49%	1.89%		

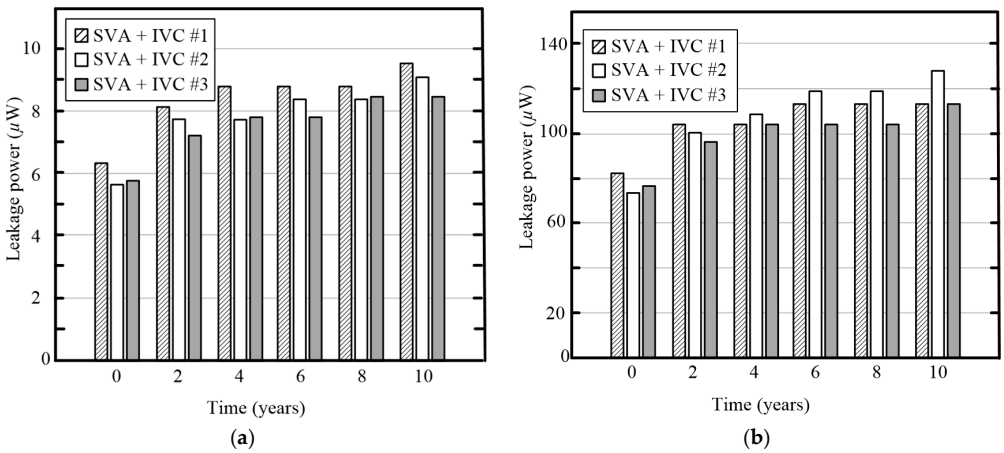


Figure 7. Leakage power dissipation of SVA with different input vectors for c432 and c7552 circuits. c432 circuit; (**b**) c7552 circuit.

The histograms in Figure 7 show that, for both circuits, the P_{leak} of SVA + IVC #2 and SVA + IVC #3 increase faster than that of SVA + IVC #1. However, for the c432 circuit, the leakage power in standby mode that corresponds to IVC #1 is much higher than that corresponding to the other two ILP formulations at the starting time (0 year), which makes it still the highest after some iterations of V_{dd} adjustment. Therefore, the P_{leak} of SVA + IVC #1 is higher than that of SVA combined with IVC #2 and IVC #3, as shown in Table 5. In contrast, although the initial leakage power that corresponds to the input vector found by IVC #2 is also the lowest for the c7552 circuit, the P_{leak} of SVA + IVC #2 is the highest for the c7552 circuit. The reason for this phenomenon is that the frequency of V_{dd} adjustment for SVA + IVC #2 is much faster than for SVA + IVC #1 and IVC #3 because of the severe delay degradation in standby mode, and makes its corresponding leakage power also increase fast as shown in Figure 7b. Finally, we can see that the input vector obtained by our proposed co-optimization ILP formulation can provide a balanced tradeoff between NBTI and leakage, so that both specifications are near optimal, and it can help the SVA save more leakage power than the ILP formulation for a single effect.

Moreover, we have analyzed the power dissipation of the SVA method when R_{AS} is 0.01 and 1.0, and the results are shown in Tables 6 and 7, respectively.

Table 6. Leakage and dynamic power of SVA combined with different ILP formulations (R_{AS} = 0.01).

Circuit	SVA + IVC #1 (μW)		SVA + IVC #2 (μW)		SVA + IVC #3 (μW)	
	P_{leak}	P_{dyn}	P_{leak}	P_{dyn}	P_{leak}	P_{dyn}
c432	8.52	17.26	7.65	17.89	7.38	17.34
c880	17.87	39.61	15.70	41.00	15.26	39.99
c1908	21.96	47.77	20.38	48.63	19.92	47.85
c2670	33.42	75.29	29.16	76.30	28.67	75.29
c3540	47.73	97.61	47.13	100.59	45.33	97.62
c5315	78.50	187.71	71.68	192.41	68.39	188.02
c7552	97.77	266.61	104.12	287.98	90.81	267.39
s5378	58.49	113.37	52.63	115.76	51.17	113.57
s9234	82.45	147.05	74.47	150.14	72.26	148.23
s13,207	127.09	197.03	109.01	200.94	105.96	197.17
Avg.	13.54%	−0.31%	4.28%	2.69%		

Table 7. Leakage and dynamic power of SVA combined with different ILP formulations (R_{AS} = 1.0).

Circuit	SVA + IVC #1 (μW)		SVA + IVC #2 (μW)		SVA + IVC #3 (μW)	
	P_{leak}	P_{dyn}	P_{leak}	P_{dyn}	P_{leak}	P_{dyn}
c432	10.18	18.58	8.58	18.77	8.70	18.60
c880	22.11	43.25	18.50	43.79	18.58	43.38
c1908	26.33	51.46	23.64	51.70	23.82	51.51
c2670	40.06	81.20	34.20	81.48	34.43	81.20
c3540	57.74	105.82	54.53	106.89	55.04	105.84
c5315	96.15	204.45	84.63	206.35	83.45	204.61
c7552	125.18	295.82	118.91	304.07	115.96	296.16
s5378	70.15	122.12	60.67	122.71	61.12	122.16
s9234	99.57	159.15	86.57	159.90	86.01	159.45
s13,207	153.49	213.15	128.55	215.10	127.77	213.20
Avg.	14.16%	−0.10%	0.03%	0.87%		

Tables 5–7 show that the power reduction result of the SVA method is dependent on both the input vector in standby mode and the R_{AS} value. First, compared with the SVA + IVC #1 method, our proposed SVA + IVC #3 method can save more leakage power, at the cost of a small increase of dynamic power. Second, when R_{AS} decreases, the advantage of our proposed SVA + IVC #3 method over the SVA + IVC #2 method on power reduction becomes high. For example, when R_{AS} is 0.01, the SVA +

IVC #3 method can save 4.28% more leakage power on average than that of SVA + IVC #2. However, when the R_{AS} is 1.0, our proposed method can only save 0.03% more leakage power. The reason for this phenomenon is that when the R_{AS} is small, the ratio of standby mode in the whole lifetime becomes high; the advantage of the input vector found by IVC #1 and IVC #3 on NBTI mitigation becomes more distinct over the input vector obtained by IVC #2. Therefore, the frequency of V_{dd} adjustment for the SVA method when using the input vector found by IVC #3 is much slower than that of IVC #2, which in turn helps the SVA + IVC #3 method save more leakage and dynamic power than that of the SVA + IVC #2 method.

In Ref. [27], Firouzi et al. have proposed a kind of co-optimization method for NBTI and leakage reduction. This co-optimization ILP formulation is named IVC #4 in the following section. Their method constructed an ILP formulation to find the minimum NBTI-induced delay degradation with different power constraints. In this paper, we also use IVC #4 to find the input vector and analyze the power reduction result of the SVA method when using these input vectors. First, the ILP formulation for leakage minimization and the modified version of ILP formulation for leakage maximization are generated as per the design flow in Ref. [27]. Then, we find the potential best and worst leakage power for the circuit by solving these formulations. Second, a set of power constrains can be built with 10% steps of the leakage power compared to the potential minimum value. With each constrain, an ILP formulation for NBTI mitigation is generated, and the result of these ILP formulations are input vectors, which can obtain the minimum NBTI-induced aging and satisfy the leakage power constrain. Finally, we use each of these ten input vectors in standby mode and apply an SVA to compensate for the performance aging. At the end of the circuit's lifetime, we calculate the average leakage and dynamic power of an SVA when using each input vector. Suppose $P_{\text{leak},i}$ and $P_{\text{dyn},i}$ is the leakage and dynamic power of an SVA corresponding to input vector i. $P_{\text{leak},min}$ and $P_{\text{dyn},min}$ is the potential minimum leakage and dynamic power for all of the ten input vectors. Then we define $E_i = P_{\text{leak},i}/P_{\text{leak},min} + P_{\text{dyn},i}/P_{\text{dyn},min}$ for each input vector i, and the minimum E_i is considered as the optimal result on power reduction for each circuit when using IVC #4. The leakage and dynamic power of the SVA method when using the input vector found by IVC #4 and our proposed IVC #3 method is shown in Table 8.

Table 8. Leakage and dynamic power of SVA method using input vector found by Ref. [27] and the proposed ILP formulation.

Circuit	SVA + IVC #4 in Ref. [27]		the proposed SVA + IVC #3	
	P_{leak} (μW)	P_{dyn} (μW)	P_{leak} (μW)	P_{dyn} (μW)
c432	7.95	17.90	7.95	17.90
c880	16.91	41.51	16.67	41.51
c1908	21.65	49.51	21.61	49.51
c2670	31.49	77.78	30.98	77.78
c3540	49.92	101.73	49.39	101.23
c5315	76.19	195.38	75.08	195.59
c7552	100.21	278.69	100.16	278.71
s5378	56.17	117.32	55.46	117.43
s9234	80.48	153.20	78.22	153.20
s13,207	117.51	204.41	115.67	204.49
Avg.	1.16%	0.02%		

From Table 8, we can see that compared with the IVC #4 method, our proposed method can save more leakage power dissipation during a circuit's lifetime, at the cost of a slight increase in dynamic power. Moreover, the design procedure of our proposed method is much simpler than that in Ref. [27], which demonstrates the advantage of our method.

In addition, we implement a simulation on c880 and c3540 circuits to investigate the leakage and dynamic power change of the SVA method when using the input vector obtained by IVC #4 under

different power constrains in detail. In order to observe the change more precisely, the leakage and dynamic power results of SVA + IVC #4 are normalized to the power results obtained by the proposed SVA + IVC #3 method. The results are shown in Figure 8.

In Figure 8, the x-axis represents the different power constrains for the ILP formulation in Ref. [27], and the y-axis is the ratio of P_{dyn} and P_{leak} between the SVA + IVC #3 method and the SVA + IVC #4 method. Figure 8 shows that, for the different circuits, the co-optimization ILP formulations with different power constrains can obtain the optimal leakage and dynamic power reduction result. For example, the power reduction result is optimal for an c880 circuit when the constrain is 30%. However, for the c3540 circuit, the optimal result can be obtained when the constrain is set to 10%. Therefore, it is inconvenient to find the best parameter for the co-optimization ILP formulation in Ref. [27]. In comparison, our proposed ILP formulation can obtain the only optimal input vector that can help the SVA method save power dissipation conveniently.

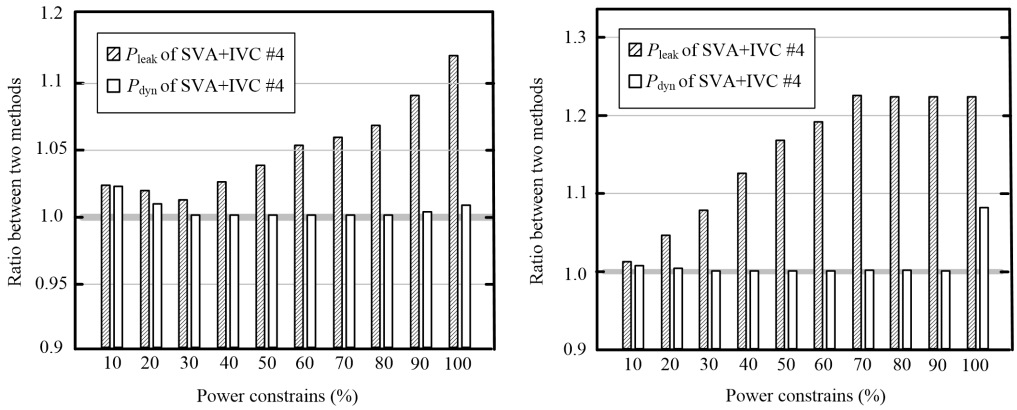


Figure 8. Leakage and dynamic power of SVA for the c880 and c3540 circuits when using the input vector obtained by the co-optimization method in Ref. [27] under different power constrain settings. (**a**) c880 circuit; (**b**) c3540 circuit.

Finally, we implement a 5000 times Monte Carlo simulation to find input vectors for the circuit. We calculate the P_{leak} and P_{dyn} of the SVA in ten years when these randomly selected input vectors are used in standby mode. The simulation setting is the same as the above section. We compare the power dissipation of SVA + MC with our proposed SVA + IVC #3 method. The result is shown in Table 9.

Table 9. Leakage and dynamic power of SVA using an input vector found by Monte Carlo (MC) simulation and the IVC #3 method.

Circuit	SVA + MC (μW)		SVA + IVC #3	
	P_{leak} (μW)	P_{dyn} (μW)	P_{leak} (μW)	P_{dyn} (μW)
c432	8.37	17.93	7.95	17.90
c880	18.21	41.55	16.67	41.51
c1908	22.67	49.79	21.61	49.51
c2670	32.76	76.67	30.98	77.78
c3540	51.93	102.13	49.39	101.23
c5315	83.11	196.66	75.08	195.59
c7552	102.21	273.18	100.16	278.71
s5378	58.82	115.74	55.46	117.43
s9234	87.18	153.23	78.22	153.20
s13207	129.53	205.18	115.67	204.49
Avg.	7.26%	−0.22%		

Table 9 shows that the proposed IVC #3 method can find the optimal input vector and help the SVA save more leakage power than the input vector obtained by MC simulation. Since the dynamic power

is strongly dependent on the circuit's supply voltage in the active mode, the impact of NBTI-induced V_{dd} change on power dissipation is great. As shown in Figure 6, the result of NBTI mitigation by MC simulation is close or even better than the result by the proposed IVC #3 method, so the best result of the dynamic power for SVA + MC is close to the dynamic power of the SVA + IVC #3 method. Finally, the P_{dyn} and P_{leak} of the SVA method for the c880 and c3540 circuits when using the input vector obtained by MC and the three IVC methods are illustrated in Figure 9, respectively.

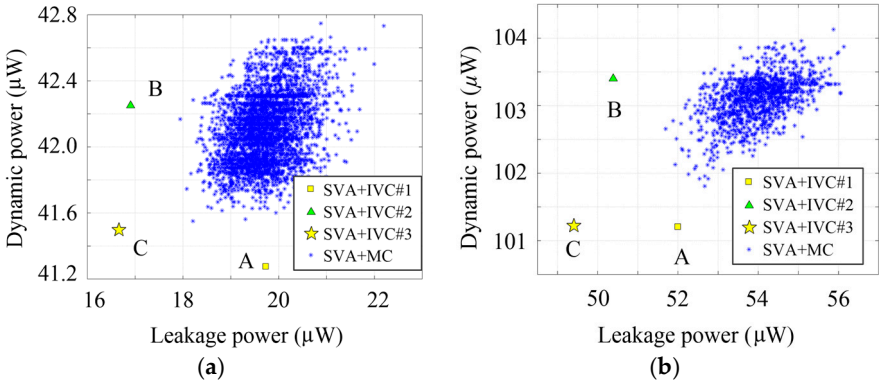


Figure 9. Leakage and dynamic power of SVA for c880 and c3540 circuits when using the input vector obtained by MC simulation and our proposed IVC #3 method. (**a**) c880 circuit; (**b**) c3540 circuit.

In Figure 9, the x-axis and y-axis represent the leakage and dynamic power of the SVA method, respectively. Point A (the rectangular point) and B (the triangle point) correspond to the result of SVA + IVC #1 and SVA + IVC #2, respectively. Point C (the star point) represents the result of our proposed SVA + IVC #3 method. The small asterisk point represents the leakage and dynamic power of the SVA method using the input vector obtained by MC simulations. The iteration number for MC simulation is 100,000. From Figure 9, we can get the following conclusions: first, the dynamic power of SVA when using the input vector obtained by IVC #1 is the lowest, because the ILP formulation for NBTI reduction can find the minimum degradation vector (MDV), and the frequency of V_{dd} adjustment for SVA + IVC #1 is the slowest. However, because the initial leakage power that corresponds to IVC #1 is the highest, the total leakage power dissipation for SVA + IVC #1 is the highest among the three ILP formulations. Second, although the leakage power dissipation for SVA + IVC #2 is low, its dynamic power is relatively high because of the high V_{dd} adjustment frequency. Finally, the P_{dyn} and P_{leak} of our proposed SVA + IVC #3 method are all near the optimal result, which demonstrates its advantage over MC simulation and ILP formulations for a single effect.

5. Conclusions

In this paper, an IVC and SVA combination method is proposed to reduce NBTI and leakage simultaneously. First, the dependence of NBTI and leakage on input vectors is analyzed and the procedure for a delay degradation and leakage power reduction technique based on the ILP approach is described. Based on this, a minimum NBTI vector selection method is proposed, which considers the power effect. Our proposed ILP formulation can be generated automatically and the parameters in the objective function can be adjusted adaptively for different circuits, so that the circuit designers can find the optimal input vector conveniently. In addition, we combine our proposed IVC method with the supply voltage assignment technique, and compare the average power dissipation of SVA when using different input vectors in standby mode. The experimental results on ten benchmark circuits show that, compared with MC simulation and the other kinds of ILP formulations, our proposed method can balance the tradeoff between NBTI and leakage, and it can help SVA reduce more power dissipation and guarantee the circuit's performance simultaneously.

Acknowledgments: This work was supported by the National Natural Science Foundation of China (Nos. 61201015, 61102036, 61571161).

Author Contributions: Peng Sun conceived and designed the experiments; Yang Yu performed the experiments; Junbao Li analyzed the data; and Peng Sun, Zhiming Yang, and Xiyuan Peng wrote the paper. This work was supported by the National Natural Science Foundation of China (Nos. 61201015, 61102036, 61571161).

Conflicts of Interest: The authors declare no conflict of interest.

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