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Article

Work Function Adjustment by Using Dipole Engineering for TaN-Al_2O_3-Si_3N_4-$HfSiO_x$-Silicon Nonvolatile Memory

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Abstract: This paper presents a novel TaN-Al_2O_3-$HfSiO_x$-SiO_2-silicon (TAHOS) nonvolatile memory (NVM) design with dipole engineering at the $HfSiO_x$/SiO_2 interface. The threshold voltage shift achieved by using dipole engineering could enable work function adjustment for NVM devices. The dipole layer at the tunnel oxide–charge storage layer interface increases the programming speed and provides satisfactory retention. This NVM device has a high program/erase (P/E) speed; a 2-V memory window can be achieved by applying 16 V for 10 μs. Regarding high-temperature retention characteristics, 62% of the initial memory window was maintained after 10^3 P/E-cycle stress in a 10-year simulation. This paper discusses the performance improvement enabled by using dipole layer engineering in the TAHOS NVM.

Keywords: TaN-Al_2O_3-HfSiOx-SiO_2-Silicon (TAHOS); nonvolatile memory (NVM); dipole engineering; work function

1. Introduction

Nonvolatile memory (NVM), because of its high density and low cost, is widely used for portable mass storage purposes in digital cameras, tablet PCs, and smartphones [1]. A crucial challenge in the electronics industry is obtaining low-power fast NVM devices with small dimensions. A silicon-oxide-nitride-oxide-silicon (SONOS)-like structure has become widely used for charging

devices because it does not have a planar scaling problem for floating gate isolation and exhibits considerable potential for achieving high program/erase (P/E) speeds, low programming voltages, and low power performance [1–7].

Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) flash memory devices are potential candidates for replacing conventional floating-gate NAND (Not AND) flash devices in the sub-32 nm technology node [6,7]. SONOS-like devices have several advantages over the conventional floating-gate device, such as rapid programming, low-power operation, high-density integration, and excellent reliability.

According to studies on SONOS flash, TaN-Al_2O_3-Si_3N_4-SiO_2-silicon (TANOS) structure flash memory [8–10] exhibits excellent performance because of its immunity to gate injection when metal gate TaN with a high work function is used. Moreover, several studies have presented various types of high-*k* dielectric trapping layers as potential candidates for replacing Si_3N_4 to provide discrete NVM charge storage [11–16]. Furthermore, high-*k* dielectric materials can improve the gate capacitance, and maintain an equivalent potential difference for a greater thickness compared with SiO_2. Therefore, the leakage through the dielectric can be minimized, and the scaling limits can be extended. Moreover, to achieve a large memory window for differentiating between stable programs and erased states, a high-*k* dielectric trapping layer can provide sufficiently high trapping density for charge storage [17]. According to the International Technology Roadmap for Semiconductors, high-*k* trapping layer use in flash memory has high potential for scalability below the 32-nm node [18].

Metal gate electrodes with high-*k* dielectric oxide may be made more effective than poly-Si by improving the carrier mobility, thus avoiding the poly-Si depletion effect and dopant penetration through the gate oxide [19–22]. However, using a metal gate layer requires *n*- and *p*-type metals with appropriate work functions for targeting the suitable threshold voltage (V_{th}) for high-performance complementary metal-oxide-semiconductor (CMOS) logic applications on bulk Si [23,24]. In addition, studies have demonstrated V_{th} shift caused by dipole formation at high-*k*/SiO_2 interfaces [25–27]. The areal density difference of oxygen atoms is the driving force in dipole formation at these interfaces [28,29]. In this study, we used the dipole engineering for NVM to modulate V_{th} with different high-*k* dielectric layers. The proposed design with adjustable V_{th} exhibited excellent characteristics such as a considerably large memory window, high-speed P/E, excellent endurance, and optimal disturbance.

2. Experimental Section

Figure 1 illustrates the structure of our TAHOS SONOS-like NVMs. These devices were fabricated on 6 inch Si wafers. After the active region was patterned, a 4 nm oxide tunnel was thermally grown at 1000 °C in a vertical furnace system. Next, 1 nm HfO_2 and Al_2O_3 thin films, used in the dipole layer, were deposited using metal–organic chemical vapor deposition (MOCVD). We compared three samples: one without a dipole layer, one with a 1 nm HfO_2 dipole layer, and one with a 1 nm Al_2O_3 dipole layer. Table 1 compares the devices. After a 10 nm trapping $HfSiO_x$ deposition, MOCVD was used to deposit a 10 nm Al_2O_3 thin film, which was used as a blocking oxide. Next, a 100 nm TaN layer was deposited using a sputtering method. After gate patterning, a self-aligned implantation was used to create an n^+ source/drain with As^+ at a dose of 5×10^{15} cm^{-2} and energy of 15 keV. Dopant activation and the interaction of the dipole layer with tunnel oxide were accomplished through rapid thermal annealing (RTA) at 950 °C for

15 s. The remainder of the subsequent standard CMOS procedures were completed for fabricating the TAHOS SONOS-like NVM devices.

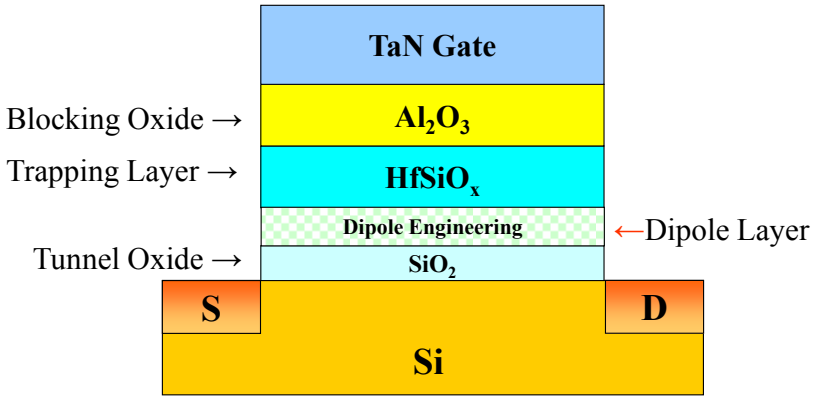

Figure 1. Cross-sectional cell structure of the TAHOS NVM device using dipole engineering.

Table 1. Dipole engineering for TAHOS NVM devices.

Dipole engineering	w/o Dipole	w/i Dipole Al_2O_3	w/i Dipole HfO_2
Tunneling oxide	SiO_2 40 Å	SiO_2 40 Å	SiO_2 40 Å
Dipole layer	–	Al_2O_3 10 Å	HfO_2 10 Å
Trapping layer	$HfSiO_x$ 100 Å	$HfSiO_x$ 100 Å	$HfSiO_x$ 100 Å
Blocking oxide	Al_2O_3 100 Å	Al_2O_3 100 Å	Al_2O_3 100 Å

3. Results and Discussion

Figure 2 plots the I_d-V_g curve of the proposed TAHOS NVM devices. The drain voltage (V_d) of the I_d-V_g curve is 0.1 V, and V_g transverses from 0 to 5 V. The V_{th} at 10^{-7} A I_d is 1.68, 2.11, and 1.82 V for the without dipole, Al_2O_3 dipole, and HfO_2 dipole samples, respectively. Al_2O_3/HfO_2 dipole layer incorporation in the TAHOS stacks results in a positive V_{th} shift in the NVM devices. The V_{th} tuning was found to be proportional to the net dipole moment associated with the Hf-O/Si-O and Al-O/Si-O bonds at the high-*k*/SiO_2 interface because of electronegativity and areal density difference of oxygen atoms [28,29]. According to the electrical measurement results, the dipole effects caused by the interfacial Al_2O_3 and HfO_2 dipole layer shift the effective work function toward p-metal. Therefore, different dipole layers can be used for V_{th} adjustment for tuning the conventional gate electrode work function.

X-ray photoelectron spectroscopy (XPS) was performed by using an Al Kα X-ray source (1486.6-eV photons) to determine the bonding environments of the Hf atoms. Figure 3 shows the Hf 4f photoemission peaks of the samples without dipole, with Al_2O_3 dipole, and with HfO_2 dipole. The test sample for XPS was prepared for the without dipole or with Al_2O_3 dipole layer following preparation of the $HfSiO_x$ thin film after RTA at 950 °C for 15 s. In the without dipole sample, we observed well-defined $4f_{5/2}$ and $4f_{7/2}$ feature peaks for the $HfSiO_x$ thin film that correspond to Hf–O–Si bonding. For the HfO_2 dipole sample, these peaks shifted to lower binding energies ($4f_{5/2}$: *ca.* 17.7 eV; $4f_{7/2}$: *ca.* 16.2 eV), resulting in HfO_2 dipole formation after RTA [30]. Moreover, for the Al_2O_3 dipole sample, these peaks shifted to higher binding energies ($4f_{5/2}$: *ca.* 18.7 eV; $4f_{7/2}$: *ca.* 17.2 eV), resulting in Al_2O_3

dipole formation after RTA [31]. The XPS results provide definite evidence of HfO_2 and Al_2O_3 dipole formation through dipole engineering.

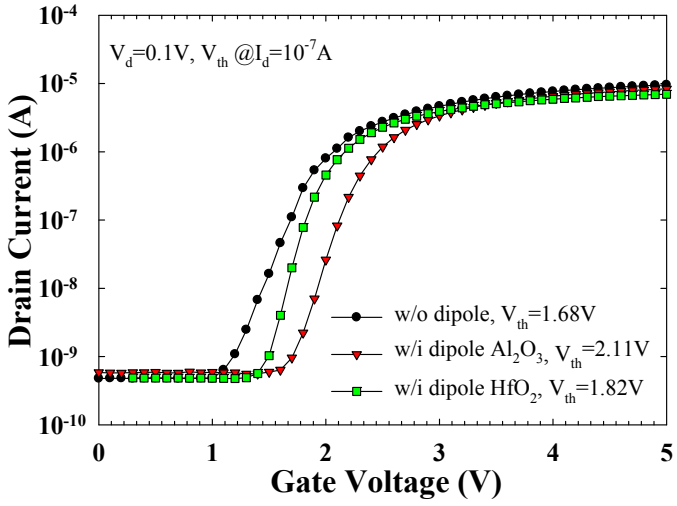

Figure 2. I_d–V_g curve of the TAHOS NVM devices.

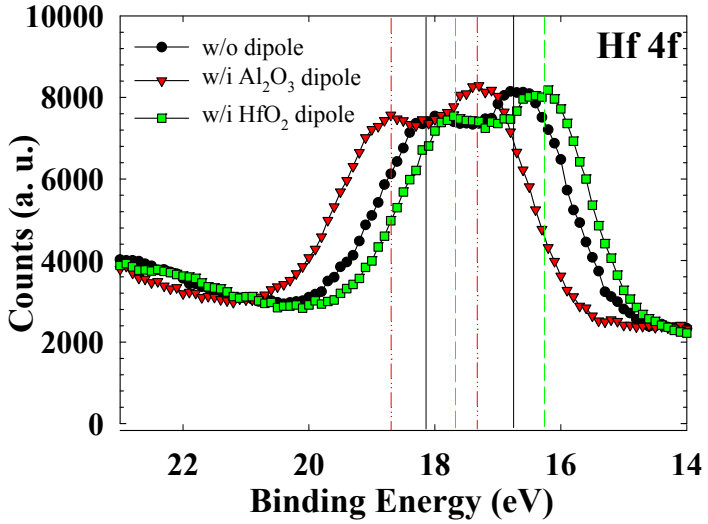

Figure 3. Hf 4f XPS spectra of the samples without dipole, with Al_2O_3 dipole, and with HfO_2 dipole.

Figure 4a,b presents the P/E characteristics of various pulse widths for different operation conditions. The P/E operations were performed using Fowler–Nordheim tunneling at V_g = 16 V and V_g = −15 V with V_d = V_s = 0 V. The V_{th} shift is defined as the threshold voltage change of a device between the written and the erased states. ΔV_{th} increased with the P/E pulse time and bias, and the memory window was >1.5 V. In conventional flash memory, >0.8 V memory window is sufficient for judge the "1" or "0" state, the V_{th} window of the device between program/erase state is enough for flash memory operation. No erase saturation effect occurred even at high erase bias or over a long erase time because of TaN's high work function (4.7 eV), which prevents the injection of electrons from the gate [10]. Regarding the dipole splits, the Al_2O_3 and HfO_2 dipole samples have higher programming speeds than does the without dipole sample because of the low barrier height for electron tunneling. The Al_2O_3 or HfO_2 dipole samples have slightly lower erasing speeds because of the increasing thickness of gate oxide.

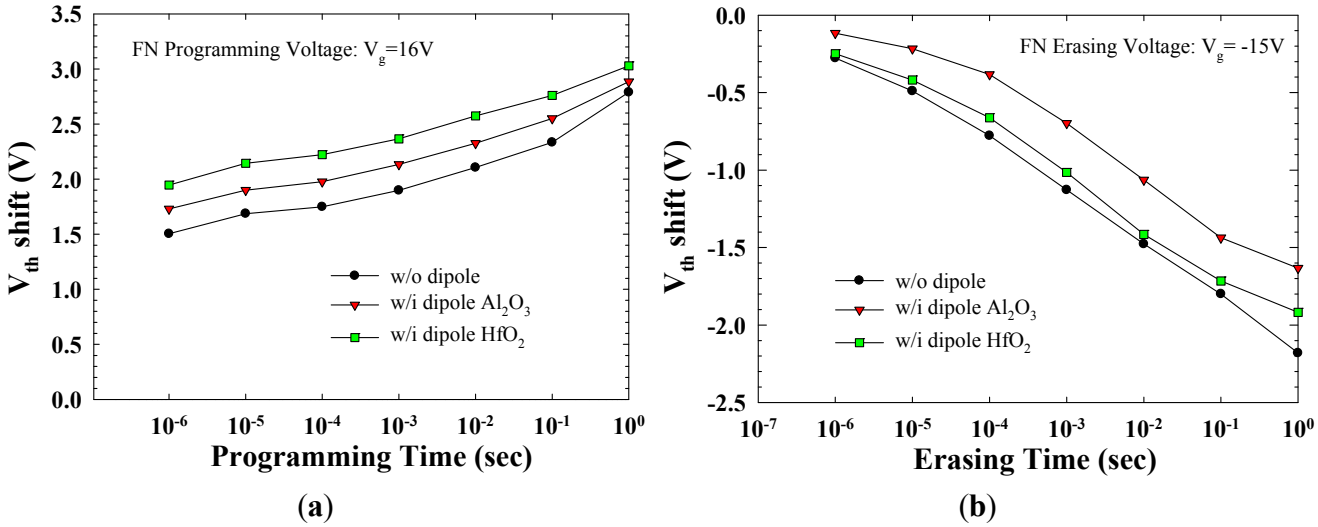

Figure 4. (**a**) Program characteristics of the TAHOS NVM devices; (**b**) Erase characteristics of the TAHOS NVM devices.

Figure 5 plots the endurance characteristic of the proposed TAHOS NVM devices. To achieve approximately the same memory window, we used the following P/E conditions: V_g = 16 V, 1 us/V_g = −15 V, and 0.1 s for the without dipole sample; V_g = 16 V, 1 us/V_g = 16 V, and 0.1 s for the Al_2O_3 dipole sample; and V_g = 16 V, 1 us/V_g = −16 V, and 0.1 s for the HfO_2 dipole sample. The NVM device displayed more favorable endurance, retaining 75% of its initial memory window after 10^3 P/E cycles. For the endurance characteristics, higher erasing V_t after cycling is the reliability issue in the conventional flash memory for thick tunnel oxide degradation [2,6,8]. This result is because the degradation of the tunnel oxide (SiO_2) in TAHOS NVM devices mainly depends on the electrical field. In addition, the endurance curves increase slightly as the number of P/E cycles increase, because of the formation of operation-induced trapped electrons. This is intimately related to the use of thick tunnel oxide and presence of minute residual charges in the SiO_2 after cycling.

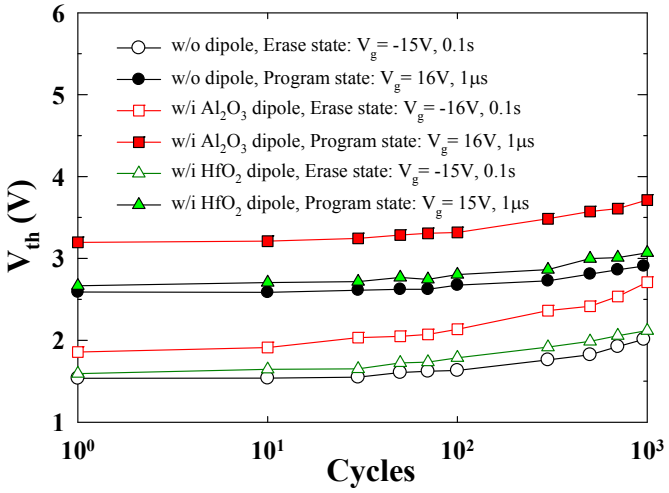

Figure 5. Endurance characteristics of the TAHOS NVM devices.

Figure 6 illustrates the retention characteristics with 10^3 P/E cycled stress condition of the proposed TAHOS NVM at a high temperature (T = 85 °C). The retention time was up to 10^8 s for 38%, 48%, and

72% charge losses for the Al_2O_3 dipole, HfO_2 dipole, and without dipole samples, respectively. The retention of both of the dipole samples was superior to that of the without dipole sample because of the formation of a thick tunnel oxide. Moreover, the Al_2O_3 dipole sample exhibited superior retention to that of the HfO_2 dipole sample because the Al_2O_3 layer has a greater electron barrier height [31].

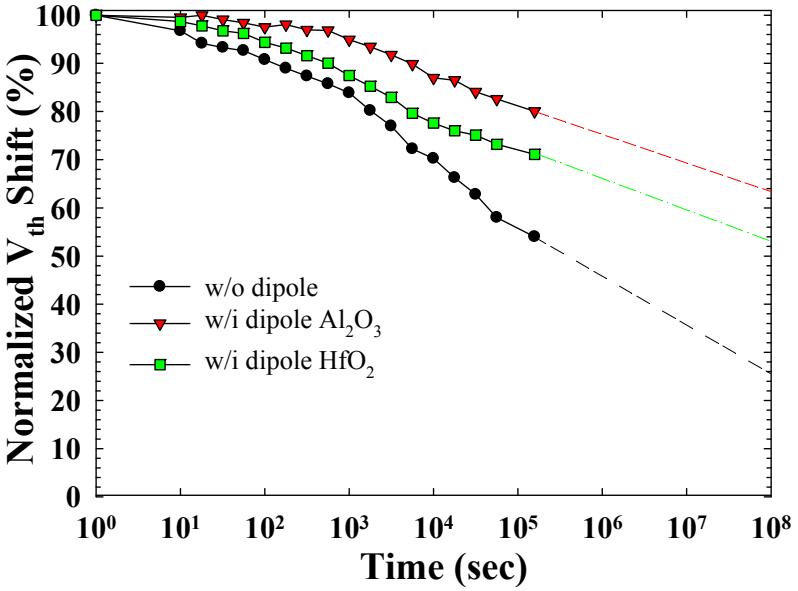

Figure 6. Retention characteristics of the TAHOS NVM devices.

4. Conclusions

TAHOS NVM was fabricated using an Al_2O_3/HfO_2 dipole layer at an $HfSiO_x/SiO_2$ interface, demonstrating a V_{th} shift and providing work function adjustment. A 2-V memory window was achieved by applying 15 V for only 10 μs. Regarding endurance, a 1-V of memory window was maintained after 10^3 P/E stress cycles. Regarding retention, 62% of the initial memory window was maintained after a 10-year simulation at high temperature (T = 85 °C). Thus, dipole engineering has great potential for work function adjustment in conventional SONOS-type NVM.

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Author Contributions

Yu-Hsien Lin organized the research and wrote the manuscript; Yi-Yun Yang performed the experiments and performed data analysis; Yu-Hsien Lin and Yi-Yun Yang discussed the experiments and the manuscript.

Conflicts of Interest

The authors declare no conflict of interest.

References

1. Li, Y.; Quader, K.N. NAND Flash Memory: Challenges and Opportunities. *Computer* **2013**, *46*, 23–29.
2. Lin, Y.H.; Chien, C.H. Nanoscale 2-bit/cell HfO_2 Nanocrystal Flash Memory. *IEEE Trans. Nanotechnol.* **2012**, *11*, 412–417.
3. Wu, C.C.; Yang, W.L.; Chang, Y.M.; Liu, S.H.; Hsiao, Y.P. Plasma-Enhanced Storage Capability of SONOS Flash Memory. *Int. J. Electrochem. Sci.* **2013**, *8*, 6678–6685.
4. Hung, M.F.; Wu, Y.C.; Tang, Z.Y. High Performance Gate-All-Around Poly-Si Nanowire with Si Nanocrystals Nonvolatile Memory. *Appl. Phys. Lett.* **2011**, *98*, 162108.
5. Chen, L.C.; Wu, Y.C.; Lin, T.C.; Huang, J.Y.; Hung, M.F.; Chen, J.H.; Chang, C.Y. Poly-Si Nanowire Nonvolatile Memory with Nanocrystal Indium-Gallium-Zinc-Oxide Charge-Trapping Layer. *IEEE Electron. Device Lett.* **2010**, *31*, 1407–1409.
6. Lin, Y.H.; Chien, C.H. HfO_2 Nanocrystal Memory on SiGe Channel. *Solid State Electron*. **2013**, *80*, 5–9.
7. Zhao, C.; Zhao, C.Z.; Taylor, S.; Chalker, P.R. Review on Non-Volatile Memory with High-*k* Dielectrics: Flash for Generation Beyond 32 nm. *Materials* **2014**, *7*, 5117–5145.
8. Lin, Y.H.; Wu, Y.C.; Hung, M.F.; Chen, J.H. Charge Storage Characteristics of Pi-Gate Poly-Si Nanowires TaN-Al_2O_3-Si_3N_4-SiO_2-Si Flash Memory. *Int. J. Electrochem. Sci.* **2012**, *7*, 8648.
9. Beug, M.F.; Melde, T.; Czernohorsky, M.; Hoffmann, R.; Paul, J.; Knoefler, R.; Tilke, A.T. Analysis of TANOS memory cells with sealing Oxide Containing Blocking Dielectric. *IEEE Trans. Electron Devices* **2010**, *57*, 1590–1596.
10. Lee, C.H.; Choi, K.I.; Cho, M.K.; Song, Y.H.; Park, K.C.; Kim, K. A Novel SONOS Structure of SiO_2/SiN/Al_2O_3 with TaN Metal Gate for Multi-Giga Bit Flash Memories. In Proceedings of the IEEE International Electron Devices Meeting, Washington, DC, USA, 8–10 December 2003; pp. 26.5.1–26.5.4.
11. Kittl, J.A.; Opsomer, K.; Popovici, M.; Menou, N.; Kaczer, B.; Wang, X.P.; Adelmann, C.; Pawlak, M.A.; Tomida, K.; Rothschild, A.; *et al.* High-*k* dielectrics for future generation memory devices. *Microelectron. Eng.* **2009**, *86*, 1789–1795.
12. Chen, F.H.; Pan, T.M.; Chiu, F.C. Metal-Oxide-High-k-Oxide-Silicon Memory Device Using a Ti-Doped Dy_2O_3 Charge-Trapping Layer and Al_2O_3 Blocking Layer. *IEEE Trans. Electron Devices* **2011**, *58*, 3847–3851.
13. Liu, S.H.; Wu, C.C.; Yang, W.L.; Lin, Y.H.; Chao, T.S. Ion-Bombarded and Plasma-Passivated Charge Storage Layer for SONOS-Type Nonvolatile Memory. *IEEE Trans. Electron Devices* **2014**, *61*, 3179–3185.
14. Breuil, L.; Lisoni, J.G.; Blomme, P.; van den bosch, G.; van Houdt, J. HfO_2 Based High-*k* Inter-Gate Dielectrics for Planar NAND Flash Memory. *IEEE Electron Device Lett.* **2013**, *35*, 45–47.

15. Pavunny, S.P.; Scott, J.F.; Katiyar, R.S. Lanthanum Gadolinium Oxide: A New Electronic Device Material for CMOS Logic and Memory Devices. *Materials* **2014**, *7*, 2669–2696.
16. Chiang, T.Y.; Wu, Y.H.; Ma, W.C.Y.; Kuo, P.Y.; Wang, K.T.; Liao, C.C.; Yeh, C.R.; Yang, W.L.; Chao, T.S. Characteristics of SONOS-Type Flash Memory with *in Situ* Embedded Silicon Nanocrystals. *IEEE Trans. Electron Devices* **2010**, *57*, 1895–1902.
17. Clark, R.D. Emerging Applications for High K Materials in VLSI Technology. *Materials* **2014**, *7*, 2913–2944.
18. The International Technology Roadmap for Semiconductors (ITRS). Available online: http://www.itrs.net/ (accessed on 8 April 2014).
19. Collaert, N.; Demand, M.; Ferain, I.; Lisoni, J.; Singanamallan, R.; Zimmerman, P.; Yim, Y.S.; Schram, T.; Mannaert, G.; Goodwin, M.; *et al.* Tall Triple-Gate Devices with TiN/HfO_2 Gate Stack. In Proceedings of the Symposia on VLSI Technology and Circuits, Kyoto, Japan, 14–16 June 2005; pp. 108–109.
20. Singanamalla, R.; Yu, H.Y.; Daele, B.V.; Kubicek, S.; Meyer, K.D. Effective Work-Function Modulation by Aluminum-Ion Implantation for Metal-Gate Technology (Poly-Si/TiN/SiO_2). *IEEE Electron Device Lett.* **2007**, *28*, 1089–1091.
21. Weber, O.; Andrieu, F.; Mazurier, J.; Casse, M.; Garros, X.; Leroux, C.; Martin, F.; Perreau, P.; Fenouillet-Beranger, C.; Barnola, S.; *et al.* Work-Function Engineering in Gate First Technology for Multi-V_T Dual-Gate FDSOI CMOS on UTBOX. In Proceedings of the IEEE International Electron Devices Meeting, San Francisco, CA, USA, 6–8 December 2010; pp. 3.4.1–3.4.4.
22. Chau, R. Advanced Metal Gate/High-*k* Dielectric Stacks for High Performance CMOS Transistors. In Proceedings of the AVS 5th International Microelectronics Interfaces Conference, Santa Clara, CA, USA, 1–4 February 2004; pp. 3–5.
23. Chau, R. Application of High-*k* Gate Dielectrics and Metal Gate Electrodes to Enable Silicon and Non-Silicon Logic Nanotechnology. *Microelectron. Eng.* **2005**, *80*, 1–6.
24. Huang, A.P.; Zheng, X.H.; Xiao, Z.S.; Wang, M.; Di, Z.F.; Chu, P.K. Interface Dipole Engineering in Metal Gate/High-*k* Stacks. *Chin. Sci. Bull.* **2012**, *57*, 2872–2878.
25. Sivasubramani, P.; Kim, J.; Kim, M.J.; Gnade, B.E.; Wallace, R.M. Effect of Composition on the Thermal Stability of Sputter Deposited Hafnium Aluminate and NitridedHafnium Aluminate Dielectrics on Si (100). *Jpn. J. Appl. Phys.* **2007**, *101*, 114108.
26. Lerouxa, C.; Baudota, S.; Charbonniera, M.; van der Geesta, A.; Caubetb, P.; Toffolia, A.; Blaisea, P.; Ghibaudoc, G.; Martina, F.; Reimbolda, G. Investigating Doping Effects on High-*k* Metal Gate Stack for Effective Work Function Engineering. *Solid State Electron* **2013**, *88*, 21–26.
27. Kita, K.; Toriumi, A. Intrinsic Origin of Electric Dipoles Formed at High-*k*/SiO_2 Interface. *Appl. Phys. Lett.* **2009**, *94*, 132902.
28. Sivasubramani, P.; Böscke, T.S.; Huang, J.; Young, C.D.; Kirsch, P.D.; Krishnan, S.A.; Quevedo-Lopez, M.A.; Govindarajan, S.; Ju, B.S.; Harris, H.R.; *et al.* Dipole Moment Model Explaining nFETVt Tuning Utilizing La, Sc, Er, and Sr Doped HfSiON Dielectrics. In Proceedings of the Symposia on VLSI Technology and Circuits, Kyoto, Japan, 12–16 June 2007; pp. 68–69.

29. He, G.; Liu, M.; Zhu, L.Q.; Chang, M.; Fang, Q.; Zhang, L.D. Effect of Postdeposition Annealing on the Thermal Stability and Structural Characteristics of Sputtered HfO_2 Films on Si (1 0 0). *Surf. Sci.* **2005**, *576*, 67–75.
30. Yu, H.Y.; Li, M.F.; Cho, B.J.; Yeo, C.C.; Joo, M.S.; Kwong, D.L.; Pan, J.S.; Ang, C.H.; Zheng, J.Z.; Ramanathan, S. Energy Gap and Band Alignment for $(HfO_2)_x$ $(Al_2O_3)_{1-x}$ on (100) Si. *Appl. Phys. Lett.* **2002**, *81*, 376–378.
31. Xu, K.; Sio, H.; Kirillov, O.A.; Dong, L.; Xu, M.; Ye, P.D.; Gundlach, D.; Nguyen, N.V. Band Offset Determination of Atomic-Layer-Deposited Al_2O_3 and HfO_2 on InP by Internal Photoemission and Spectroscopic Ellipsometry. *Jpn. J. Appl. Phys.* **2007**, *113*, 024504.