

Review

Porous Dielectrics in Microelectronic Wiring Applications

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Abstract: Porous insulators are utilized in the wiring structure of microelectronic devices as a means of reducing, through low dielectric permittivity, power consumption and signal delay in integrated circuits. They are typically based on low density modifications of amorphous SiO₂ known as SiCOH or carbon-doped oxides, in which free volume is created through the removal of labile organic phases. Porous dielectrics pose a number of technological challenges related to chemical and mechanical stability, particularly in regard to semiconductor processing methods. This review discusses porous dielectric film preparation techniques, key issues encountered, and mitigation strategies.

Keywords: porosity; dielectric; interconnect; microelectronic; integrated circuit; semiconductor

1. Introduction

The characteristic trend of the semiconductor industry over the last several decades has been the continual miniaturization of microelectronic devices. Integrated circuit density per unit area has doubled every one and a half to two years, a relationship commonly known as Moore's Law. Density increases have been accompanied by comparable increases in device performance. In recent years, however, it has become necessary to introduce new technology elements in order to maintain historical trends. The appearance of porous dielectrics in microelectronic devices represents one of the significant materials changes required to keep performance improvements on pace with device density increases.

Porous dielectrics are not employed as structural components of elementary semiconductor devices such as transistors. Rather, they serve as electrical insulation between wires used to connect different devices. Their utility lies in reducing, by virtue of a lower dielectric permittivity compared to similar non-porous insulators, the capacitance between neighboring wires. This reduction has a direct influence on power consumption and, importantly for performance, the time required for an electrical signal to travel along a wire.

Excluding very low resistance interconnects, signal delay varies as the product of wire resistance R and capacitance C [1]. In early technology generations, wire RC delays were small compared to those associated with the operation of semiconductor devices. Thus there was little motivation for reducing either wire resistivity or the dielectric constant of the materials used to insulate wires from each other. Consequently, device interconnections in high performance parts remained for many years relatively unchanged apart from dimensional scaling and were comprised of a chemically and mechanically robust combination of aluminum-based wires embedded in amorphous SiO₂ dielectric. The situation was more complicated for non-scaled products, in which *e.g.*, microprocessor size did not shrink due to added functionality. Such very large scale integration (VLSI) created the possibility of significant wire RC delays, which could be mitigated by adding wiring with large cross-sectional areas and correspondingly low resistance [2]. By the late 1990s, however, material changes were necessitated by the threat of performance improvement limitations due to wire RC delays that could not be adequately addressed by this approach.

The semiconductor industry's initial response to the *RC* wiring delay problem was by-and-large to convert from aluminum-based to lower resistivity copper-based wiring [3]. This was a revolutionary development as it involved not only a completely different metallurgical system but, in many respects, fundamentally different manufacturing processes. The superior electromigration performance of copper versus aluminum wires [4] allowed copper wire heights to be reduced to match aluminum wire resistance, with the result that capacitance improvements benefitting both power and performance could be realized. Today, Cu-based wiring is industry-standard for high performance microelectronic devices. Section 2 of the review describes a production flow for fabrication of copper interconnects and considers, as a prelude to subsequent discussions, the relative impact of individual process steps on porous dielectrics in the wiring structure.

Introduction of dielectrics with reduced permittivity followed less than a decade after the conversion to copper wiring for high performance integrated circuits. A great many dielectric alternatives spanning several material classes were investigated by individual manufacturers, industry consortia such as SEMATECH, and universities. As eventually implemented in manufacturing, the progression of new dielectrics appears to have an evolutionary character: a silica-like network of bridging oxygens is maintained for structural integrity and the dielectric constant lowered through reductions in polarizability and/or density. Plasma enhanced chemical vapor deposition (PECVD) is the predominant preparation method, although other techniques such as spin-casting of polymeric solutions (called spin-on dielectrics, or SODs) exist. For the PECVD method, modification of the dielectric structure is achieved by adjusting the chemistries of the plasma precursors and process parameters such as partial pressure, flow rate, and temperature as well as electrical characteristics of the plasma. The processes developed to create lower permittivity films are not easily described as evolutionary, however, since they have involved new precursors and, for very low dielectric constants, new preparation techniques altogether.

PECVD fluorinated silica glass (FSG) films with dielectric constant in the K = 3.6-3.8 range compared to K = 4 for SiO₂ were the first reduced permittivity insulators to appear after the

introduction of copper interconnects [5]. Carbon-doped oxides (CDO, or SiCOH) with K = 3 and below followed next [6]. More recently, multiphase carbon-doped materials in which an organic phase is burned out either thermally, by electron-beam (e-beam) radiation, or by ultraviolet (UV) radiation to create porosity and K < 2.6 have been introduced [7]. Precursors used to create such labile phases are called porogens. Accordingly, the term porous is usually restricted to this class of ultra low-K (ULK) or pSiCOH dielectrics. This review will consider both SiCOH and pSiCOH films as the former provide the structural skeleton for the latter. Section 3 presents an overview of material preparation for different types of low-K and ULK dielectrics with an eye toward strategies for mechanical property optimization. Section 4 examines trends of important physical properties versus porosity level.

Although bulk physical properties are extremely important, they do not by themselves determine how well porous dielectrics perform in microelectronic applications. Surfaces which are exposed to plasma processes during manufacturing are susceptible to damage, as reflected by increased permittivity, especially as porosity increases. Section 5 discusses the issue and mitigation strategies.

Continual modification of SiCOH films to achieve high levels of porosity for capacitance reduction is recognized as posing inherent mechanical challenges for microelectronic devices. Potential solutions to this dilemma are discussed in the Concluding Remarks, Section 6.

2. Copper Interconnect Fabrication

The greater part of fabrication of semiconductor devices and their interconnections proceeds by wafer-level processing. A wafer starts as a slice of single crystal semiconductor, called the substrate, upon which multiple microelectronic devices are built simultaneously. This section describes schematically a process flow for wafer-level fabrication of copper interconnects, the aim of which is to identify those issues which drive mechanical optimization of low-*K* and ULK materials (discussed in Section 3) and mitigation strategies related to process-induced damage (discussed in Section 5). The fabrication method depicted is an example of what is frequently called the dual inlay process. This name refers to the fact that metal deposition occurs after both interlevel and intralevel wiring patterns have been formed in the dielectric. It is also called dual damascene, in reference to an ancient method of creating metal inlay patterns.

Figure 1(a) shows a planar array of wires upon which a subsequent level of wiring is to be built. The dual inlay process begins by depositing a dielectric stack on the wafer, as illustrated in Figure 1(b). The lowermost film in the stack shown is a Cu-diffusion barrier dielectric, or cap, required for interconnect reliability [8]. An adhesion layer to improve the typically weak interfacial strength between low permittivity insulators and cap materials [9] comes next. The main (*i.e.*, low-*K* or ULK) dielectric follows and constitutes the greater part of the total stack thickness. A protective film, or hardmask, frequently SiO₂, is employed on top of the main dielectric as a process aide, e.g., to prevent surface damage in subsequent fabrication steps.

Figure 1(c) shows the wafer after a first wiring pattern has been developed in a photo-sensitive organic material, or photoresist. The latter is typically coated over the dielectric stack following a buried anti-reflective coating (BARC), used to assist photolithographic patterning. The first wiring pattern as drawn in the figure represents interlevel connections between adjacent wiring levels.

After the interlevel wiring pattern has been printed on the wafer, the images are transferred into the dielectric stack by a reactive ion etch (RIE) process. Figure 1(d) shows the transferred pattern after any remaining photolithographic materials have been removed, or stripped, from the wafer. Stripping is a critical step insofar as processes capable of removing the organic films used in the patterning process may also damage carbon-containing low-*K* and ULK dielectrics [11].

Figure 1. Schematic process flow for copper interconnects: (a) a planar array of wires embedded in a dielectric stack with top wire surfaces exposed; (b) deposition of a blanket dielectric stack; (c) photolithographic patterning of interlevel connections; (d) transfer of interlevel connection pattern into the dielectric stack; (e) photolithographic patterning of the intralevel wiring; (f) transfer of the intralevel wiring pattern into the dielectric stack; (g) metal deposition; (h) planarization of metal overfill.



With the interlevel connection pattern transferred into the dielectric stack, photolithographic patterning of the intralevel connections proceeds next. The main challenge at this point relates to the existence of exposed low-K or ULK dielectric surfaces. This raises issues of photolithographic material compatibility. Such problems can be avoided using the process structure depicted in Figure 1(e). An organic planarizing layer (OPL) is coated on the wafer followed by deposition of a low temperature oxide (LTO) film which essentially acts as a new hardmask [12]. BARC coating,

photoresist coating, and printing of the intralevel wiring pattern then proceeds as for the interlevel pattern.

Figure 1(f) depicts the interconnect structure after the intralevel wiring pattern has been transferred into the dielectric stack by a RIE process, the LTO film removed, any remaining OPL material stripped from the wafer, and the cap film opened. By this point there have been many opportunities for exposed low-*K* or ULK dielectric surfaces to be damaged or contaminated by the patterning process and it is typical for the wafer to be exposed to a compatible wet clean process, e.g., dilute hydrofluoric acid [13]. As damage typically manifests itself as a densification of the exposed low-*K* film surfaces to form poor quality SiO₂, design of the etch, strip, and clean processes is critical for maintaining low dielectric permittivity and becomes more difficult as porosity increases.

After cleaning, the wafer is ready for metallization. For copper wiring, the process begins with deposition of a barrier metal film stack, or liner, which prevents diffusion of copper into the dielectric [14]. This is important for reasons of reliability [15] and becomes more challenging as porosity in the dielectric increases, since coverage becomes difficult and the opportunity for barrier defects increases. For copper interconnects formed by electrochemical plating, as typical, the barrier film deposition process is followed by deposition of a thin Cu layer, or seed. An excess copper thickness is then plated onto the wafer, as shown in Figure 1(g). This assists the eventual planarization of the wiring level by chemical-mechanical polishing (CMP).

CMP provides one of the most critical tests of the mechanical integrity of low-*K* dielectrics. The wet environment and application of abrasive force create a situation highly conducive to crack growth, which is of particular concern for low-*K* and ULK dielectrics as these are typically in a state of tensile stress on a wafer. Moreover, the driving force for cracking can be significantly enhanced by the presence of underlying wiring [16]. Since the driving force for crack propagation increases with increasing stress level and decreasing elastic modulus, optimization of low-*K* and ULK films for these properties becomes critical.

Figure 1(h) depicts the wiring level after the CMP process has been completed. At this point the sequence starting with Figure 1(b) repeats for fabrication of the next wiring level. Complex microelectronic products can have more than ten such dual-inlay wiring levels.

3. Dielectric Deposition Processes

The focus of this section will be on precursor choice for property optimization of PECVD SiCOH and pSiCOH films. Background information on the PECVD technique can be found in Cote *et al.* [17] for conventional SiO₂ films and in Grill [18] for PECVD SiCOH, pSiCOH, and other novel dielectrics such as diamond-like carbon (DLC). Fluorinated silica glass (FSG) will be briefly discussed since it involves a modification of the silica network structure—removal of bridging oxygens—that is important in carbon-doped low-*K* and ULK films.

3.1. Fluorinated SiO₂

FSG films can be prepared by addition of SiF_4 to either conventional silane (SiH₄) or TEOS [tetraethyl orthosilicate, $Si(OC_2H_5)_4$] based oxide deposition processes or by addition of a fluorocarbon precursor such as C_2F_6 to a TEOS-based deposition process [19]. At low doping levels,

fluorine reduces the dielectric constant by eliminating highly polarizable silanol (SiOH) groups in the films and, at higher levels, by replacing bridging oxygen structures (Si-O-Si) in the glass network. Dielectric constant reductions down to K = 3 are possible. However, fluorine bonding is not stable at elevated concentrations and can adversely affect metal reliability, e.g., through attack of Ta-based barriers. FSG films as typically employed have dielectric constants in the K = 3.6-3.8 range. These films are not porous, although density [20] and modulus [20,21] are reduced compared to SiO₂.

3.2. Low-K SiCOH

In order to achieve a dielectric constant K<3 in silica network films, it is necessary to modify the structure of the material in a way that reduces polarizability and/or density. This can be achieved by bonding methyl groups to Si. The elimination of bridging oxygens by this means allows the silica network to assume a less dense arrangement than in pure SiO₂. It is possible to prepare PECVD low-*K* SiCOH films with such a structure using mixtures of hydrocarbons with the conventional oxide precursor silane [22]. More typically, silicon precursors with "built-in" methyl groups are used. These include acyclic compounds such as trimethylsilane (CH₃)₃SiH [23,24] and tetramethylsilane (CH₃)₄Si [25]. Fluorinated carbon-doped films have been prepared using mixtures of trimethylsilane and SiF₄ [26] as well. However, cyclic precursors in which the ring structure can be preserved to some extent in the final material have been found to be among the most mechanically robust low-*K* films, a finding which has guided identification of new precursors [27,28].

Grill [29] describes preparation of films with dielectric constant K = 2.8 using the cyclic compound tetramethylcyclotetrasiloxane (TMCTS, Si₄O₄C₄H₁₆) without use of a separate oxidizing agent. Lin, Tsui, and Vlassak [30] prepared PECVD carbon-doped films with dielectric constants in the range K = 3-3.3 using the cyclic compound octamethylcyclotetrasiloxane (OMCTS, C₈H₂₄O₄Si₄) and oxygen. They reported that the lowering of the dielectric constant was accompanied by a decrease in network Si-O bonds as detected by the FTIR peak near the 1062 cm⁻¹ wavenumber and an increase in suboxide/chain Si-O bonds related to the FTIR peak near the 1023 cm⁻¹ wavenumber. Such changes in bond state require careful attention as far as mechanical property optimization is concerned. Grill *et al.* [31] found that film stress decreases and that hardness and elastic modulus increase as the fraction—determined by relative FTIR peak area—of network Si-O bonds increases, with accompanying improvements in film cracking resistance. Ida *et al.* [32] found in their study of films with dielectric constants in the range K = 2.7-3.0 that low stress and higher mechanical strength correspond to greater cross-linking per ¹³C and ²⁹Si nuclear magnetic resonance (NMR). The degree of cross-linking in low-*K* SiCOH films can be increased by exposure to UV radiation [33–35].

Although the plasma reactions involved in the deposition of low-*K* carbon-doped oxide films tend to be quite complex, there have been attempts to understand mechanisms and the relationship to final film properties. Tajima *et al.* [36] attempted to predict dielectric and mechanical properties of a TMCTS-based film from first principles. Although agreement was not perfect, the role of cross-linking in promoting desirable mechanical properties was confirmed. In a subsequent theoretical analysis of chemical reactions, Tajima *et al.* [37] found that precursors should promote formation of SiC_n· radicals in the reaction chamber for efficient cross-linking.

Porosity in the low-*K* SiCOH films described in this section is interstitial in nature and not easily detectable down to K = 2.8 [38]. Nevertheless, these films have a relatively open structure as indicated by enhanced gas diffusivity, with reliability implications for their use in microelectronic applications [39]. Lane *et al.* [40] reported measureable porosity of 22% by volume for a film with K = 2.76 using positron annihilation spectroscopy (PAS/PALS). Other advanced porosimetry techniques developed to overcome difficulties associated with application of traditional gas absorption/microbalance methods to thin films include small angle X-ray scattering (SAXS) in combination with specular X-ray reflectivity (XR), small angle neutron scattering (SANS) in combination with XR, and ellipsometric porosimetry (EP) [38].

3.3. Ultra Low-K SiCOH

In order to achieve dielectric constants with K < 2.6, two-phase film deposition techniques have been developed whereby a labile organic phase is removed to leave a discrete pore structure in a more or less dense skeleton phase. Grill and Patel [41] prepared films with a dielectric constant as low as K = 2 by adding an organic precursor to the reaction chamber during deposition of a TMCTS-based film with nominal K = 2.8. The porogen phase was removed by annealing the film at 400 °C. Examples of porogen precursors that have been used with TMCTS are cyclopentene oxide (CPO, C_5H_8O) and butadiene monoxide (BMO, C_4H_6O) [42]. Gates *et al.* [43] prepared porous films using OMCTS and CPO. In principle, any hydrocarbon that can be delivered as a gas to the reaction chamber and which can be dissociated at an RF power low enough that the dielectric properties of the base film are not degraded can be used to form the porogen phase. These include cyclic unsaturated hydrocarbons, linear alkenes, and molecules with strained rings such as cycloalkene oxides [35].

The porogenic technique restores some freedom with regard to precursor choice for the skeleton phase, since this is no longer solely responsible for porosity formation, and has been extended to noncyclic precursors accordingly. Another development has been the replacement of the thermal anneals used to remove the labile phase in early ULK films by UV radiation and e-beam assisted processes. Grill *et al.* [44] developed a K = 2.4 material using diethoxymethylsilane (DEMS, C₅H₁₄O₂Si) as the skeleton precursor and bicycloheptadiene (BCHD, C₇H₈) as the porogen, with UV curing for removal of the labile phase. Aimaddeddine *et al.* [45] achieved K = 2.3 with UV-curing of an unspecified precursor system. Jousseaume *et al.* [46] compared UV and e-beam assisted removal of the labile phase in a DEMS-based film and found subtle differences in the final chemical structure.

There have been several studies aimed at understanding the formation of the dual phase and final material structure in pSiCOH films. For example, Burkey and Gleason [47] characterized condensation reactions and porogen decomposition using FTIR; Favennec *et al.* [48] studied matrix structure and porogen loading influences using FTIR and ²⁹Si solid nuclear magnetic resonance; and Castex *et al.* [49] characterized precursor reaction mechanisms in porogenic films using FTIR and quadrupole mass spectroscopy.

In addition to reducing the process time required for porogen removal, radiation enhancement promotes cross-linking in the film with accompanying improvements in mechanical properties such as Young's modulus, similar to findings in non-porous SiCOH. However, changes in stress state can be induced in other films in the dielectric stack [50] and excessive curing can actually damage pSiCOH

films [51]. Multistep processes have been proposed to optimize porogen removal and mechanical properties separately [52].

The preceding observations involve UV-assisted processes but e-beam curing raises similar concerns and a particular one with regard to electrical degradation of semiconductor devices. Owada *et al.* [53] have reported a K = 2.25 e-beam cured film free of this issue, however.

Complexities associated with the porogen approach to ultra low-K films have sustained an interest in alternative preparation methods. Kwak et al. [54] describe the use of vinyltrimethylsilane [VTMS, $CH_2 = CHSi(CH_3)_3$ for producing a porous film without introduction of a separate porogen precursor into the reaction chamber. The vinyl groups promote formation of a labile second phase which can be removed by annealing. Asami et al. [55] prepared a film with K = 2.4 using an unspecified organosilane compound containing an acetylene bond. The low dielectric constant was achieved after e-beam curing. Burkey and Gleason [56] prepared carbon-doped oxide films with dielectric constants in the K = 2.4-2.9 range using pulsed plasma chemical vapor deposition of both cyclic and non-cyclic organosilicon precursors with water as the oxidizing agent. They were able to achieve a hardness/dielectric constant combination for TMCTS comparable to that found for a porogen-based process. Tada et al. [57] prepared films with dielectric constants K<2.5 without porogens or cure processes using cyclic precursors with various side chain groups. Best results were obtained when the latter involved both vinyl (unsaturated hydrocarbon) and large alkyl (saturated hydrocarbon) groups deposited under conditions of low power and high partial pressure. Yasuhara *et al.* [58] report K = 2.2films with high modulus prepared by neutral beam enhanced CVD (NBECVD) using either dimethyldiethoxysilane (DMDEOS, (CH₃)₂Si(OC₂H₅)₂) or dimethyldimethoxysilane (DMDMOS, Si(OCH₃)₂(CH₃)₂) as precursor. In the NBECVD process, precursors are adsorbed onto the wafer and reacted using a neutral Ar beam, in contrast to conventional PECVD in which the precursors react in the plasma and subsequently deposit onto the wafer. It is evident from the preceding that several avenues to PECVD porous low-K materials are available. At present, however, the porogenic approach in conjunction with UV curing is the standard preparation technique for ULK films in the semiconductor industry. A detailed discussion of porous PECVD SiCOH precursor systems, preparation methods, and characterization techniques can be found in Grill [59].

3.4. Spin-on Dielectrics

It is possible to synthesize cage-like $(RSiO_{3/2})_n$ structures, where R is hydrogen or a methyl group. The interstices at the centers of the cages can be viewed as extremely small pores. Films based on such silsesquioxane chemistries can be formed by spin-casting and drying of solutions. Furthermore, they can be converted to dense SiO₂ by annealing and were evaluated as such as potential replacements for plasma SiO₂ films in aluminum technologies [60]. However, it is possible to preserve the cage structure such that a film with dielectric constant at or slightly below K = 3 is obtained [61]. Although the preceding references pertain to hydrogen silsesquioxane (HSQ), methyl silsesquioxane (MSQ) films have also been evaluated in similar applications and form the parent material for a large class of porous spin-on dielectrics which have been evaluated for copper wiring applications.

Porous methyl silsesquioxane films can be created by removal of a labile organic phase similarly to PECVD carbon-doped films. Knoesen *et al.* [62] prepared porous MSQ films with dielectric constants

in the range K = 1.9-2.5 using poly(dimethylaminoethyl methacrylate-co-methyl methacrylate) (DMAEMA-MMA or PMA-co-DMAEMA) as the porogen with thermal annealing. Lazzeri *et al.* [63] characterized the thermal transformation kinetics of the same system. Padovani *et al.* prepared [64] and characterized [65] porous MSQ films with dielectric constants in the range K = 2.35–2.7 in which trimethoxysilyl norbornene (TMSNB) and triethoxysilyl norbornene (TESNB) were used as porogens with thermal annealing. Chemical bonds were found between TMSNB and MSQ but not between TESNB and MSQ in the as-deposited films. Interestingly, the fracture toughness of the TESNB films was superior to the TMSNB films as well as the base MSQ material. Peng *et al.* [66] found that porogen functional groups strongly affect the final pore structure in their study of silsesquioxane-based films. As was the case for PECVD films, it is possible to create labile phases without a separate porogen precursor. Char *et al.* [67] prepared porous films by grafting various porogenic moieties onto the MSQ skeleton material.

Similar to PECVD films, radiation-assisted cures can be utilized with spin-on dielectrics. Lin *et al.* [68] found property improvements for an e-beam cured non-porogenic MSQ film used in an aluminum wiring technology. The e-beam process was found to impact semiconductor device behavior, however. Iijima *et al.* [69] compared a thermally cured porous MSQ film (K = 2.25) with a UV-cured MSQ film with higher carbon-content (K = 2.2) and improved pore structure. Volksen *et al.* [70] found that laser spike annealing helped to toughen porous organosilicate films.

Spin-on dielectrics are not limited to the silsesquioxane family of compounds, nor are they necessarily silicon-based. Wang *et al.* [71] produced a non-porogenic oxygen-free polycarbosilane-based film with K = 2.32, for example. Yamazaki *et al.* [72] prepared carbon-doped spin-on films with K = 2 using a sol-gel type method and UV curing. Silica xerogels with even lower dielectric constants have been studied as potential dielectrics for microelectronic applications [73] and used for development of porous low-*K* characterization techniques [74,75]. Integrated circuits built using spin-on organic dielectrics have also been evaluated [76,77] and porogenic versions developed [78]. High thermal expansion coefficients and related reliability issues have hindered adoption of spin-on organic films for microelectronic applications, however.

4. Physical Property Trends

For a given family of porous dielectrics, density is a useful indicator for other physical properties such as permittivity and elastic modulus. It is therefore a convenient starting point for examining the effect of porosity additions and some of the issues associated with its characterization. It will be apparent that direct comparison between different pSiCOH films with differing levels of porosity is difficult. It is possible to verify general trends, however.

If pores are assumed to exist as void space in an otherwise dense medium with density ρ_0 , porous film density decreases with increasing pore volume fraction ϕ according to the relation:

$$\rho = \rho_0 (1 - \phi) \tag{1}$$

This is certainly an approximation for the low-K dielectrics used in microelectronic applications, which lack smooth pore walls due to the interstitial character of the porosity. The density of the skeleton phase is inherently non-uniform and likely dependent on the level of porosity. These

complications pertain to the assumption that ρ_0 is constant in equation (1). There is also uncertainty with regard to the pore volume fraction ϕ , however. Measurement sensitivity with respect to pore size and interconnectivity can lead to differences in apparent porosity levels for a given material using different porosimetry techniques [38,79].

Figure 2 shows a plot of film density ρ versus non-pore volume fraction (1- ϕ) for several PECVD SiCOH films [29,80,81], spin-on films (HSQ and MSQ) [80], and xerogels [74,75]. In general, density decreases with increasing porosity, as expected. The line indicates the prediction of equation (1) with pore wall density $\rho_0 = 1.32$ g/cm³. This value equals the density of the non-porous K = 2.8 base film in [29] and is close to the pore wall densities for porous MSQ ($\rho_0 = 1.35$ g/cm³) and porous PECVD SiCOH ($\rho_0 = 1.31$ g/cm³) reported in [80]. It is evident that different values of ρ_0 must apply to at least some of the films. This is confirmed by the pore wall density measurements $\rho_0 = 1.16$ g/cm³ for the xerogel characterized in [74] and $\rho_0 = 1.83$ g/cm³ for the porous HSQ film in [80]. It is worth noting that, although these films have been viewed as low density modifications of SiO₂, the pore wall density cannot be assumed to be that of amorphous silica ($\rho = 2.2$ g/cm³). Ryan *et al.* [74] found that calculating ϕ from the measured density under this assumption gives unreasonably high predictions compared to the value determined using small angle neutron scattering.

Figure 2. Density ρ plotted against non-pore volume fraction $(1-\phi)$ for several PECVD and spin-on dielectric materials. The line represents the prediction of equation (1) assuming $\rho_0 = 1.32$ g/cm³, the density of the non-porous K = 2.8 film reported in [29].



The dielectric constant of a porous material can be calculated with the aid of the Clausius-Mossotti equation:

$$\frac{K-1}{K+2} = \frac{4\pi}{3} \sum_{i} n_i \alpha_i \tag{2}$$

where n_i is the concentration of the *i*th molecular component with polarizability α_i . If the molecular components exist in fixed relative proportions throughout the material then (2) can be rewritten in terms of the density ρ :

$$\frac{K-1}{K+2} = \frac{4\pi}{3} \frac{N_0 \alpha}{M} \rho \tag{3}$$

where N_0 is Avogadro's number, M the molecular weight, and α the polarizability of a stoichiometric unit of the material. Substitution of equation (1) into (3), which amounts to the effective medium approximation [82], yields:

$$\frac{K-1}{K+2} = \frac{4\pi}{3} \frac{N_0 \alpha}{M} \rho_0 (1-\phi)$$
(4)

The comments made in regard to ρ_0 and ϕ in equation (1) apply equally well to equation (4). Validation of the relation in (4) is further complicated by the fact that stoichiometry and polarizability are highly process dependent. For example, the series of SiCOH films characterized by Lin *et al.* [30] showed decreasing values of ρ/M and α as the C/Si ratio increased and the dielectric constant decreased. Significantly, these authors found that α values for SiCOH films were higher than for SiO₂, indicating that lower dipole density is the major factor in accounting for dielectric constant reduction in the former.

Figure 3 shows a plot of the Clausius-Mossotti parameter (K-1)/(K+2) versus non-pore volume fraction $(1-\phi)$ for several PECVD [29,40,44–46,50,79–81] and spin-on/xerogel [62,68,69,75,79,80] films. In general, dielectric constant decreases with increasing porosity, as expected. The line indicates the prediction of equation (4) using values of $\rho/M = 0.023$ mol/cm³ and $\alpha = 6.5$ Å³, which were extrapolated from data in Lin *et al.* [30] to an MSQ-like carbon-to-silicon ratio of 1:1. These values give a reasonable prediction of *K* for many of the films. However, it is again clear that different constants are required for different films, assuming that ϕ values are accurate. The two sets of data reported by Baklanov [79] are of particular interest in regard to this last caveat as they represent different porosity measurements on the same films. The open circles correspond to measurements made using ellipsometric porosimetry while the closed circles correspond to measurements made using small angle neutron scattering in combination with X-ray reflectance.

The dependence of Young's modulus *E* on porosity for a one-dimensional material composed of material chains interposed with channels of open pores was derived in closed form by Wagh *et al.* [83] and predicted to follow a power law relationship with non-pore volume fraction $(1 - \phi)$:

$$E = E_0 \left(1 - \phi\right)^n \tag{5}$$

The authors verified the validity of (5) in three-dimensional systems using numerical simulations. It is therefore not unreasonable to expect such a relation to hold for the porous dielectrics of interest. Munro [84] analyzed data for a large number of oxide ceramics and found the exponent *n* to range between 1.78 and 4.99, with average \sim 3, indicating the strength of the power law that might be expected to hold for ULK dielectrics. Difficulties similar to those encountered in analyzing the porosity dependence of density and dielectric constant apply to the case of modulus, of course, since the parameter E_0 , which corresponds to the modulus at zero porosity, is base material-specific and its independence with regard to porosity level questionable. In addition to the uncertainty in ϕ that exists

for all parameters discussed so far, there are intrinsic measurement issues for modulus, e.g., substrate effects, which make reported values at times unreliable [59].

Figure 3. Clausius-Mossotti parameter (K-1)/(K+2) plotted against non-pore volume fraction $(1-\phi)$ for several PECVD and spin-on dielectric materials. The line represents the prediction of equation (4) assuming $\rho/M = 0.023$ mol/cm³ and $\alpha = 6.5$ Å³, obtained by extrapolating data in Lin *et al.* [30] to an MSQ-like carbon-to-silicon ratio of 1:1.



Figure 4 shows a log-log plot of Young's modulus *E* versus non-pore volume fraction $(1-\phi)$ for several PECVD [29,44–46,81] and spin-on/xerogel [67,69,75] films. In general, modulus decreases with increasing porosity, as expected. The lines included in the figure represent the expected slope of the data for different values of the exponent *n* in equation (5). Individual fits to the larger data sets, not shown in Figure (4), indicate n = 4.01 for the xerogels in Herrmann [75] and n = 3.35 for the porous MSQ films in Char [67], which place them in the same range reported by Munro [84]. It is difficult to draw stronger conclusions, however.

The last parameter to be examined in this section is not a physical property *per se* but a processdependent material characteristic. A crack driving force parameter, designated G', related to the crack extension force or fracture energy release rate [85] per unit blanket film thickness can be defined in terms of the residual film stress σ and elastic modulus E as follows:

$$G' = \sigma^2 / E \tag{6}$$

This parameter, which differs from the true crack driving force per unit film thickness by a multiplicative constant of order unity, provides a highly useful figure of merit for how well low-K and ULK films, which are generally tensile stressed, behave during CMP and other situations of mechanical loading, including service: the larger the value of G', the greater the risk of cohesive failure to occur. Since residual film stress is not an intrinsic physical property with a definite relationship to porosity level, it will be more convenient to consider the trend of G' versus dielectric constant in the discussion which follows.

Figure 4. Young's modulus *E* plotted against non-pore volume fraction $(1-\phi)$ for several PECVD and spin-on dielectric materials. The lines represent the expected slope for different values of exponent *n* in equation (5).



Figure 5 shows a plot of crack driving force parameter *G*' versus dielectric constant *K* for several PECVD SiCOH [24,31,32], PECVD ULK SiCOH [44,45,50], and spin-on porous MSQ [69] films. The crack driving force parameter is found to increase rapidly with reduction in dielectric constant in the range K = 2.7-3.1 where the transition from a non-porous to porous structure occurs. With further reductions in *K*, the crack driving force appears to increase more slowly or to remain fairly flat. Irrespective of any fundamental explanation for the observed behavior, it is evident that for a given value of *K*, a wide range of crack driving forces is possible. This underscores the need for film optimization for low stress and high modulus, particularly in light of the fact that cohesive strength drops with decreasing dielectric constant [86].

It should be emphasized that the parameter *G*', while a highly useful metric, can be misleading if examined without reference to other relevant data. For example, the porous MSQ film with K = 2.25 studied by Iijima *et al.* [69] appears to have exceptionally good crack resistance compared to the other ULK films shown. However, as the authors indicate, this particular film has large pores which make it highly susceptible to other types of process-induced damage, discussed in the next section. The K = 2.2 film from the same reference has a crack driving force parameter more than twice as great but improved process robustness in comparison, due to its finer pore structure.

Figure 5. Crack driving force parameter G' defined in equation (6) plotted versus dielectric constant K for several carbon-doped oxide films including non-porous CVD SICOH, porous CVD ULK SiCOH, and porous spin-on MSQ.



5. Plasma-Induced Damage and Repair

The discussion of the preceding section focused on optimization of low-*K* and ULK dielectric deposition processes for bulk physical properties. However, as mentioned in Section 2, the exposure of the dielectric to reactive ion etch and strip processes required for interconnect patterning can damage the film such that the original bulk properties, dielectric constant in particular, are severely degraded. The propensity for damage is exacerbated by the presence of porosity which allows deeper penetration of the plasma into the film, especially for highly interconnected pores [87]. Worsley *et al.* [88] showed that solvent penetration studies are effective for characterizing the interconnectedness of pore morphology. Solvent diffusivity was found to increase rapidly at about 25% pore volume, indicating the onset of open porosity. The data in Figure 3 suggest that this increased sensitivity to plasma penetration and damage occurs as the dielectric constant drops below K = 2.5 approximately.

Strategies involving modified porogen removal approaches have been developed for reducing plasma-induced damage in ULK films. Kagawa *et al.* [89] used partial porogen removal after ULK film deposition with removal of remaining porogen by thermal treatment after wires had been fully formed, a variant on full post-metallization porogen removal [90]. These approaches require that the porogen phase be stable at normal process temperatures prior to final removal [91]. Retention of the porogen phase evidently blocks penetration of the plasma into the film. A similar benefit is seen in the conventional porogen removal approach by increasing carbon content in the post-cured film [92].

Considerable care is required in developing etch and strip chemistries. During pattern transfer, dimensional control is typically achieved by depositing a thin fluorocarbon film on the sidewalls of the dielectric to prevent lateral etching. This film helps to limit damage to the dielectric but must be removed to avoid metallization issues. The challenge is to find strip chemistries which are effective at removing the fluorocarbon film and any remaining sacrificial patterning films such as OPL with

minimal damage to the dielectric. Furukawa *et al.* in studies of porous spin-on MSQ [93] and CVD SiCOH [94] films found that CF_4/O_2 and N_2/O_2 strip chemistries were highly effective at removing fluorocarbon but caused extensive depletion of carbon in the etched films, while N_2/H_2 chemistries had thinner damage layers but were less effective at fluorine removal. Aimadeddine *et al.* [95] reported that oxygen-based strips had deleterious effects and nitrogen-based strips positive effects on interconnect reliability. Dalton *et al.* [96] found that oxidizing chemistries were highly damaging in porous films as well, although viable in dense films. Positive results for an oxidizing strip chemistry with ULK were reported, however, by Shi *et al.* [97] and Liu *et al.* [98] for CO₂-based strip processes. N_2/H_2 strips have been recommended for SiO₂ aerogels [99] and for post-metallization porogen removal schemes [100].

Apparently contradictory data abound in the literature and reflect the fact that development of etch and strip process is very much an art, with strip performance being highly material dependent. In contrast to the several positive results cited above for reducing chemistries, Grill and coworkers found that H_2 containing plasmas were highly damaging to PECVD ULK SiCOH [101], with the extent of the damage influenced by the precursor system of the dielectric [102]. Gas mixture composition in the strip process matters as well. Grill and Patel [103] found that N_2/H_2 was superior to N_2/He but inferior to N_4 with respect to damage propensity.

Worsley *et al.* [104] found that different strip processes tend to result in similar final damage signatures (e.g., loss of methyl groups, increased cross linking and densification with concomitant increases in dielectric constant) but differ in kinetics. Ion bombardment appears to be an important factor [11]. Downstream plasma strip processes, in which the wafer is remote from the plasma source, appear to reduce damage propensity [11,105].

No strip process appears to be completely satisfactory at achieving a damage-free structure in ULK materials and corrective actions are typically required. A conventional approach is to try to limit the damage as much as possible and to remove the damaged layer prior to metallization, e.g., by dilute hydrofluoric acid (DHF) [13]. Broussous *et al.* [106] found that a DHF clean was necessary to improve interconnect yield but had a narrow process window.

An alternative approach is to intentionally damage the exposed surfaces in a controlled manner in order to create a permanent thin dense layer [107–109]. NH₃ plasma pore sealing has been found to prevent moisture uptake in ULK materials [110] and even to be resistant to limited DHF exposure [111]. The disadvantage of plasma pore sealing is that it tends to raise the effective dielectric constant, although low impact processes have been reported [112]. A potential advantage is mitigation of metal barrier coverage issues over porous surfaces [113]. Pore sealing techniques based on organic polymer deposition [114,115] have also been investigated. These do not address plasma-induced damage, however.

A third alternative is to try to restore the ULK dielectric constant by damage repair processes, frequently called silvlation. Supercritical CO_2 can be used to carry various organosilicon compounds into the interior of a damaged ULK film for removal of silanol (SiOH) groups [116,117]. Hexamethyldisilazane (HMDS) [118] and TMCTS [119] treatments has been reported to have similar damage repair capability. Without the assistance of supercritical CO_2 , the ability for repair chemicals to enter the damaged dielectric depends heavily on the surface tension state [120].

Yet another, perhaps counterintuitive, approach is to use a plasma for film recovery. Bao *et al.* [121] reported the ability of a CH_4 plasma to repair oxygen plasma damage, although the recovery was not complete due to the formation of a thin polymer film on exposed surfaces, which limited penetration.

6. Concluding Remarks

The aim of this review was five-fold: to describe the microelectronic scaling trends which led to the introduction of porous insulators in integrated circuits; to highlight the manufacturing process sensitivities which dictate the physical property requirements for these materials; to identify the characteristics of material precursors which help to promote the required properties; to validate the expected dependencies of important physical properties on porosity level; and to describe methods for guaranteeing the desired physical properties in the final integrated wiring structure. It cannot claim to be exhaustive in terms of all relevant contributions to the literature, particularly in regard to the vast amount of characterization work documented. Nor is it completely comprehensive with respect to all issues relevant to low-*K* and porous dielectrics in microelectronic applications, e.g., protection of the wiring structure during chip dicing [122,123] and in service [124,125].

The review concludes with some final remarks on possible future directions for very low permittivity dielectrics in microelectronic applications. There are essentially three paths available. The first is to continue to increase porosity levels using established ULK dielectric preparation techniques. This will require careful optimization of the skeletal structure for mechanical properties. Recent work testifies to the viability of this approach. Adjustment of precursor chemistries to promote formation of alkyl bridge groups, for example, shows promise for both PECVD [126] and spin-on films [127]. The second is to develop new materials with the desired structure/property relations. Periodic porous self-assembled SiO₂ films, for example, show improved mechanical properties versus random structures [128], although pore size control is still critical [129]. The third is to adopt a paradigm shift for achieving low effective dielectric constants. Airgaps, in which low permittivity areas are created in critical areas with the majority of the structure remaining a robust, higher-*K* film [130] are an especially attractive solution to problem of achieving low-*K* with superior mechanical properties, as indicated by an already extensive literature.

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