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A Semi-Analytical Extraction Method for Interface and Bulk Density of States in Metal Oxide Thin-Film Transistors

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Abstract: A semi-analytical extraction method of interface and bulk density of states (DOS) is proposed by using the low-frequency capacitance–voltage characteristics and current–voltage characteristics of indium zinc oxide thin-film transistors (IZO TFTs). In this work, an exponential potential distribution along the depth direction of the active layer is assumed and confirmed by numerical solution of Poisson's equation followed by device simulation. The interface DOS is obtained as a superposition of constant deep states and exponential tail states. Moreover, it is shown that the bulk DOS may be represented by the superposition of exponential deep states and exponential tail states. The extracted values of bulk DOS and interface DOS are further verified by comparing the measured transfer and output characteristics of IZO TFTs with the simulation results by a 2D device simulator ATLAS (Silvaco). As a result, the proposed extraction method may be useful for diagnosing and characterising metal oxide TFTs since it is fast to extract interface and bulk density of states (DOS) simultaneously.

Keywords: capacitance–voltage (C–V) characteristics; current–voltage (I–V) characteristics; density of states (DOS); metal oxide thin-film transistors (TFTs)

1. Introduction

Thin film transistors (TFTs) are one kind of field-effect transistors (FETs). Their structure and operation principles are similar to those of metal oxide semiconductor field effect transistors (MOSFETs), which are commonly used in modern integrated circuits (ICs) [1]. Amorphous oxide semiconductor thin-film transistors (AOS TFTs) are considered one of the most promising technologies for flat panel display (FPD) due to transparency, good uniformity, higher mobility than hydrogenated amorphous silicon TFTs (a-Si:H TFTs), good process compatibility with a-Si TFTs, and a lower temperature fabrication process than low temperature poly-silicon (LTPS) TFTs [2–5]. The electrical characteristics of AOS TFTs are significantly affected by the bulk density of states (DOS) in the active layer and the interface density of states between the gate insulator and the active layer. The bulk DOS may be attributed to structural disorder (bond angles and length variations), dangling bonds, non-stoichiometry, and carrier scattering in the amorphous films [6]. The interface DOS may be caused by defects located at the interface, which can exchange charge with the active layers by capturing or emitting electrons [7]. It is important to extract DOS of TFTs for device design, process characterization, or modeling. Several methods have been developed to extract only the bulk DOS, such as numerical

calculations [8], optical illumination [9], temperature-dependent characteristics [10], or multi-frequency current–voltage (C–V) characteristics [11]. However, it is usually difficult to extract the interface DOS and the bulk DOS simultaneously.

Lui et al. [12] and Kimura [13] extracted the interface and bulk density of states in TFTs from the characteristics of capacitance–voltage and current–voltage based on the numerical iterative solution of Poisson's equation. However, the numerical iterative solution generally has the disadvantages of operation complexity, long computational time, and possible convergence problems. Hastas et al. extracted interface trap states from analysis of the transfer characteristics in the sub-threshold region and the bulk trap states by numerically fitting the surface potential equation [14]. Tsuji et al. extracted the interface trap density based on an expression of interface trap charge density (Q_{it}) as functions of the front and back-side surface potentials, in which the electric field at the back side is assumed to be zero [15]. Therefore, it is essential to develop analytical methods for extracting both the interface DOS and the bulk DOS of TFTs.

In this work, we propose a semi-analytical method to extract the interface DOS and the bulk DOS in indium zinc oxide (IZO) TFTs simultaneously by only using the low-frequency capacitance–voltage characteristics and current–voltage characteristics.

2. Extraction Method

Figure 1a shows a schematic cross-sectional view of indium zinc oxide (IZO) TFTs with inverted staggered bottom gate structure. The IZO material as the channel layer has the advantages of transparency, high mobility, and excellent drain current saturation [16]. Figure 1b shows the energy band diagram of the device, in which the surface potential (Ψ_s) and the back interface potential (Ψ_b) are respectively labeled. Poisson's equation is given by

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\varepsilon_s} = \frac{q}{\varepsilon_s} \Big[n_{free}(x) + n_{trap}(x) \Big]$$
(1)

where $n_{free}(x)$ and $n_{trap}(x)$ are the free electron concentration and localised trapped electron concentration, respectively.



Figure 1. (a) Cross-sectional view of indium zinc oxide thin-film transistors (IZO TFTs) with inverted staggered bottom gate structure; (b) energy band diagram along the thin-film depth direction of IZO TFTs.

Using the relationship $\frac{d^2\psi}{dx^2} = \frac{1}{2}\frac{d}{d\psi}\left(\frac{d\psi}{dx}\right)^2$, we can get

$$\left. \left(\frac{d\psi}{dx} \right)^2 \right|_{\psi = \psi_s} - \left. \left(\frac{d\psi}{dx} \right)^2 \right|_{\psi = \psi_b} = 2 \int_{\psi_b}^{\psi_s} \frac{d^2\psi}{dx^2} d\psi \tag{2}$$

Substituting Equation (1) into Equation (2) and differentiating both sides with respect to Ψ , we have

$$\left. \frac{d}{d\psi_s} \left(\frac{d\psi}{dx} \right)^2 \right|_{\psi = \psi_s} = -2 \frac{\rho(\psi_s)}{\varepsilon_s} \tag{3}$$

$$\left. \frac{d}{d\psi_b} \left(\frac{d\psi}{dx} \right)^2 \right|_{\psi = \psi_b} = -2 \frac{\rho(\psi_b)}{\varepsilon_s} \tag{4}$$

where $\rho(\Psi_s)$ is the surface charge concentration, and $\rho(\Psi_b)$ is the back interface charge concentration. Equations (3) and (4) can be further rearranged as

$$2\left(\frac{d\psi}{dx}\right)\Big|_{\psi=\psi_s}\frac{d}{d\psi_s}\left(\frac{d\psi}{dx}\right)\Big|_{\psi=\psi_s} = -2\frac{\rho(\psi_s)}{\varepsilon_s}$$
(5)

$$2\left(\frac{d\psi}{dx}\right)\Big|_{\psi=\psi_b}\frac{d}{d\psi_b}\left(\frac{d\psi}{dx}\right)\Big|_{\psi=\psi_b} = -2\frac{\rho(\psi_b)}{\varepsilon_s} \tag{6}$$

Based on Gauss's theorem, the surface charge per unit area in the channel (Q_s) considering the effect of the back interface potential can be expressed as

$$Q_s = \varepsilon_s \left. \frac{d\psi}{dx} \right|_{\psi = \psi_s} - \varepsilon_s \left. \frac{d\psi}{dx} \right|_{\psi = \psi_b} \tag{7}$$

In this paper, the potential distribution along the depth direction (x) of the active layer is assumed as

$$\psi(x) = \psi_s \exp\left(-\frac{x}{x_0}\right) \tag{8}$$

where x_0 is the characteristic length of the potential distribution. Note that the assumption for Equation (8) will be confirmed by the numerical solution of Poisson's equation in Appendix A and the device simulation in Section 3. Substituting Equation (8) into Equations (5)–(7), we have

$$\rho(\psi_s) = -\varepsilon_s \frac{\psi_s}{x_0^2} \tag{9}$$

$$\rho(\psi_b) = -\varepsilon_s \frac{\psi_b}{x_0^2} \tag{10}$$

$$Q_s = -\varepsilon_s \left(\frac{\psi_s}{x_0} - \frac{\psi_b}{x_0}\right) = x_0(\rho(\psi_s) - \rho(\psi_b)) \tag{11}$$

While in [12], the surface charge at the back interface was not taken into account.

The differential of surface potential with respect to gate-source bias can be expressed as [17]

$$\frac{d\psi_s}{dV_{gs}} = 1 - \frac{dQ_g/dV_{gs}}{C_{ox}} = 1 - \frac{C_g(V_{gs})}{C_{ox}}$$
(12)

where $C_g(V_{gs})$ is gate capacitance at some V_{gs} , C_{ox} is the gate oxide capacitance per unit area, and Q_g is the charge per unit area at the gate electrode

$$Q_{g} = \int_{0}^{V_{gs}} C_{g} (V_{gs}') dV_{gs}'$$
(13)

The nonlinear relation between Ψ_s and V_{gs} can be obtained by integrating Equation (12) over V_{gs} :

$$\psi_{s} = \int_{V_{fb}}^{V_{gs}} \left(1 - \frac{C_{g}(V_{gs}')}{C_{ox}} \right) dV_{gs}'$$
(14)

where V_{fb} is the flat band voltage.

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The free charge density per unit area (Q_i) can be expressed by an integration of $n_{free}(x)$ over x.

$$Q_i(V_{gs}) = -q \int_0^{t_s} n_0 \exp\left(\frac{\psi(x)}{V_t}\right) dx = -q \int_0^{t_s} n_0 \exp\left(\frac{\psi_s \exp\left(-\frac{x}{x_0}\right)}{V_t}\right) dx \tag{15}$$

where t_s is the thickness of the active layer, n_0 is the flat band electron concentration, and V_t is the thermal voltage (kT/q). On the other hand, Q_i can also be obtained from the transfer characteristics of TFT at low V_{ds} .

$$Q_i(V_{gs}) = -\frac{I_d(V_{gs})}{\mu \frac{W}{L} V_{ds}}$$
(16)

Note that n_0 can be extracted from Equation (15) equal to Equation (16) at the condition of flat band, i.e., $\Psi_s = 0$ and $V_{gs} = V_{fb}$. Then, x_0 at some V_{gs} can be calculated from Equation (15) equal to Equation (16) by numerical integration.

Furthermore, based on the charge conservation relationship $Q_g + Q_o + Q_s = 0$, where Q_o is the effective interface charge per unit area at the gate insulator, one obtains

$$Q_o = -Q_g - Q_s \tag{17}$$

Thus, the interface density of states (N_{it}) can be calculated by differentiating Q_0 with respect to Ψ_s

$$N_{it}(E_{F0} + q\psi_S) = -\frac{1}{q^2} \frac{dQ_0}{d\psi_S}$$
(18)

where E_{F0} is the bulk Fermi level of the active layer, which is calculated from the relationship of n_0 to E_{F0} :

$$n_0 = N_C \exp(\frac{E_{F0} - E_C}{kT}) \tag{19}$$

where $N_{\rm C}$ is the effective density of states in the conduction band with a typical value of $5 \times 10^{18} \, {\rm cm}^{-3}$ [18].

Furthermore, based on the surface potential Ψ_s given by Equation (14) and the surface charge concentration $\rho(\Psi_s)$ given by Equation (9), the bulk density of states can be given by [17]

$$N_{bt}(E_{F0} + q\psi_s) = -\frac{1}{q^2} \frac{\rho(\psi_s + \Delta\psi_s) - \rho(\psi_s)}{\Delta\psi_s} - \frac{n_0}{qV_t} \exp\left(\frac{\psi_s}{V_t}\right)$$
(20)

The extraction procedure of DOS is described as follows. Firstly, Ψ_s with respect to V_{gs} is obtained from the $C_g - V_{gs}$ characteristics of TFTs by Equation (14). Secondly, x_0 can be calculated from the current characteristics of TFTs by using Equations (15) and (16). Thirdly, $\rho(\Psi_s)$, Q_s , and Q_o will be subsequently obtained by Equations (9), (11), and (17), respectively. Finally, the interface density of states ($N_{it}(E)$) and the bulk density of states ($N_{bt}(E)$) can be extracted by Equations (18) and (20), respectively. As a result, the extraction method may be easily realised step by step as seen from the above extraction procedure.

3. Results and Discussion

The fabrication process of the IZO TFTs is described as follows. A gate electrode of molybdenum (Mo, 200 nm) is deposited by direct current (DC) sputtering. Subsequently, a 300 nm gate insulator (SiO₂) was deposited by plasma-enhanced chemical vapor deposition (PECVD). A 30 nm IZO active layer is deposited by using a radio frequency (RF) magnetron system with the segregated target of IZO (In₂O₃:ZnO = 1:1). Then, an etch stopper layer (ESL) SiO₂ is deposited by PECVD to protect the active layer. Finally, a 200nm Mo is formed by sputtering as S/D electrodes. The channel length and width of IZO TFTs are determined by layout and patterned by the conventional lithographic techniques.

The current–voltage (I–V) and C–V characteristics of TFTs are measured by using a probe station and a semiconductor parameter analyser (Agilent B1500, Agilent Technologies Inc., Santa Clara, CA, USA). The transfer characteristics are measured by scanning the gate-source voltage (V_{gs}) from -10 V to 10 V with the step of 0.1 V at the condition of V_{ds} = 0.1 V. The C–V characteristics are measured by superimposing the AC voltage signal (amplitude = 200 mV, frequency = 1 kHz) to DC gate bias in the condition of source and drain electrodes connected together. Note that those measurements are done at room temperature in the dark air ambient. It is thought that the DOS distribution of AOS TFTs remains unchanged at different temperatures [10]. Figure 2a shows the transfer characteristics of IZO TFTs ($W/L = 20 \ \mu m/10 \ \mu m$). The threshold voltage, the field-effect mobility, sub-threshold swing (SS), and on/off current ratio (I_{on}/I_{off}) of the pristine TFTs are extracted to be 1.8 V, 12.36 cm²/(V·s), 0.23 V/dec, and 1×10^7 , respectively. V_{fb} is extracted as 0.6 V from the I–V characteristics following the method developed by Migliorato et al. [19]. n_0 is extracted as 3.84×10^{16} cm⁻³ by (15) when $\Psi_s = 0$, i.e., $V_{gs} = V_{fb}$. Figure 2b shows the $C_g - V_{gs}$ characteristics of the devices at the frequency of 1 kHz, which are measured with source and drain electrodes combined together. Note that the frequency of 1 kHz for the AC signal may be low enough to make the TFTs work in the quasi-static conditions. Figure 3 shows the surface potential (Ψ_s) with respect to V_{gs} from (14) based on the C–V characteristics and the value of V_{fb} . Figure 2c shows the micrograph of IZO TFTs with $W/L = 20 \ \mu m/10 \ \mu m$.



Figure 2. Experimental data of IZO TFTs ($W/L = 20 \ \mu m/10 \ \mu m$). (**a**) Transfer characteristics; (**b**) $C_g - V_{gs}$ characteristics; (**c**) The micrograph of the devices.



Figure 3. Ψ_s versus V_{gs} obtained by (14) based on the capacitance–voltage (C–V) characteristics.

For further verification of (8), we perform the device simulation by the 2D device simulator ATLAS (Silvaco) for the IZO TFTs as described above. Figure 4 shows the distribution of the potential along the depth direction (x) at the conditions of $V_{gs} = 2.0$ V, $V_{ds} = 0.1$ V. It is found that the proposed Equation (8) can fit the simulated potential distribution well. Note that at other values of Vgs including that at the subthreshold region, the simulated potential distributions are also found to be well fitted by Equation (8) with different values of x_0 . As a result, Equation (8) may be reasonable and correct

for reproducing the potential distribution of the thin active layer. Furthermore, based on the I–V characteristics and the surface potential distribution as seen in Figure 3, the value of x_0 can be extracted from Equation (15) equal to Equation (16), as shown in Figure 5. It is found that the value of x_0 tends to vary slowly when V_{gs} is larger than the threshold voltage, because the variation of Q_i changes more slowly for TFTs working in the above-threshold region.



Figure 4. The potential distribution simulated by a 2D device simulator ATLAS.



Figure 5. The calculated results of x_0 versus V_{gs} .

Figure 6 shows the extracted interface density of states profile calculated from Equation (18). It is found that the interface DOS distribution is quite flat for the energy far from E_C , while it linearly increases with the increase of energy close to E_C at the exponent coordinate. Then, the interface DOS of AOS TFTs may be divided into two parts: constant deep states and exponential tail states, i.e.,

$$N_{it}(E) = N_{iD} + N_{iT} \exp\left(\frac{E - E_C}{E_{iT}}\right)$$
(21)

where N_{iD} is the density of deep states, N_{iT} is the density tail states at the conduction edge, and E_{iT} is the characteristic energy of tail states. For details, N_{iD}/N_{iT} is extracted by extrapolating the deep/tail states to $E = E_C$, and E_{iT} is extracted from the slope of $\log(N_{it})$ versus ($E - E_C$) for the tail states. The extracted values are $N_{iD} = 1.3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, $N_{iT} = 2.9 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, $E_{iT} = 0.08 \text{ eV}$. Obviously, the interface DOS distribution can be used to characterise interface quality and the reliability of AOS TFTs [20,21].



Figure 6. Extracted interface density of states (DOS) as a function of $E - E_C$ from the proposed method (symbols) and results fitted by (21) (solid lines).

Figure 7 shows the bulk density of states profile extracted from Equation (20). It is observed that the bulk DOS distribution slowly increases with the increase of the energy far from E_C , while it quickly increases with the increase of energy close to E_C at the exponent coordinate. It is found that the bulk DOS may be a superposition of exponential deep states and exponential tail states, i.e.,

$$N_{bt}(E) = N_{bD} \exp\left(\frac{E - E_C}{E_{bD}}\right) + N_{bT} \exp\left(\frac{E - E_C}{E_{bT}}\right)$$
(22)

where N_{bD}/N_{bT} is the density of deep/tail states at the conduction edge and E_{bD}/E_{bT} is the characteristic energy of deep/tail states, of which the extraction method is similar to that of interface DOS as described above. The extracted values are $N_{bD} = 6.0 \times 10^{16} \text{ cm}^{-3} \text{ eV}^{-1}$, $E_{bD} = 5.0 \text{ eV}$, $N_{bT} = 6.5 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$, and $E_{bT} = 0.10 \text{ eV}$. Such double exponential distribution for the bulk DOS can also be seen in other previously reported works [8–11]. For details, the deep states in AOSs may derive from oxygen deficiency, while the tail states originate from the variation of In–O–metal bonding angles [22].



Figure 7. Extracted bulk DOS as a function of $E - E_C$ from the proposed method (symbols) and results fitted by (22) (solid lines).

The device simulation is performed by a 2D device simulator ATLAS (Silvaco, Silvaco International, Santa Clara, CA, USA) to verify the proposed method, where the extracted values of interface DOS and bulk DOS are inserted into the simulator. The other parameters of IZO TFTs in the simulation are the same as those of the fabricated IZO TFTs. As seen from Figure 8, the simulation results exhibit a good agreement with the measured transfer and output characteristics of IZO TFTs.

In brief, the proposed extraction method for interface and bulk DOS is valuable for the application in metal oxide TFTs.



Figure 8. Experimental data (symbols) and simulated results (solid lines) of IZO TFTs with $W/L = 20 \ \mu m/10 \ \mu m$. (a) Transfer characteristics; (b) output characteristics.

4. Conclusions

In this paper, we propose a semi-analytical extraction method for the interface DOS and the bulk DOS of IZO TFTs by using the low-frequency C–V characteristics and I–V characteristics. It is shown that the interface DOS is extracted as a superposition of constant deep states and exponential tail states with $N_{iD} = 1.3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, $N_{iT} = 2.9 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, and $E_{iT} = 0.08 \text{ eV}$. Additionally, the bulk DOS is extracted as the superposition of exponential deep states and exponential tail states with $N_{bD} = 6.0 \times 10^{16} \text{ cm}^{-3} \text{ eV}^{-1}$, $E_{bD} = 5.0 \text{ eV}$, $N_{bT} = 6.5 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$, and $E_{bT} = 0.10 \text{ eV}$. Furthermore, the device simulation is performed by a 2D device simulator to verify the extracted values of interface DOS and bulk DOS. It is found that there is a good agreement between simulation results and the measured transfer and output characteristics of IZO TFTs. Hence, the proposed extraction method for interface and bulk DOS may be valuable for characterising metal oxide TFTs due to the advantages of being semi-analytical and fast. Since the proposed extraction method is directly deduced from Poisson's equation, it may also be applied in other types of TFTs, such as a-Si:H TFTs, polysilicon TFTs, or organic TFTs.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Poisson's equation is rewritten by

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_s} \left[n_{free}(x) + n_{trap}(x) \right]$$
(A1)

where $n_{free}(x)$ and $n_{trap}(x)$ may be expressed as

$$n_{free}(x) = n_0 \exp(\frac{\psi(x)}{V_t}) \tag{A2}$$

$$n_{trap}(x) = \int_{E_V}^{E_{F0} + q\psi(x)} N_{bt}(E) dE$$
(A3)

Note that, Equation (A2) represents the electron concentration varying with surface band bending [7]. Substituting (22) into (A3) and integrating, we have

$$n_{trap}(x) = N_{D0} \exp\left(\frac{q\psi}{E_{bD}}\right) + N_{T0} \exp\left(\frac{q\psi}{E_{bT}}\right) - n_{t0}$$
(A4)

with

$$N_{D0} = N_{bD}E_{bD}\exp\left(\frac{E_{F0} - E_c}{E_{bD}}\right)$$
$$N_{T0} = N_{bT}E_{bT}\exp\left(\frac{E_{F0} - E_c}{E_{bT}}\right)$$
$$n_{t0} = N_{bD}E_{bD}\exp\left(\frac{E_v - E_c}{E_{bD}}\right) + N_{bT}E_{bT}\exp\left(\frac{E_v - E_c}{E_{bT}}\right)$$

Then, substituting (A2) and (A4) into (A1), yields

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_s} \left[n_0 \exp(\frac{\psi}{V_t}) + N_{D0} \exp(\frac{q\psi}{E_{bD}}) + N_{T0} \exp(\frac{q\psi}{E_{bT}}) - n_{t0} \right]$$
(A5)

Obviously, there is no analytical solution for (A5) due to its complexity. Hence, a numerical iterative solution for (A5) should be used to observe the distribution of potential.

Under the boundary conditions

$$\psi(0) = \psi_s \text{and} - \frac{d\psi}{dx}\Big|_{x=0} = E_s$$
 (A6)

where Ψ_s is obtained from (14). E_s is the surface electric field of the active layer, which is obtained from the relationships $\varepsilon_{ox}V_{ox}/t_{ox} = \varepsilon_s E_s$ and $V_{gs} = \phi_{ms} + \psi_s + V_{ox}$, where V_{ox} is the voltage across the oxide and Φ_{ms} is the work function difference between the gate and active layer semiconductor.

Then

$$E_s = (V_{gs} - \phi_{ms} - \psi_s)C_{ox}/\varepsilon_s \tag{A7}$$

As a result, Poisson's equation of (A5) can be numerically solved under the boundary conditions of (A6) by using the conventional finite difference method. Figure A1 shows the numerical results of the potential along the depth direction (*x*) with the extracted values of $N_{bt}(E)$ at the condition of $V_{gs} = 1.0$ V. It is shown that the numerical results of potential distribution may be reproduced well by (8). It is further found that the numerical results of potential distribution at other V_{gs} can also be fitted well by (8) with different x_0 . Similarly, analytical complex exponential distributions of potential are also obtained by only taking into account either the free electrons [23] or the trapped electrons [12] in Poisson's equation. In brief, Equation (8) may be a reasonable approximation for the potential distribution to achieve a good tradeoff between accuracy and simplicity.



Figure A1. The potential distribution by numerical solution for (A5).

References

- 1. Yue, K. Thin film transistor technology—Past, present, and future. *Electrochem. Soc. Interface* 2013, 22, 55–61.
- Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* 2004, 432, 488–492. [CrossRef] [PubMed]
- 3. Park, J.S.; Maeng, W.-J.; Kim, H.-S.; Park, J.-S. Review of recent developments in amorphous oxide semiconductor thin-film transistor devices. *Thin Solid Films* **2012**, *520*, 1679–1693. [CrossRef]
- Lin, Z.; Lan, L.; Xiao, P.; Sun, S.; Li, Y.; Song, W.; Gao, P.; Wang, L.; Ning, H.; Peng, J. High-mobility thin film transistors with neodymium—Substituted indium oxide active layer. *Appl. Phys. Lett.* 2015, 107, 112108. [CrossRef]
- Sheng, J.; Lee, H.-J.; Oh, S.; Park, J.-S. Flexible and high-performance amorphous indium zinc oxide thin-film transistor using low-temperature atomic layer deposition. *ACS Appl. Mater. Interfaces* 2016, *8*, 33821–33828.
 [CrossRef] [PubMed]
- 6. Yu, E.K.-H.; Jun, S.; Kim, D.H.; Kanicki, J. Density of states of amorphous In-Ga-Zn-O from electrical and optical characterization. *J. Appl. Phys.* **2014**, *116*, 154505. [CrossRef]
- 7. Nicollian, E.H.; Brews, J.R. *MOS (Metal Oxide Semiconductor) Physics and Technology;* Wiley–Interscience: New York, NY, USA, 1982.
- 8. Kimura, M.; Nakanishi, T.; Nomura, K.; Kamiya, T.; Hosono, H. Trap densities in amorphous-InGaZnO₄ thin-film transistors. *Appl. Phys. Lett.* **2008**, *92*, 133512. [CrossRef]
- Bae, H.; Choi, H.; Jun, S.; Jo, C.; Kim, Y.H.; Hwang, J.S.; Ahn, J.; Oh, S.; Bae, J.-U.; Choi, S.-J.; et al. Single-scan monochromatic photonic capacitance-voltage technique for extraction of subgap DOS over the bandgap in amorphous semiconductor TFTs. *IEEE Electron Dev. Lett.* 2013, *34*, 1524–1526. [CrossRef]
- 10. Chen, C.; Abe, K.; Kumomi, H.; Kanicki, J. Density of states of a-InGaZnO from temperature-dependent field-effect studies. *IEEE Trans. Electron Dev.* **2009**, *56*, 1177–1183. [CrossRef]
- 11. Lee, S.; Park, S.; Kim, S.; Jeon, Y.; Jeon, K.; Park, J.-H.; Park, J.; Song, I.; Kim, C.J.; Park, Y.; et al. Extraction of subgap density of states in amorphous InGaZnO thin-film transistors by using multifrequency capacitance-voltage characteristics. *IEEE Electron Dev. Lett.* **2010**, *31*, 231–233.
- 12. Lui, O.K.B.; Tam, S.W.B.; Migliorato, P.; Shimoda, T. Method for the determination of bulk and interface density of states in thin-film transistors. *J. Appl. Phys.* **2001**, *89*, 6453–6458. [CrossRef]
- 13. Kimura, M. Extraction technique of trap densities in thin films and at insulator interfaces of thin-film transistors. *IEEE Electron Dev. Lett.* **2010**, *31*, 570–572. [CrossRef]
- 14. Hastas, N.A.; Tassis, D.H.; Dimitriadis, C.A.; Kamarinos, G. Determination of interface and bulk traps in the subthreshold region of polycrystalline silicon thin-film transistors. *IEEE Trans. Electron Dev.* **2003**, *50*, 1991–1994. [CrossRef]
- 15. Tsuji, H.; Kamakura, Y.; Taniguchi, K. Simple extraction method of interface trap density in thin-film transistors. *J. Electrochem. Soc.* **2009**, *156*, H430–H433. [CrossRef]

- Dehuff, N.L.; Kettenring, E.S.; Hong, D.; Chiang, H.Q.; Wager, J.F.; Hoffman, R.L.; Park, C.H.; Keszler, D.A. Transparent thin-film transistors with zinc indium oxide channel layer. *J. Appl. Phys.* 2005, 97, 064505. [CrossRef]
- 17. Wu, W.-J.; Chen, C.-L.; Hu, X.; Xia, X.-H.; Zhou, L.; Xu, M.; Wang, L.; Peng, J.-B. Analytical extraction method for density of states in metal oxide thin-film transistors by using low-frequency capacitance-voltage characteristics. *J. Disp. Technol.* **2016**, *12*, 888–891. [CrossRef]
- Fung, T.-C.; Chuang, C.-S.; Chen, C.; Abe, K.; Cottle, R.; Townsend, M.; Kumomi, H.; Kanicki, J. Two-dimensional numerical simulation of radio frequency sputter amorphous In-Ga-Zn-O thin-film transistors. J. Appl. Phys. 2009, 106, 084511. [CrossRef]
- 19. Migliorato, P.; Seok, M.; Jang, J. Determination of flat band voltage in thin film transistors: The case of amorphous-indium gallium zinc oxide. *Appl. Phys. Lett.* **2012**, *100*, 073506. [CrossRef]
- 20. Park, J.S.; Kim, H.; Kim, I.D. Overview of electroceramic materials for oxide semiconductor thin film transistors. *J. Electroceram.* **2014**, *32*, 117–140. [CrossRef]
- Conley, J.F. Instabilities in oxide semiconductor transparent thin film transistors. In Proceedings of the 2009 IEEE International Integrated Reliability Workshop Final Report, South Lake Tahoe, CA, USA, 18–22 October 2009; pp. 50–55.
- 22. Hsieh, H.-H.; Kamiya, T.; Nomura, K.; Hosono, H.; Wu, C.-C. Modeling of amorphous ingazno(4) thin film transistors and their subgap density of states. *Appl. Phys. Lett.* **2008**, *92*, 133503. [CrossRef]
- 23. Kimura, M.; Takizawa, T.; Inoue, S.; Shimoda, T. Analytical current-voltage model for polycrystalline-silicon thin-film transistors. *Appl. Phys. Lett.* **2002**, *80*, 2326–2328. [CrossRef]



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