

Article

# Bias Stress and Temperature Impact on InGaZnO TFTs and Circuits

Jorge Martins <sup>1</sup>, Pydi Bahubalindrani <sup>2,\*</sup>, Ana Rovisco <sup>1</sup>, Asal Kiazadeh <sup>1</sup>, Rodrigo Martins <sup>1</sup>, Elvira Fortunato <sup>1</sup> and Pedro Barquinha <sup>1,\*</sup>

<sup>1</sup> CENIMAT/I3N, Departamento de Ciência dos Materiais, Faculdade de Ciências e Tecnologia (FCT), Universidade NOVA de Lisboa (UNL) and CEMOP/UNINOVA, 2829-516 Caparica, Portugal; jds.martins@campus.fct.unl.pt (J.M.); a.rovisco@campus.fct.unl.pt (A.R.); a.kiazadeh@fct.unl.pt (A.K.); rm@uninova.pt (R.M.); emf@fct.unl.pt (E.F.)

<sup>2</sup> IIT Delhi, Okhla Industrial Estate, Phase III, New Delhi 110020, India

\* Correspondence: bpganga@iiitd.ac.in (P.Bah.); pmcb@fct.unl.pt (P.Bar.); Tel.: +91-11-26907-424 (P.Bah.)

Received: 26 April 2017; Accepted: 14 June 2017; Published: 21 June 2017

**Abstract:** This paper focuses on the analysis of InGaZnO thin-film transistors (TFTs) and circuits under the influence of different temperatures and bias stress, shedding light into their robustness when used in real-world applications. For temperature-dependent measurements, a temperature range of 15 to 85 °C was considered. In case of bias stress, both gate and drain bias were applied for 60 min. Though isolated transistors show a variation of drain current as high as 56% and 172% during bias voltage and temperature stress, the employed circuits were able to counteract it. Inverters and two-TFT current mirrors following simple circuit topologies showed a gain variation below 8%, while the improved robustness of a cascode current mirror design is proven by showing a gain variation less than 5%. The demonstration that the proper selection of TFT materials and circuit topologies results in robust operation of oxide electronics under different stress conditions and over a reasonable range of temperatures proves that the technology is suitable for applications such as smart food packaging and wearables.

**Keywords:** bias stress; a-IGZO TFTs; robust oxide TFT circuits; large-area flexible electronics

## 1. Introduction

InGaZnO thin-film transistors (IGZO TFTs) enable uniformity over large-areas, compatibility with low-cost and low-temperature fabrication techniques, and high mobility ( $>10 \text{ cm}^2/\text{V}\cdot\text{s}$ ), setting oxide TFTs as a winning alternative for flexible large area electronics (LAE) when compared to competing TFT technologies (e.g., a-Si:H and poly-Si) [1]. As a good maturity level of this transistor technology starts to be achieved, circuit design and fabrication [2–5] becomes increasingly important, enabling one to implement smart integrated systems—namely, near-field communication (NFC) smart labels [6], intelligent packaging, and systems on glass, plastic, or garments [7]. However, the continuous real-time operation of these applications demands robust circuit performance against bias stress and over a reasonable range of temperatures. Though IGZO TFTs show better stability compared to a-Si:H TFTs, several studies have demonstrated that they still show non-negligible threshold voltage ( $V_{TH}$ ) shift with respect to bias stress [8–10] and temperature [11,12].

In oxide TFTs,  $V_{TH}$  variation with gate bias stress is due to the charge trapping at the semiconductor dielectric interface or charge getting into the dielectric [8–10]. Due to the variation in total charge of the conductive channel, the drain current ( $I_{DS}$ ) of the TFT will also be changed. On the other hand, as temperature increases, mobility increases and  $V_{TH}$  tends to have a negative shift, implying that the semiconductor and hence the device are becoming more conductive. Possible causes are oxygen vacancies in the semiconductor creating additional states near conduction band and

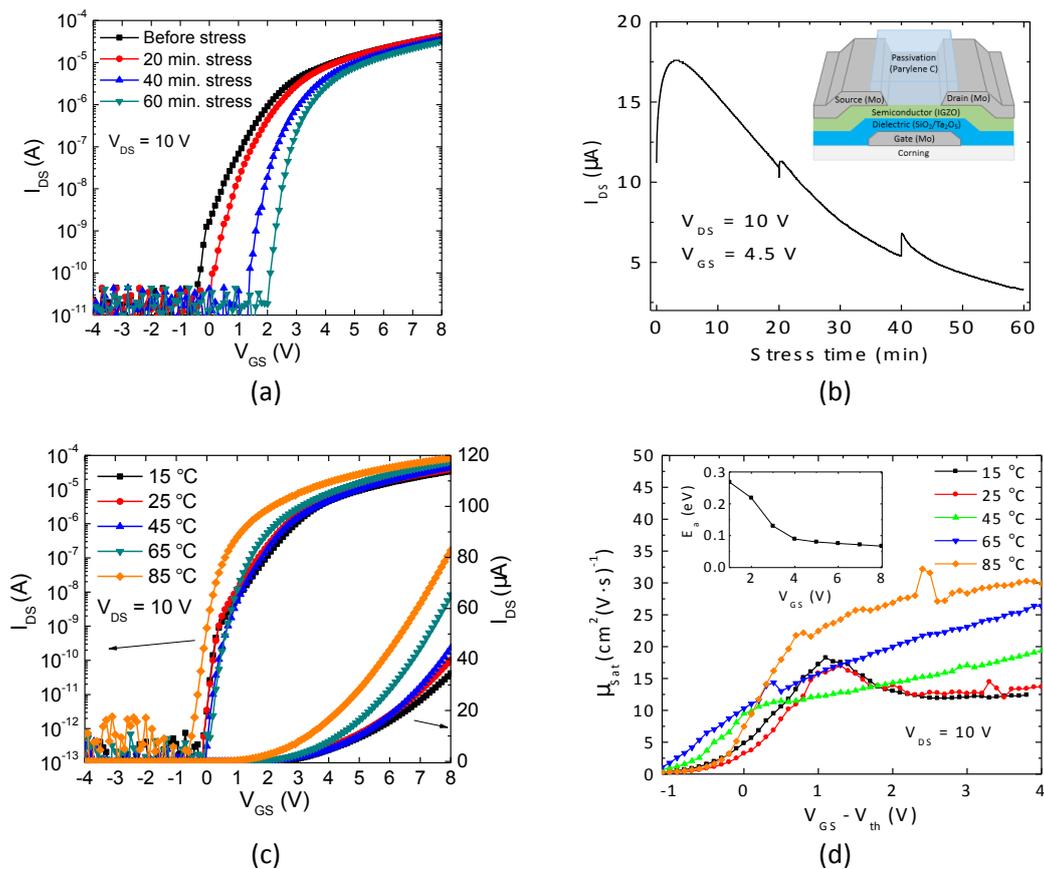
excitation of electrons due to temperature. IGZO TFTs have been analyzed under different temperature ranges to gain insights into the mechanisms controlling carrier transport. Chowdhury et al. worked in a low-temperature range (10–300 K), concluding that variable range hopping was dominant below 80 K, and that above this temperature thermally-activated band conduction would dominate [12]. Between 300 and 10 K, a  $V_{TH}$  shift as high as +8 V and saturation mobility ( $\mu_{sat}$ ) decrease from 22 to  $<1$  cm<sup>2</sup>/V·s were reported. Godo et al. have shown a  $V_{TH}$  shift  $>4$  V between 120 °C and 180 °C also for IGZO TFTs, explained by assuming two kinds of donor-like states as carrier generation sources [11].

Despite the high relevance of these studies to gain insights on device physics, the works in this area are typically based on oxide TFTs annealed at high temperatures ( $>300$  °C), which are more stable than low-temperature ones but are not compatible with low-cost flexible LAE concepts. Furthermore, reports on temperature/stress analysis of circuits based on oxide TFTs or even on other thin-film technologies are scarce. A common-source amplifier static performance with a-Si:H TFTs was reported under bias stress conditions at room temperature, the transfer characteristics of the amplifier being resistant to  $V_{TH}$  shift in the TFTs [13]. The current work presents for the first time a unified characterization of low-temperature (180 °C) oxide TFTs and circuits behavior under bias stress and temperatures ranging from 15 to 85 °C. The temperature range was selected having in mind typical storage/utilization environments of general-purpose smart packages and wearables (due to a setup limitation, it was not possible to extend the analysis to lower temperatures; still, as will be seen in the results section, smaller variation of properties are seen as temperature is decreased). From measurements, it was clear that  $I_{DS}$  has a strong dependency with temperature and bias stress. However, circuits (inverter and current mirrors) have shown a robust performance by compensating these  $I_{DS}$  shifts, even if a low-temperature oxide TFT process is used (180 °C), which leads to lower TFT performance and more device-to-device variation than what is typically obtained with high-temperature processing ( $>300$  °C).

The rest of the paper is structured as follows: Section 2 describes fabrication details of TFTs and circuits. Section 3 presents isolated TFTs stress and temperature-dependent behavior. Section 4 introduces robust circuit topologies that can cancel  $I_{DS}$  variations. Section 5 discusses the measured circuit response under bias stress and over a valid range of temperatures, and finally conclusions are drawn in Section 6.

## 2. Transistor and Circuit Fabrication and Characterization

In a  $2.5 \times 2.5$  cm<sup>2</sup> glass substrate, individual TFTs and circuits were fabricated with a staggered bottom gate structure and annealed at 180 °C. Gate, source, and drain electrodes were made of 60 nm-thick Mo deposited in an AJA ATC-1800 sputtering tool (AJA International Inc, North Scituate, MA, USA). The oxide semiconductor was a 30 nm-thick In<sub>2</sub>O<sub>3</sub>-Ga<sub>2</sub>O<sub>3</sub>-ZnO (IGZO) layer, and the dielectric layer was a 175 nm-thick multicomponent/multilayer stack based on Ta<sub>2</sub>O<sub>5</sub> and SiO<sub>2</sub>. The semiconductor and dielectric layers were deposited by RF magnetron sputtering in an AJA ATC-1300F system (AJA International Inc, North Scituate, MA, USA) without intentional substrate heating. The electrodes and the semiconductor were patterned using a liftoff process, while the dielectric was etched by reactive ion etching in a Trion Phantom 3 system with SF<sub>6</sub> atmosphere. On top of the devices and after the 180 °C annealing on a hot-plate for 1 h, a 1 μm-thick chemical vapor-deposited parylene-C (poly (monochloro-p-xylylene)) was deposited in a CVD-PDS-2010 tool (Speciality Coating Systems, Indianapolis, IN, USA). The parylene-C layer was deposited on top of an adhesion promoter consisting of Sylane A-147 from Specialty Coating to improve adhesion to IGZO. Access to gate, source, and drain pads was opened using oxygen plasma in the Trion Phantom 3 system (Trion Technology, Inc., Clearwater, FL, USA). This passivation layer improves device stability, as shown in [14,15]. All the TFTs (isolated and integrated in circuits) had a channel length (L) of 20 μm, with channel widths (W) in the range of 40 to 320 μm. A cross-sectional view of the TFT structure is presented in the inset of Figure 1b. Regarding circuits, inverter (common-source amplifier with a diode connected load), 2-TFT, and cascode current mirrors were evaluated.



**Figure 1.** Effect of (a,b) positive gate and drain bias stress and (c,d) measurement temperature on the electrical properties of  $\text{In}_2\text{O}_3\text{-Ga}_2\text{O}_3\text{-ZnO}$  (IGZO) thin-film transistors (TFTs). (a,c) show transfer characteristics; (b) shows  $I_{DS}$  evolution measured continuously during bias stress and the inset presents device structure cross sectional view; (d) shows  $\mu_{sat}$  dependence of  $V_{GS}-V_{TH}$  for the different temperatures and the inset presents activation energy with respect to the gate voltage.

Electrical characterization of the TFTs and circuits was carried out with an Agilent 4155C semiconductor parameter analyzer (Agilent Technologies, Santa Clara, CA, USA) and a Cascade Microtech M150 probe station with a ERS AC3 chuck for temperature control. All measurements and device stressing were done in the dark.

Regarding bias stress, transistors and circuits were measured before (pre-stressed state) and with a bias stress for every 20 min up to one hour. For isolated TFT,  $V_{GS}$  and  $V_{DS}$  were set to 4.5 V and 10 V, respectively. To mimic these conditions in inverters,  $V_{IN}$  of 4.5 V and  $V_{DD}$  of 10 V were used. For two-TFT current mirrors, a constant input current ( $I_{IN}$ ) of 10  $\mu\text{A}$  was supplied, while maintaining the output voltage at 10 V. For the cascode current mirror, output voltage was kept at 15 V instead. For these biasing conditions, the  $V_{GS}$  of TFTs in the current mirrors was approximately 4.5 V during stress. Regarding temperature stress, all the devices were allowed to settle at each temperature during 20 min before measurement.

### 3. Isolated TFT Behavior

#### 3.1. Stress-Dependent Behavior

Typically, oxide TFTs show positive  $V_{TH}$  shift under positive gate bias stress due to charge trapping at the semiconductor/dielectric interface or charge getting into the dielectric [8–10]. However, oxide TFTs employing high-k dielectrics can also show an anomalous trend of negative  $V_{TH}$  shift, typically attributed to charge detrapping from the dielectric and charge migration by dipole-creation [16–18].

Transfer curves measured after discrete periods of gate bias stress are presented in Figure 1a. They suggest a charge trapping mechanism only, with a  $V_{TH}$  shift of 1.29 V after 60 min stress. Further insights into the instability mechanism can be seen by analyzing the continuous  $I_{DS}$  variation during the entire stress period (Figure 1b). While a decrease of  $I_{DS}$  with time is the general trend (in agreement with the positive  $V_{TH}$  shift), an opposite behavior is verified during the first minutes of stress. This suggests that in fact the two instability mechanisms mentioned above can be present, but charge trapping tends to dominate for longer periods of stress. The small peaks visible in this plot are due to the short interruptions of bias stress for the measurement of transfer characteristics (20 min and 40 min). A detailed analysis of these competing mechanisms is currently under study.

### 3.2. Temperature-Dependent Behavior

Figure 1c shows the transfer characteristics within a temperature range of 15–85 °C. Three effects are readily observed as temperature increases: (i)  $V_{TH}$  is shifted towards negative values; (ii) maximum  $I_{DS}$  is increased; (iii) non-idealities appearing at the subthreshold region disappear. The  $V_{TH}$  and  $I_{DS}$  trends can be explained by the larger concentration of free carriers available, which escape from localized states as temperature is increased [19]. Note that the negative  $V_{TH}$  shift is not the only reason for the larger maximum  $I_{DS}$ ; in fact,  $\mu_{sat}$  is significantly enhanced as temperature increases (Figure 1d). It is interesting to notice that Chen et al. obtained a considerably smaller increase of field-effect mobility within the same temperature range on IGZO TFTs (from  $\approx 9$  to 11  $\text{cm}^2/\text{V}\cdot\text{s}$ ). This can be justified by the different temperatures used for device fabrication: Chen et al. used 300 °C, against 180 °C of our oxide TFTs. It is well known that (post-)processing temperature is one of the most important parameters in setting the quality of IGZO thin films, with lower temperatures resulting in larger density of subgap trap states, hence to more notorious thermal activation of  $\mu_{sat}$  [20,21]. This is also related to effect (iii), observed in Figure 1c and also in Figure 1d: As expected,  $E_a$  decreases with increase in  $V_{GS}$  and a minimum of 70 meV is obtained at  $V_{GS} = 8$  V from Figure 1d inset. Values lower than this are typically reported in literature for IGZO TFTs (around 26 meV) [19]. However, it should be noted again that the processing temperature of the present devices is quite low (180 °C) compared to the typical  $>300$  °C reported in literature. As shown in [20], defects close to 100–300 meV are annihilated as annealing temperature increases; hence, it would be expected that devices annealed at lower temperature would present higher  $E_a$ .

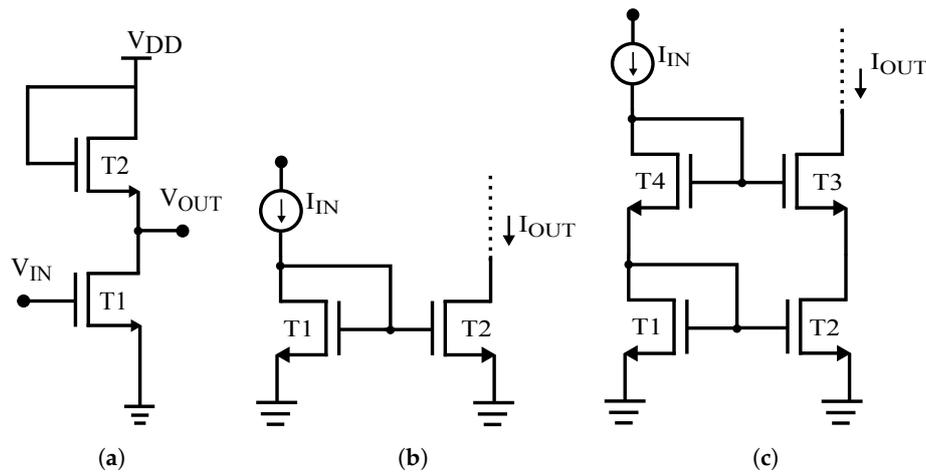
Table 1 shows measured  $I_{DS}$  with respect to stress and temperature variation, taken for  $V_{GS} = 4.5$  V and  $V_{DS} = 10$  V. Under the considered testing conditions,  $I_{DS}$  can be changed by more than 170%, as can be noticed from Table 1.

**Table 1.** Drain current variation on IGZO TFTs under different durations of gate and drain bias stress and measurement temperature.  $I_{DS}$  measured at  $V_{GS} = 4.5$  V and  $V_{DS} = 10$  V.

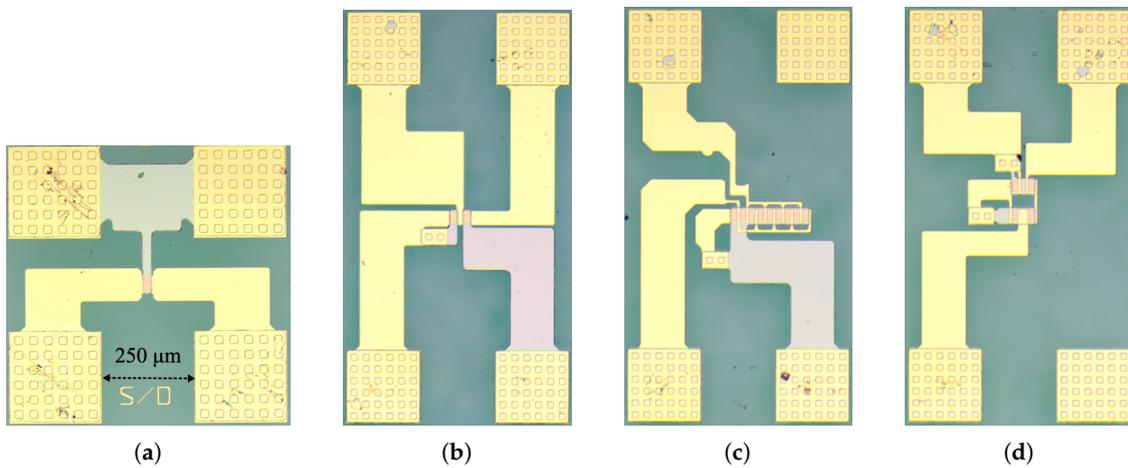
	Stress (Min.)				Temperature (°C)				
	0	20	40	60	15	25	45	65	85
$I_{DS}$ ( $\mu\text{A}$ )	11.3	10.7	6.8	5.0	6.8	8.1	7.1	11.5	21.9
Relative variation (%)	0.0	−5.2	−39.5	−56.0	−15.5	0.0	−12.2	43.3	172.3

## 4. Robust Circuits against Bias Stress and Temperature: Theoretical Analysis

When isolated TFTs show significant performance variation under external stimulus, obviously circuits and systems employing these devices tend to show degradation in their performance. Robust circuit topologies have been analyzed to infer about their ability to counteract  $I_{DS}$  variation. Circuit schematics and the corresponding micrographs are presented in Figures 2 and 3, respectively.



**Figure 2.** Circuit schematics: (a) Inverter; (b) Two-TFT current mirror; (c) Cascode current mirror.



**Figure 3.** Micrographs of (a) TFT; (b) Inverter 40–40; (c) Two-TFT current mirror with  $W_{T1} = 40 \mu\text{m}$   $W_{T2} = 320 \mu\text{m}$ ; (d) Cascode current mirror.

For the sake of simplicity, threshold voltage with respect to stress time and temperature variation is expressed as follows:

$$V_{TH}(t, T) = V_{TH0} + \Delta V_{TH}(t, T) \quad (1)$$

where  $t$  is stress time,  $T$  is temperature, and  $\Delta V_{TH}(t, T)$  is change in the threshold voltage with respect to the stress time and the temperature variation.

**Inverter:** Considering the inverter circuit (Figure 2a), from a large signal analysis perspective, when T1 and T2 are under saturation, and assuming that they have same dimensions and are well matched, (i.e., no significant variation due to process non-uniformity is verified), output voltage ( $V_{OUT}$ ) can be expressed as

$$V_{OUT} = V_{DD} - \frac{\mu_{T1}(T)}{\mu_{T2}(T)} V_{IN} - [(\Delta V_{TH}(t, T))_{T2} - \frac{\mu_{T1}(T)}{\mu_{T2}(T)} \Delta V_{TH}(t, T)_{T1}] \quad (2)$$

When T1 and T2 are exposed to same conditions (bias stress and temperature), the output signal is almost independent of the  $\Delta V_{TH}(t, T)_{T1, T2}$  and mobility variation due to temperature ( $\mu_{T1} \approx \mu_{T2}$ ).

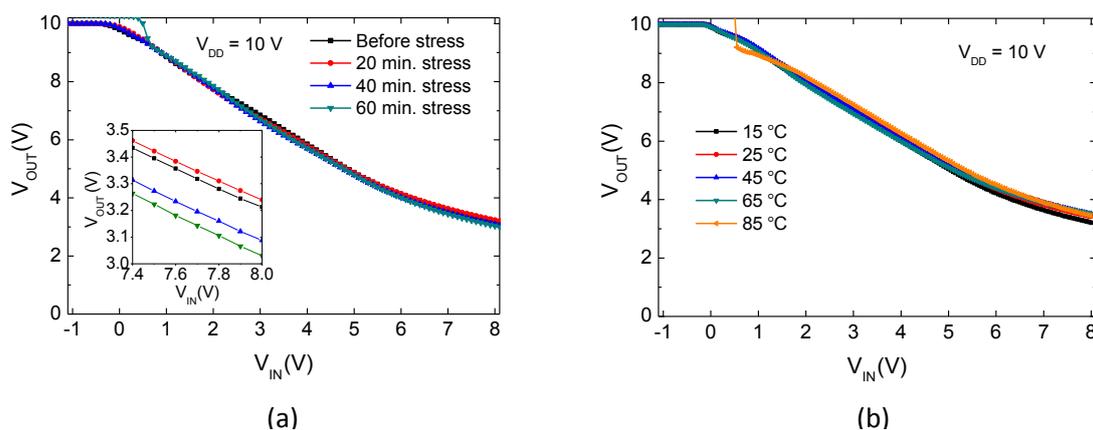
**Current Mirrors:** When the TFTs are matched, have equal channel length, and ignoring the channel length modulation due to the long L ( $=20 \mu\text{m}$ ), the input and output currents in this circuit (Figure 2b) are related by

$$\frac{I_{OUT}}{I_{IN}} = \frac{W_{T2}\mu_{T2}(T)(V_{GS} - V_{TH2})^2}{W_{T1}\mu_{T1}(T)(V_{GS} - V_{TH1})^2} \quad (3)$$

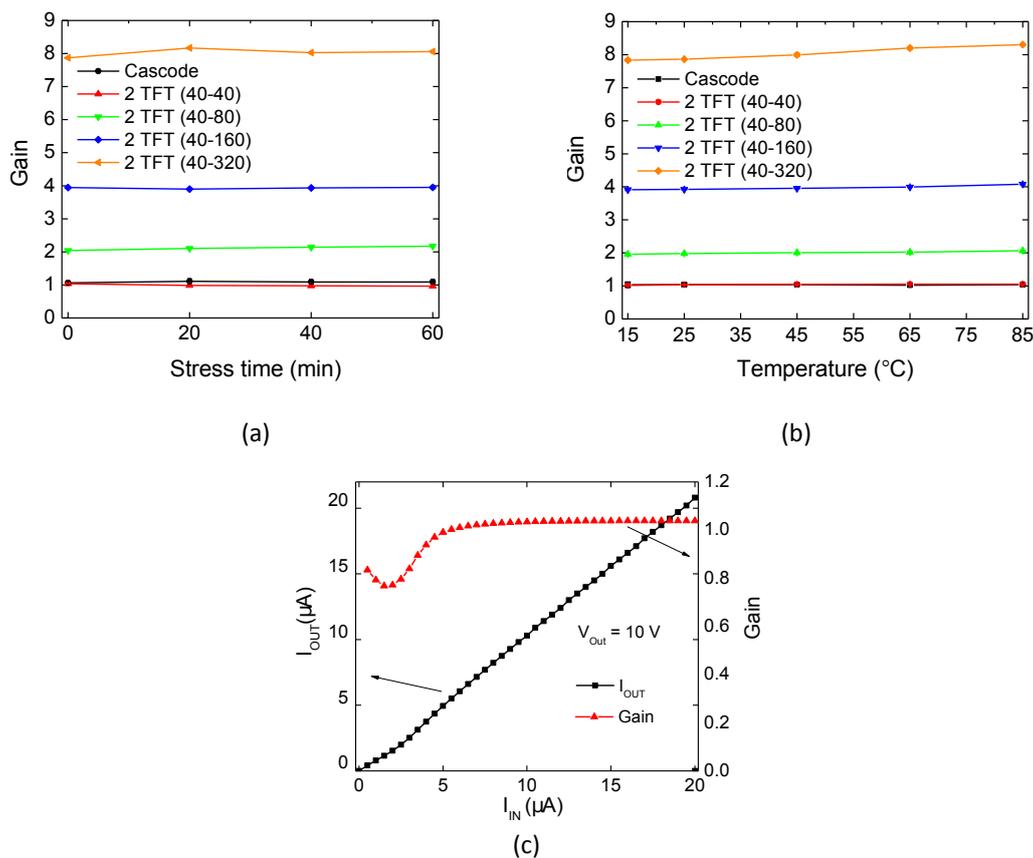
When all transistors in this circuit are exposed to the same bias stress conditions (it should be noted that  $V_{GS}$  of  $T1$  and  $T2$  are equal) and/or temperature variations,  $V_{TH}$  variation is going to be the same for both the TFTs, and hence the mirrored current is supposed to be robust against operating conditions. This circuit output resistance is equal to the output resistance of a single TFT ( $r_o$ ). Under similar conditions, the same analysis is valid for the cascode current mirror (Figure 2c), and this circuit has high accuracy because of its high output impedance ( $g_m r_o^2$ ).

## 5. Circuits Measurements and Discussion

A characterization of inverters and current mirrors under different bias stress periods and temperatures is presented in Figures 4 and 5. The gain of the inverter is approximately given by  $\sqrt{\frac{W_{T1}}{W_{T2}}}$ , when  $T1$  and  $T2$  have same channel length and good matching. A value of 0.98 was measured, which is close to unity, as expected. As is apparent from Figure 4, when the inverter circuit is subjected to bias stress or temperature, its voltage transfer characteristics are not significantly affected because  $T1$  and  $T2$  are exposed to relatively similar conditions:  $V_{TH}$  and mobility variations in one TFT should be canceled by the other, as per (2). The gain of the inverter changed by less than 8% from its original value under bias stress, and less than 5% regarding temperature, as as it can be noticed from Table 2. The inset in Figure 4a shows a magnification of the output voltage when input voltage is high ( $V_{OL}$ ). A decrease of  $\approx 0.2$  V on  $V_{OL}$  can be noticed between the unstressed state and after 60 min stress. This indicates a decrease of the driver TFT's ( $T1$ ) resistance comparatively to the load TFT ( $T2$ ) as stress time is increased. The effect can be understood by analyzing the bias stress conditions of each transistor: By fixing  $V_{IN} = V_{GST1} = 4.5$  V,  $V_{OUT} = V_{DST1} = 5.2$  V. Hence, since  $V_{DD} = 10$  V,  $V_{DST2} = V_{GST2} = 4.8$  V. With lower  $V_{GS}$  and higher  $V_{DS}$ , the  $V_{TH}$  shift for  $T1$  is smaller than for  $T2$  [22,23]. Given that close to  $V_{OL}$   $T1$  is operating in linear regime,  $R_{T1}/R_{T2}$  is decreased for longer stress periods. The small increase of  $V_{OL}$  between the unstressed state and after 20 min stress might be explained by considering that the initial period where the anomalous  $V_{TH}$  shift is predominant (Figure 1b) is found to have some variation from device to device. Hence, until the 20 min stress period, the anomalous  $V_{TH}$  shift (negative) in  $T2$  might be slightly more significant than in  $T1$ .



**Figure 4.** Transfer characteristics of IGZO TFT-based inverters under different (a) bias stress (gate + drain) periods and (b) temperatures. The inset in (a) shows a magnification at the  $V_{OL}$  region.



**Figure 5.** Mirroring ratios of IGZO TFT-based current mirrors under different (a) bias stress (gate + drain) periods and (b) measurement temperatures. A typical characteristic of a current mirror is presented in (c), showing constant gain between  $I_{IN} = 5\text{--}20\ \mu\text{A}$ .

**Table 2.** Inverter maximum gain variation with respect to bias stress and temperature variation.

	Stress (Min.)				Temperature (°C)				
	0	20	40	60	15	25	45	65	85
Gain	0.99	0.95	0.94	0.92	0.98	0.98	0.97	0.94	0.97
Relative variation (%)	0.0	−4.0	−4.9	−7.3	0.1	0.0	−1.2	−4.3	−1.3

For the current mirrors, gain with respect to bias stress and temperature is presented in Figure 5. This gain as well as its variation relative to unstressed states and room temperature measurements are reported in Table 3. Current mirrors with different  $\frac{W_2}{W_1}$  are presenting close-to-theoretical gain, without significant changes under bias stress or temperature, as expected per (3). A maximum variation below 9% was measured with increasing stress time, while for temperature variation it was always below 5%. Proving its robustness, the cascode current mirror presents higher stability than the two-TFT configurations due to its high output impedance. The presented gains are taken as an average of gain between  $I_{IN} = 5\text{--}20\ \mu\text{A}$ , with the standard deviation over this range never exceeding 2%. Figure 5c illustrates this by showing for the two-TFT (40–40) current mirror that  $I_{OUT}$  is increasing linearly with  $I_{IN}$ , resulting in a constant gain over this range. This is verified for all the current mirrors, regardless of bias stress and temperature. It should be noted that the circuits have shown a robust performance, irrespective of the unavoidable mismatches arising due to the low-temperature fabrication and different layouts of the TFTs [24] (i.e., direct and fingered layouts, see Figure 3).

**Table 3.** Current mirror average gain variation under different durations of gate + drain bias stress and measurement temperature, when  $I_{in}$  is varied from 5 to 20  $\mu\text{A}$ .

Gain	Stress (Min.)				Temperature ( $^{\circ}\text{C}$ )				
	0	20	40	60	15	25	65	45	85
Cascode	1.06	1.11	1.09	1.09	1.04	1.04	1.04	1.02	1.04
Relative variation (%)	0.0	4.7	2.8	2.8	−0.2	0.0	0.0	−1.7	0.0
40–40	1.03	0.96	0.95	0.94	1.02	1.04	1.05	1.05	1.05
Relative variation (%)	0.0	−6.6	−7.9	−8.7	−1.9	0.0	1.0	1.0	1.0
40–80	2.03	2.12	2.15	2.19	1.96	1.98	2.01	2.02	2.07
Relative variation (%)	0.0	4.1	6.0	7.6	−1.1	0.0	1.3	2.1	4.2
40–160	3.95	3.85	3.86	3.86	3.91	3.92	3.95	3.99	4.08
Relative variation (%)	0.0	−2.5	−2.4	−2.4	−0.2	0.0	0.8	1.8	4.0
40–320	7.90	8.15	7.85	7.88	7.84	7.86	7.99	8.20	8.30
Relative variation (%)	0.0	3.2	−0.6	−0.2	−0.4	0.0	1.7	4.3	5.6

## 6. Conclusions

This paper presented an application-oriented analysis of oxide TFTs under gate and drain bias stress and different measurement temperatures. The relatively large changes of  $I_{DS}$  (as high as 172%) under the more severe conditions (i.e., longer bias stress period and higher temperature) are significantly attenuated on circuits, namely inverters (or common-source amplifier with a diode-connected load) and current mirrors, given that the variations seen in one node are counteracted by the ones in other node. Thus, this work shows that even when employing low-temperature oxide TFT processes (which inherently result in higher device-to-device variation and degraded TFT stability compared to higher temperature processes), oxide TFT circuitry following simple design considerations can provide robust performance in real-world applications demanding continuous operation.

**Acknowledgments:** This work is funded by FEDER funds through the COMPETE 2020 Programme and National Funds through FCT—Portuguese Foundation for Science and Technology under the project number POCI-01-0145-FEDER-007688, Reference UID/CTM/50025. The work also has received funding from the European Community’s H2020 program under grant agreement No. 644631 (Roll-Out), No. 716510 (ERC-2016-STG TREND) and early career research grant—ECR/2017/000931.

**Author Contributions:** Asal Kiazadeh designed experiments; Ana Rovisco fabricated device/circuits and supported electrical characterization; Jorge Martins performed electrical characterization, analyzed data, and wrote the manuscript together with Pydi Bahubalindrani, who also designed the transistors and circuit layouts; Pedro Barquinha revised the concept, structure and content of the different versions of the manuscript until its final form; Rodrigo Martins and Elvira Fortunato provided the fabrication and characterization facilities and reviewed the final versions of the manuscript.

**Conflicts of Interest:** The authors declare no conflict of interest.

## Abbreviations

The following abbreviations are used in this manuscript:

a-IGZO	amorphous Indium Gallium Zinc Oxide
TFT	Thin-film Transistor
NFC	Near-field communication
a-Si:H	Hydrogenated amorphous silicon
RF	Radio Frequency
RT	Room Temperature
LAE	Large area electronics

## References

1. Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **2004**, *432*, 488–492.
2. Bahubalindrani, P.G.; Tavares, V.G.; Borme, J.; de Oliveira, P.G.; Martins, R.; Fortunato, E.; Barquinha, P. InGaZnO Thin-Film-Transistor-Based Four-Quadrant High-Gain Analog Multiplier on Glass. *Electron Device Lett.* **2016**, *37*, 419–421.
3. Ishida, K.; Shabanpour, R.; Boroujeni, B.; Meister, T.; Carta, C.; Ellinger, F.; Petti, L.; Munzenrieder, N.; Salvatore, G.; Troster, G. 22.5 dB open-loop gain, 31 kHz GBW pseudo-CMOS based operational amplifier with a-IGZO TFTs on a flexible film. In Proceedings of the Asian Solid-State Circuits Conference (A-SSCC), Kaohsiung, Taiwan, 10–12 November 2014; pp. 313–316.
4. Raiteri, D.; Torricelli, F.; Myny, K.; Nag, M.; van der Putten, B.; Smits, E.; Steudel, S.; Tempelaars, K.; Tripathi, A.; Gelinck, G.; et al. A 6 b 10 MS/s current-steering DAC manufactured with amorphous Gallium-Indium-Zinc-Oxide TFTs achieving SFDR >30 dB up to 300 kHz. In Proceedings of the International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 19–23 February 2012; pp. 314–316.
5. Bahubalindrani, P.G.; Tavares, V.G.; Fortunato, E.; Martins, R.; Barquinha, P. Novel linear analog-adder using a-IGZO TFTs. In Proceedings of the International Symposium on Circuits and Systems (ISCAS), Montréal, QC, Canada, 22–25 May 2016; pp. 2098–2101.
6. Myny, K.; Steudel, S. 16.6 Flexible thin-film NFC transponder chip exhibiting data rates compatible to ISO NFC standards using self-aligned metal-oxide TFTs. In Proceedings of the 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 31 January–4 February 2016.
7. Rogers, J.A.; Ghaffari, R.; Kim, D.H. *Stretchable Bioelectronics for Medical Devices and Systems*; Springer: Berlin, Germany, 2016.
8. Fortunato, E.; Barquinha, P.; Martins, R. Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances. *Adv. Mater.* **2012**, *24*, 2945–2986.
9. Lopes, M.; Gomes, H.L.; Medeiros, M.; Barquinha, P.; Pereira, L.; Fortunato, E.; Martins, R.; Ferreira, I. Gate-bias stress in amorphous oxide semiconductors thin-film transistors. *Appl. Phys. Lett.* **2009**, *95*, 063502.
10. Suresh, A.; Muth, J. Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors. *Appl. Phys. Lett.* **2008**, *92*, 033502.
11. Hiromichi, G.; Daisuke, K.; Shuhei, Y.; Toshinari, S.; Shunichi, I.; Hiroki, O.; Akiharu, M.; Shunpei, Y. Numerical Analysis on Temperature Dependence of Characteristics of Amorphous In-Ga-Zn-Oxide TFT. *SID Symp. Dig. Tech. Pap.* **2009**, *40*, 1110–1112.
12. Hossain Chowdhury, M.D.; Migliorato, P.; Jang, J. Low temperature characteristics in amorphous indium-gallium-zinc-oxide thin-film transistors down to 10 K. *Appl. Phys. Lett.* **2013**, *103*, 152103.
13. Sambandan, S. High-gain amplifiers with amorphous-silicon thin-film transistors. *Electron Device Lett.* **2008**, *29*, 882–884.
14. Kiazadeh, A.; Gomes, H.L.; Barquinha, P.; Martins, J.; Rovisco, A.; Pinto, J.V.; Martins, R.; Fortunato, E. Improving positive and negative bias illumination stress stability in parylene passivated IGZO transistors. *Appl. Phys. Lett.* **2016**, *109*, 051606.
15. Olziersky, A.; Barquinha, P.; Vilà, A.; Pereira, L.; Gonçalves, G.; Fortunato, E.; Martins, R.; Morante, J.R. Insight on the SU-8 resist as passivation layer for transparent Ga<sub>2</sub>O<sub>3</sub>-In<sub>2</sub>O<sub>3</sub>-ZnO thin-film transistors. *J. Appl. Phys.* **2010**, *108*, 064505.
16. Carlos, E.; Branquinho, R.; Kiazadeh, A.; Barquinha, P.; Martins, R.; Fortunato, E. UV-Mediated Photochemical Treatment for Low-Temperature Oxide-Based Thin-Film Transistors. *ACS Appl. Mater. Interfaces* **2016**, *8*, 31100–31108.
17. Xu, W.; Dai, M.; Liang, L.; Liu, Z.; Sun, X.; Wan, Q.; Cao, H. Anomalous bias-stress-induced unstable phenomena of InZnO thin-film transistors using Ta<sub>2</sub>O<sub>5</sub> gate dielectric. *J. Phys. D Appl. Phys.* **2012**, *45*, 205103.
18. Jin, J.W.; Nathan, A.; Barquinha, P.; Pereira, L.; Fortunato, E.; Martins, R.; Cobb, B. Interpreting anomalies observed in oxide semiconductor TFTs under negative and positive bias stress. *AIP Adv.* **2016**, *6*, 085321.
19. Chen, C.; Abe, K.; Kumomi, H.; Kanicki, J. Density of states of a-InGaZnO from temperature-dependent field-effect studies. *IEEE Trans. Electron Devices* **2009**, *56*, 1177–1183.
20. Kamiya, T.; Nomura, K.; Hosono, H. Present status of amorphous In-Ga-Zn-O thin-film transistors. *Sci. Technol. Adv. Mater.* **2010**, *11*, 044305.

21. Kamiya, T.; Nomura, K.; Hosono, H. Electronic structures above mobility edges in crystalline and amorphous In-Ga-Zn-O: Percolation conduction examined by analytical model. *J. Disp. Technol.* **2009**, *5*, 462–467.
22. Yang, S.; Shin, J.H.; Park, S.H.K.; Cheong, W.S.; Hwang, C.S.; Yoon, S.M.; Cho, D.H.; Ryu, M.K.; Chu, H.Y.; Cho, K.I.; et al. P-12: Stability of Nano-Crystalline ZnO and Amorphous IGZO TFTs under Bias Stress. *SID Symp. Dig. Tech. Pap.* **2009**, *40*, 1121–1123.
23. Park, S.; Cho, E.N.; Yun, I. Threshold voltage shift prediction for gate bias stress on amorphous InGaZnO thin film transistors. *Microelectron. Reliab.* **2012**, *52*, 2215–2219.
24. Bahubalindrani, P.G.; Tavares, V.G.; Barquinha, P.; Duarte, C.; de Oliveira, P.G.; Martins, R.; Fortunato, E. Transparent current mirrors with a-GIZO TFTs: Neural modeling, simulation and fabrication. *J. Disp. Technol.* **2013**, *9*, 1001–1006.



© 2017 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).