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Development of a Novel Bidirectional DC/DC Converter Topology with High Voltage Conversion Ratio for Electric Vehicles and DC-Microgrids

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Abstract: The main objective of this paper was to study a bidirectional direct current to direct current converter (BDC) topology with a high voltage conversion ratio for electric vehicle (EV) batteries connected to a dc-microgrid system. In this study, an unregulated level converter (ULC) cascaded with a two-phase interleaved buck-boost charge-pump converter (IBCPC) is introduced to achieve a high conversion ratio with a simpler control circuit. In discharge state, the topology acts as a two-stage voltage-doubler boost converter to achieve high step-up conversion ratio (48 V to 385 V). In charge state, the converter acts as two cascaded voltage-divider buck converters to achieve high voltage step-down conversion ratio (385 V to 48 V). The features, operation principles, steady-state analysis, simulation and experimental results are made to verify the performance of the studied novel BDC. Finally, a 500 W rating prototype system is constructed for verifying the validity of the operation principle. Experimental results show that highest efficiencies of 96% and 95% can be achieved, respectively, in charge and discharge states.

Keywords: bidirectional dc/dc converter (BDC); electric vehicle (EV); dc-microgrid; high voltage conversion ratio

1. Introduction

In recent years, to reduce fossil energy consumption, the development of environmentally friendly dc-microgrid technologies have gradually received attention [1–7]. As shown in Figure 1, a typical dc-microgrid structure includes a lot of power electronics interfaces such as bidirectional grid-connected converters (GCCs), PV/wind distributed generations (DGs), battery energy systems (BES), electric vehicles (EVs), and so on [4]. They connect together with a high-voltage dc-bus, so that dc home appliances can draw power directly from the dc-bus. In this system, the main function of GCCs is to maintain the dc-bus voltage constant, while in order to ensure the reliability of operation for dc-microgrids, a mass of BES can usually be accessed into the system. Electric vehicles (EVs) can also provide auxiliary power services for dc-microgrids, which makes clean and efficient battery-powered conveyance possible by allowing EVs to power and be powered by the electric utility. Usually, in dc-microgrid systems, when the voltage difference between the EV battery, BES and the dc-bus is large, a bidirectional dc/dc converter (BDC) with a high voltage conversion ratio for both buck and boost operations is required [4,7]. In the previous literatures, BDCs circuit topologies of the isolated [8–10] and non-isolated type [11–23] have been described for a variety of system applications. Isolated BDCs use the transformer to implement the galvanic isolation and to comply with the different standards. Personnel safety, noise reduction and correct operation of protection systems are the main reasons behind galvanic isolation. In contrast with isolated BDCs, non-isolated BDCs lack the galvanic isolation between two sides, however, they offer the benefits of smaller volume, high reliability, *etc.*, so they have been widely used for hybrid power system [24,25].

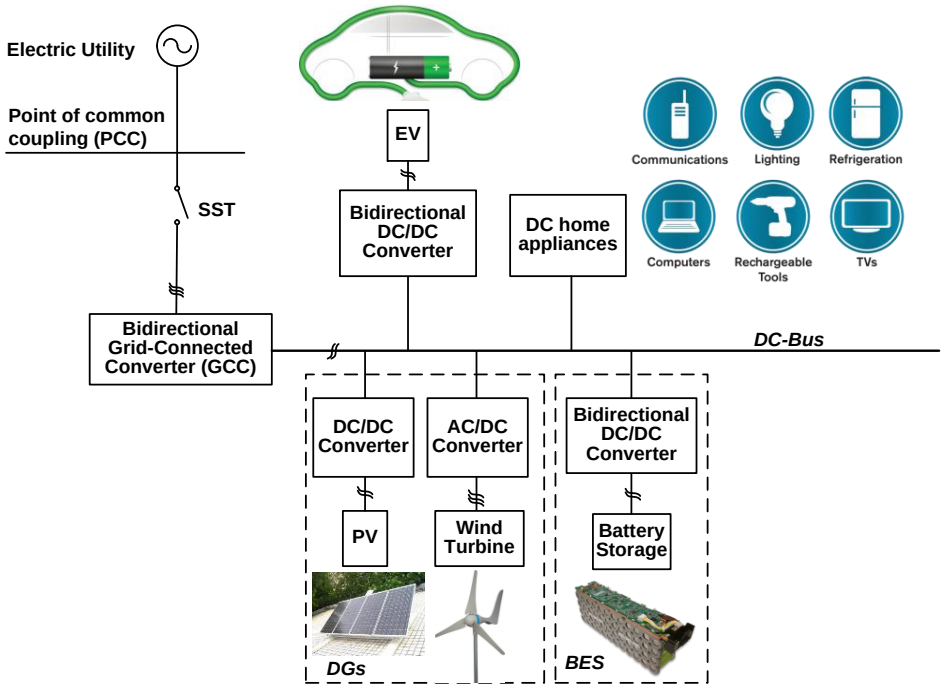

Figure 1. A typical dc-microgrid structure [4].

Compared with isolated types, BDCs with coupled-inductors for non-isolated applications possess simpler winding structures and lower conduction losses [12–17]. Furthermore, the coupled-inductor techniques can achieve easily the high voltage conversion ratio by adjusting the turn ratio of the coupled-inductor. However, the energy stored in the leakage inductor of the coupled inductor causes a high voltage spike in the power devices. Wai *et al.* [12,13] investigated a high-efficiency BDC, which utilizes only three switches to achieve the objective of bidirectional power flow. Also, the voltage-clamped technique was adopted to recycle the leakage energy so that the low-voltage stress on power switches can be ensured. To reduce the switching losses, Hsieh *et al.* proposed a high efficiency BDC with coupled inductor and active-clamping circuit [16]. In this reference, a low-power prototype was built to verify the feasibly.

As shown in Figure 2, Liang *et al.* [17] proposed a bidirectional double-boost cascaded topology for a renewable energy hybrid supply system, in which the energy is transferred from one stage to another stage to obtain a high voltage gain. Hence their conduction losses are high and it requires a large number of components.

Chen *et al.* [18] proposed a reflex-based BDC to achieve the energy recovery function for batteries connected to a low-voltage micro dc-bus system. In [18], a traditional buck-boost BDC was adopted, however, the voltage conversion ratio is limited because of the equivalent series resistance (ESR) of the inductors and capacitors and effect of the active switches [19].

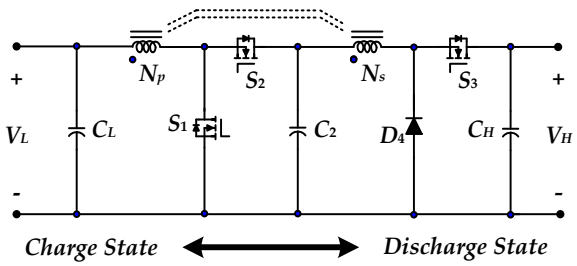

Figure 2. Circuit structure of the bidirectional double-boost cascaded topology [17].

To increase the voltage gain of the converter, the capacitors are switched and it will act as a charge-pump. The main advantage of the switched capacitor-based boost converter is that there is no need of a transformer or inductors. The main drawbacks of this topology are the complexity of the topology, high cost, low power level and high pulsating current in the input side [11,21]. In order to increase the conversion efficiency and voltage conversion ratio, multilevel combined the switched-capacitor techniques have been proposed to achieve lower stress on power devices [20–23]. As shown in Figure 3, in [22,23] two converters regulated the reasonable voltage conversion ratio with a simple pulse-width_modulation (PWM) control. However, if a high voltage conversion ratio must be provided, more power switches and capacitors are indeed required. Furthermore, although the extreme duty cycle can be avoided, the input current ripple is large due to their single-phase operation which renders these BDCs unsuitable for high current and low ripple applications.

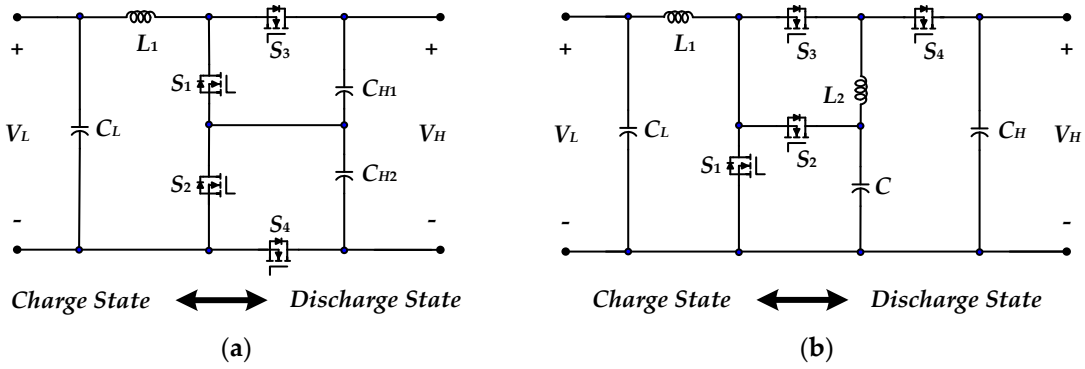

Figure 3. Two multilevel combined the switched-capacitor topologies: (**a**) circuit structure in [22]; (**b**) circuit structure in [23].

The objective of this paper is to study and develop a novel BDC for applications involving EVs connected to dc-microgrids. To meet the high current, low current ripple, and high voltage conversion ratio demands, the studied topology consists of an unregulated level converter (ULC) cascaded with a two-phase interleaved buck-boost charge-pump converter (IBCPC). In discharge state, the topology acts as a two-stage cascaded two-phase boosting converter to achieve a high step-up ratio. In charge state, the topology acts as two-stage cascaded two-phase bucking converter to achieve a high step-down ratio. The extreme duty cycle of power devices will not occur for bidirectional power flow conditions, thus not only can the output voltage regulation range be further extended but also the conduction losses can be reduced. In addition, the two-stage structure benefits reducing the voltage stress of active switches, which enables one to adopt the low-voltage rating and high performance devices, thus the conversion efficiency can be improved. The remainder of this paper is organized as follows: first, the converter topology and the operation principles of the studied BDC are illustrated in Section 2. Then, steady-state characteristic analyzes are presented in Section 3. A 500 W laboratory prototype is also constructed, and the corresponding simulation results, as well as experimental results, are provided to verify the feasibility of the studied BDC in Section 4. Finally, some conclusions are offered in the last section.

2. Proposed BDC Topology and Operation Principles

The system configuration for the studied BDC topology is depicted in Figure 4. The system contains two parts, including a ULC and a two-phase IBCPC. The major symbol representations are summarized as follows: V_H and V_L denote the high-side voltage and low-side voltage, respectively. L_1 and L_2 represent two-phase inductors of IBCPC. C_B denotes the charge-pump capacitor. C_H and C_L are the high-side and low-side capacitors, respectively. The symbols, Q_1~Q_4, and S_1~S_4, respectively, are the power switches of the IBCPC and ULC.

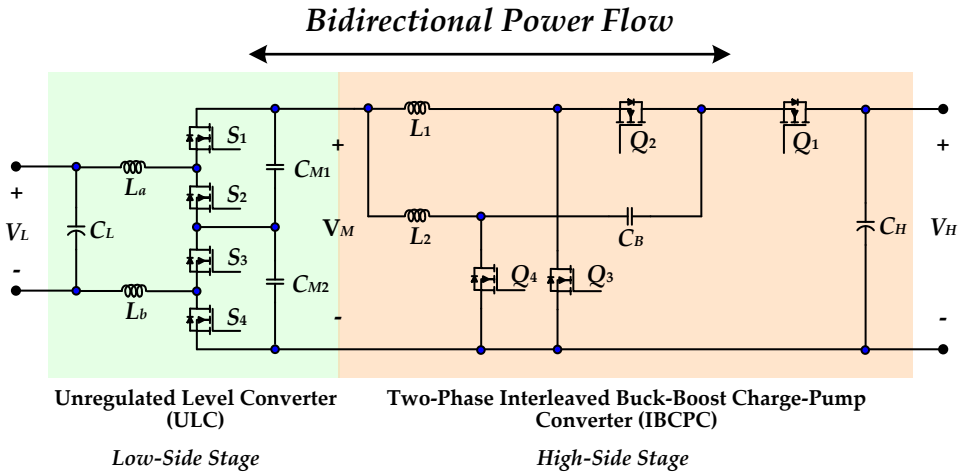

Figure 4. System configuration of the novel BDC topology.

In this study, as the low-side stage, a high efficiency magnetic-less ULC with bidirectional power flow is adopted to output a fixed voltage for a given input voltage. Because only a small sized high frequency line filter (L_a, L_b) is required, it can substantially boost the power density of the low-side stage. Furthermore, by leaving the voltage regulation to another high-side stage, the studied BDC for the low-side stage with fixed 2:1 under charge state operation or 1:2 conversion ratio under discharge state operation, can achieve high efficiency with a relatively low-side voltage in whole load range. As to the high-side stage, the structure of two-phase IBCPC is similar to a conventional buck-boost converter except two active switches in series and a charge-pump capacitor (C_B) employed in the power path. The circuit structure is simple and it can reach the high voltage conversion ratio with a reasonable duty cycle. Therefore, it can reduce the conduction loss of the switch, to further upgrade the efficiency of the whole bidirectional converter.

The studied BDC topology can deliver energy in both directions. When the energy flows from V_H to V_L, it operates in charge state (*i.e.*, buck operation); Q_1 and Q_2 are controlled to regulate the output. Thus, Q_1 and Q_2 are defined as the active switches, while Q_3 and Q_4 are the passive switches. The passive switches work as synchronous rectification (SR). When the energy flows from V_L to V_H, it operates in discharge state (*i.e.*, boost operation); Q_3 and Q_4 are controlled to regulate the output. Thus, Q_3 and Q_4 are defined as the active switches, while Q_1 and Q_2 are the passive switches.

In this study, the following assumptions are made to simplify the converter analyzes as follows: (1) the converter is operated in continuous conduction mode (CCM); (2) capacitors C_H and C_L is large enough to be considered as a voltage source; (3) the middle-link voltage $V_M = V_{M1} + V_{M2}$ is treated as a pure dc and considered as constant; (4) the two inductor L_1 and L_2 have the same inductor L_s; (5) all power semiconductors are ideal; (6) the charge-pump voltage V_{CB} is treated as a pure dc and considered as constant.

2.1. Charge State Operation

Figures 5 and 6 show the circuit configuration and characteristic waveforms of the studied BDC in charge state, respectively. It can be seen that switches Q_1 and Q_2 are driven with the phase shift angle of 180°; Q_3 and Q_4 work as synchronous rectification. In charge state, when S_1, S_3 are turned on and S_2, S_4 are turned off; or else S_2, S_4 are turned on and S_1, S_3 are turned off. The low-side voltage V_L is half the middle-link voltage V_M, *i.e.*, $V_L = 0.5V_M$. In this state, one can see that, when duty ratio of Q_1 and Q_2 are smaller than 50%, there are four operating modes according to the on/off status of the active switches.

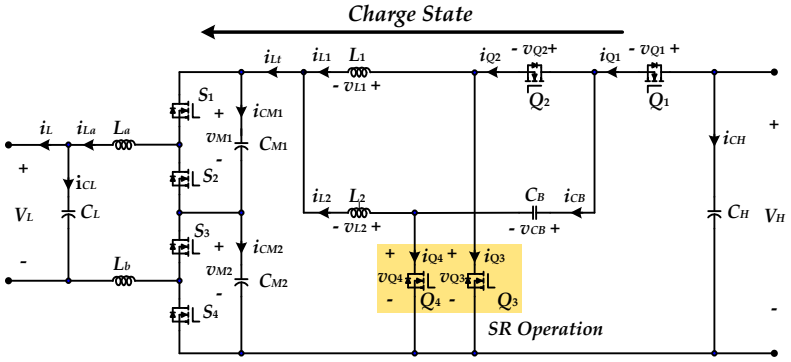

Figure 5. Circuit configuration of the studied BDC in charge state.

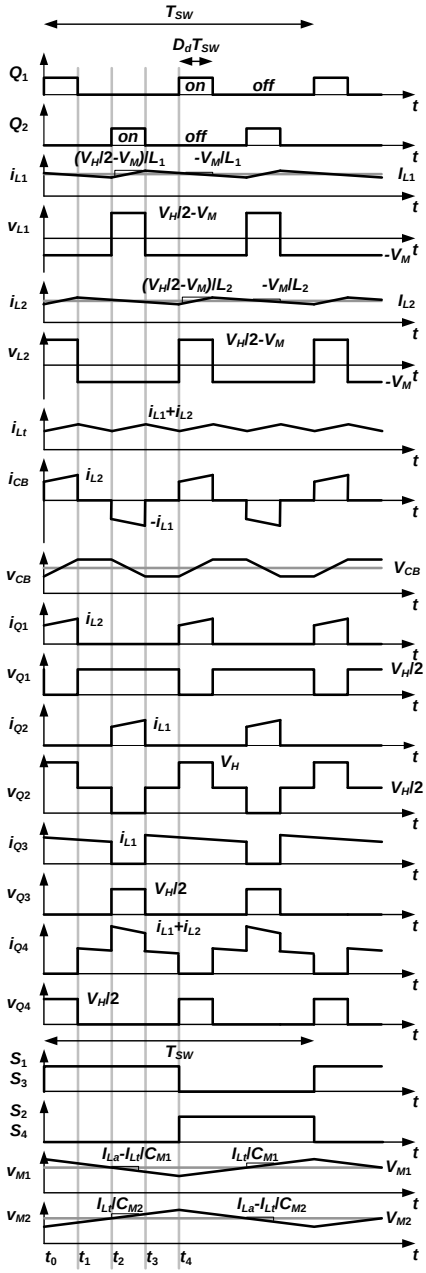

Figure 6. Characteristic waveforms of the studied BDC in charge state.

Referring to the equivalent circuits shown in Figure 7, the operating principle of the studied BDC can be explained briefly as follows.

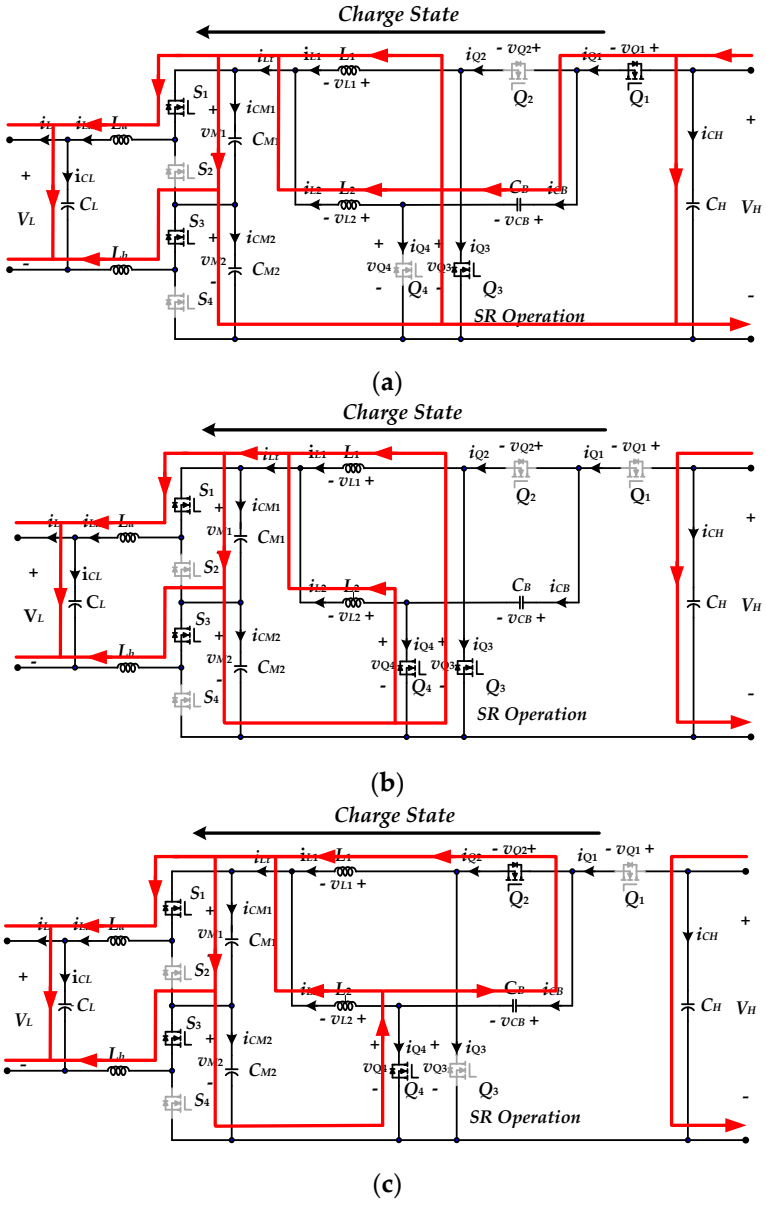

Figure 7. Equivalent circuits of the modes during different intervals in charge state: (**a**) Mode 1; (**b**) Mode 2, Mode 4; (**c**) Mode 3.

2.1.1. Mode 1 [$t_0 < t \leqslant t_1$]

The interval time is $D_d T_{sw}$, in this mode, switches Q_1, Q_3 turned on and switches Q_2, Q_4 are all off. The voltage across L_1 is the negative middle-link voltage, and hence i_{L1} decreases linearly from the initial value. Also, the voltage across L_2 is the difference of the high-side voltage V_H, the charge-pump voltage V_{CB}, and the middle-link voltage V_M, and its level is positive. The voltages across inductances L_1 and L_2 can be represented as:

$$L_1 \frac{di_{L1}}{dt} = -V_M = -2V_L \tag{1}$$

$$L_2 \frac{di_{L2}}{dt} = V_H - V_{CB} - V_M \tag{2}$$

2.1.2. Mode 2 [$t_1 < t \leqslant t_2$]

For this operation mode, the interval time is $(0.5 - D_d)T_{sw}$, switches Q_3, Q_4 are turned on and switches Q_1, Q_2 are all off. Both voltages across inductors L_1 and L_2 are the negative middle-link voltage V_M, hence i_{L1} and i_{L2} decrease linearly. The voltages across inductances L_1 and L_2 can be represented as:

$$L_1\frac{di_{L1}}{dt} = L_2\frac{di_{L2}}{dt} = -V_M = -2V_L \tag{3}$$

2.1.3. Mode 3 [$t_2 < t \leqslant t_3$]

For this operation mode, the interval time is D_dT_{sw}, switches Q_2, Q_4 are turned on and switches Q_1 and Q_3 are all off. The voltage across L_1 is the difference between the charge-pump voltage V_{CB} with the middle-link voltage V_M, and L_2 is keeping the negative middle-link voltage, the voltages across inductances L_1 and L_2 can be represented as follows:

$$L_1\frac{di_{L1}}{dt} = V_{CB} - V_M \tag{4}$$

$$L_2\frac{di_{L2}}{dt} = -V_M \tag{5}$$

2.1.4. Mode 4 [$t_3 < t \leqslant t_4$]

From this operation mode, the interval time is $(0.5 - D_d)T_{sw}$. Switches Q_3, Q_4 are turned on and switches Q_1, Q_2 are all off, and its operation is the same with that of Mode 2.

2.2. Discharge State Operation

Figures 8 and 9 show the circuit configuration and characteristic waveforms of the studied BDC in discharge state, respectively. As can be seen these figures, switches Q_3, Q_4 are driven with the phase shift angle of 180°; Q_1, Q_2 are used for the synchronous rectifier. In discharge state, when S_1, S_3 are turned on and S_2, S_4 are turned off; or else S_2, S_4 are turned on and S_1, S_3 are turned off. The low voltage V_L will charge the C_{M1} and C_{M2} to make V_{M1} and V_{M2} equal to V_L, the middle-link voltage V_M is then twice the low-side voltage V_L, *i.e.*, $V_M = 2V_L$.

Referring to the equivalent circuits shown in Figure 10, the operating principle of the studied BDC can be explained briefly as follows:

2.2.1. Mode 1 [$t_0 < t \leqslant t_1$]

The interval time is $(D_b - 0.5)T_{sw}$, switches Q_3 and Q_4 are turned on; switches Q_1 and Q_2 are all off. For the high-side stage, the middle-link voltage V_M stays between inductance L_1 and L_2, making the inductance current increase linearly, and begins to deposit energy. The voltages across inductances L_1 and L_2 can be represented as:

$$L_1\frac{di_{L1}}{dt} = L_2\frac{di_{L2}}{dt} = V_M = 2V_L \tag{6}$$

2.2.2. Mode 2 [$t_1 < t \leqslant t_2$]

In this operation mode, the interval time is $(1 - D_b)T_{sw}$. Switch Q_1, Q_3 remains conducting and Q_2, Q_4 are turned off. The voltages across inductances L_1 and L_2 can be represented as:

$$L_1\frac{di_{L1}}{dt} = V_M = 2V_L \tag{7}$$

$$L_2\frac{di_{L2}}{dt} = V_M - V_H + V_{CB} = 2V_L - V_H + V_{CB} \tag{8}$$

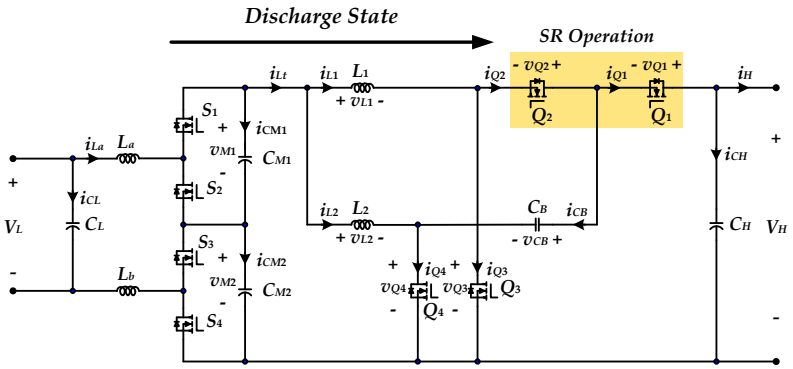

Figure 8. Circuit configuration of the studied BDC in discharge state.

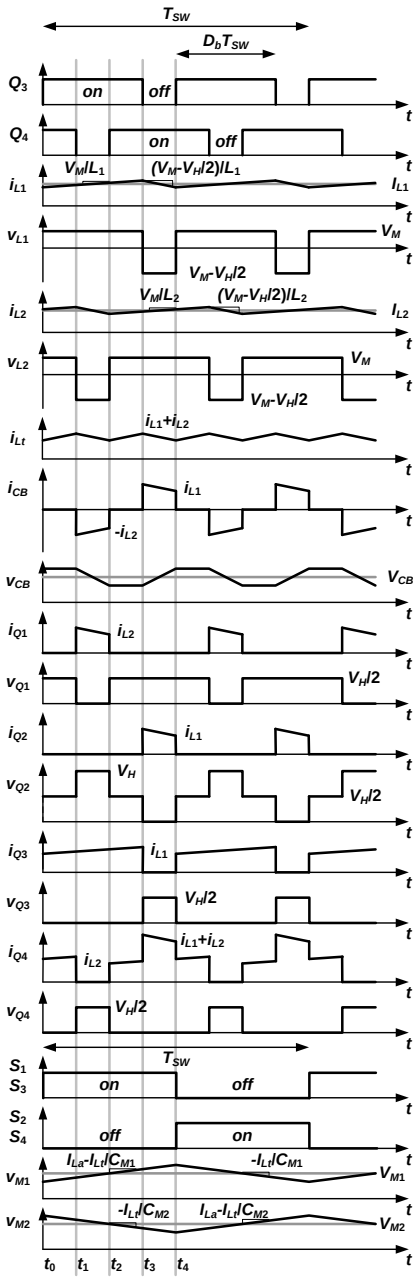

Figure 9. Characteristic waveforms of the studied BDC in discharge state.

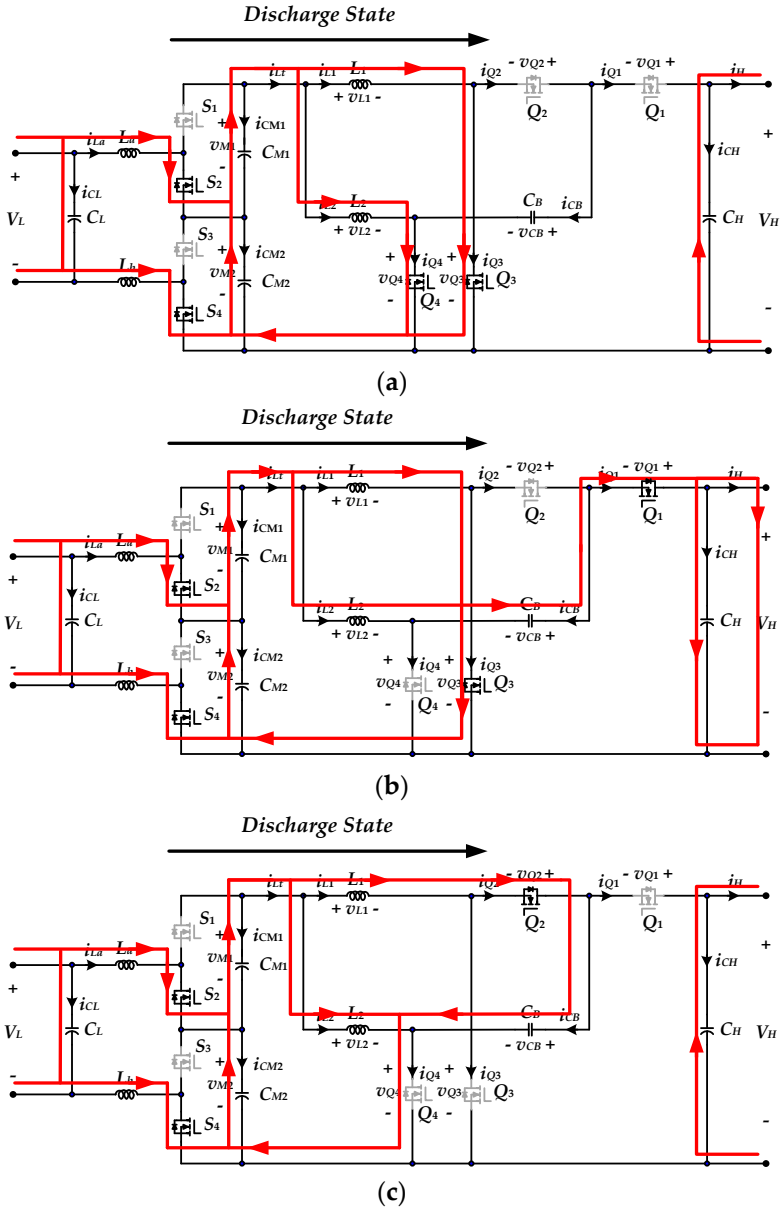

Figure 10. Equivalent circuits of the modes during different intervals in discharge state: (**a**) Mode 1, Mode 3; (**b**) Mode 2; (**c**) Mode 4.

2.2.3. Mode 3 [$t_2 < t \leqslant t_3$]

In this operation mode, the circuit operation is same as Mode 1.

2.2.4. Mode 4 [$t_3 < t \leqslant t_4$]

In this operation mode, the interval time is $(1 - D_b)T_{sw}$. For the low-side stage, switches Q_1, Q_3 are turned off and Q_2, Q_4 are turned on. The energy stored in inductor L_1 is now released energy to charge-pump capacitor C_B for compensating the lost charges in previous modes. The output power is supplied from the capacitor C_H. The voltages across inductances L_1 and L_2 can be represented as:

$$L_1 \frac{di_{L1}}{dt} = V_M - V_{CB} \tag{9}$$

$$L_2 \frac{di_{L2}}{dt} = V_M \tag{10}$$

3. Steady-State Analysis

3.1. Voltage Conversion Ratio

In charge state, V_H is the input and V_L is the output. According to Equations (1)–(5) and based on the voltage-second balance principle in L_1 and L_2, the voltage conversion ratio M_d in charge state can be derived as:

$$M_d = \frac{V_L}{V_H} = \frac{D_d}{4} \tag{11}$$

In Equation (11), D_d is the duty cycle of the active switches Q_1 and Q_2. As can be seen, the voltage conversion ratio in charge state is one-fourth of that of the conventional buck converter. Similarly, in discharge state, V_L is the input and V_H is the output. According to Equations (6)–(10) and based on the voltage-second balance principle in L_1 and L_2, the voltage conversion ratio M_b in discharge state can be derived as:

$$M_b = \frac{V_H}{V_L} = \frac{4}{1 - D_b} \tag{12}$$

where D_b is the duty cycle of the active switches Q_3 and Q_4. As can be seen, the voltage conversion ratio in discharge state is four times of that of the conventional boost converter.

Figure 11 shows that the studied BDC demands a smaller duty cycle for the active switches to produce the same voltage conversion ratio, or can produce a higher voltage conversion ratio at the same duty cycle when compared with the traditional BDC [18] and the previous BDC in [22]. Furthermore, the voltage conversion ratio of studied BDC is higher than that of the BDC proposed in [23], under a reasonable range of 25%~75% duty cycles.

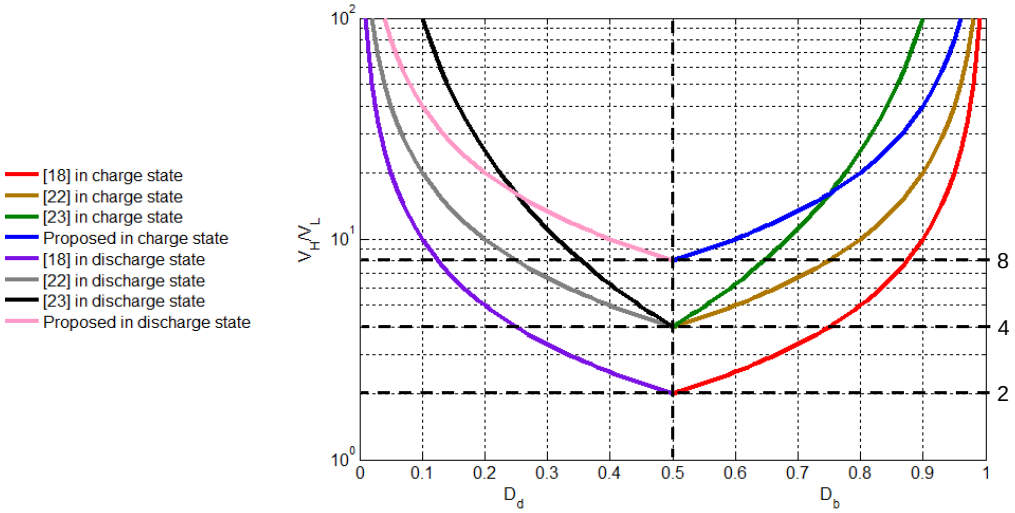

Figure 11. Comparison of voltage conversion ratios produced by the studied BDC, the converters introduced in [18,22,23].

3.2. Voltage Stress of the Switches

Whenever the ULC works as a back or front-end stage, the open circuit voltage stress on the switches S_1~S_4 of ULC is equal to the low-side input voltage V_L, as follows:

$$V_{S1,max} = V_{S2,max} = V_{S3,max} = V_{S4,max} = V_L \tag{13}$$

The particular inherent feature of the ULC benefits the low conduction losses can be achieved by adopting the low-voltage MOSFETs.

As to the high-side stage of the studied BDC, based on the aforementioned operation analyzes in Section 2, the open circuit voltage stress of switches Q_1~Q_4 can be obtained directly as:

$$V_{Q1,max} = V_{Q3,max} = V_{Q4,max} = \frac{V_H}{2} \tag{14}$$

$$V_{Q2,max} = V_H \tag{15}$$

3.3. Inductor Current Ripple

The studied BDC can operate not only in charge state but also in discharge state. Thus, the inductor can be calculated in either charge or discharge state. According to Equations (1)–(5), the total ripple current of the inductor of the studied BDC in charge state can be expressed as:

$$\Delta i_{Lt}|_{charge} = \frac{V_H T_{sw}}{L_s}(0.5 - D_d)D_d \tag{16}$$

Similarly, in discharge state, according to Equations (6)–(10), the total ripple current of the inductor of the studied BDC in discharge state can be expressed as:

$$\Delta i_{Lt}|_{discharge} = \frac{V_H T_{sw}}{L_s}(D_b - 0.5)(1 - D_b) \tag{17}$$

Figure 12 shows the normalized ripple current of the inductor of the studied BDC, the traditional BDC [18], and previous BDCs in [22,23], where the inductor and the switching frequency of these three BDCs are equal, respectively. The ripple current of the traditional BDC at 50% duty cycle is normalized as one.

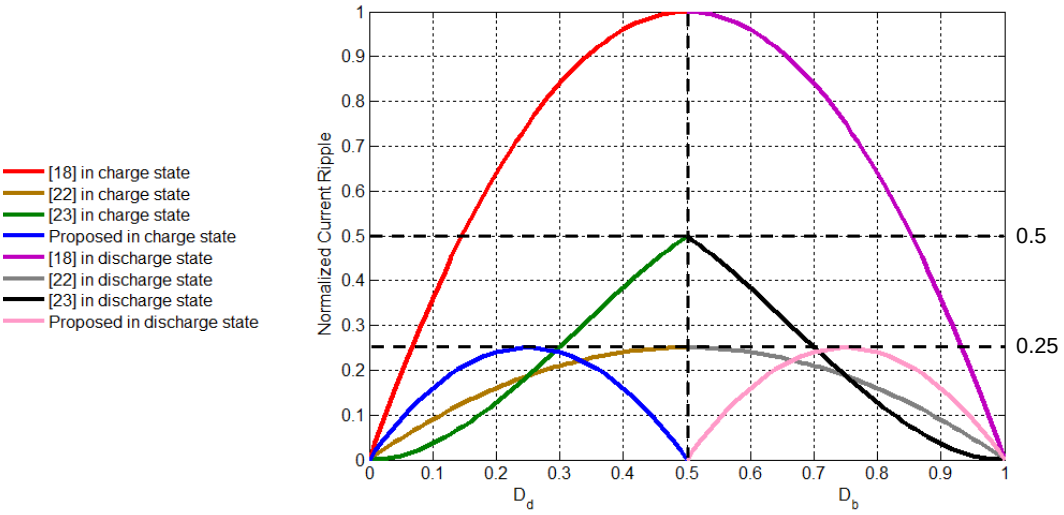

Figure 12. Comparison of the normalized ripple current of the inductor among the studied BDC, the converters introduced in [18,22,23].

It can be seen that from Figure 12, the maximum ripple current of the inductor of studied BDC is only one-fourth of that of a traditional BDC. On the other and, if the ripple currents are equal, the inductor of the studied BDC is only one-fourth of that of traditional BDC [18], which means that the studied BDC has a better dynamic response. From Figure 12, the ripple current of studied BDC is smaller than that of the converter in [22], under a reasonable range of 35%~65% duty cycles. Furthermore, the ripple current of the previous BDC proposed in [23] is higher than that of the one proposed in this study, under a reasonable range of 30%~70% duty cycles.

3.4. Boundary Conduction Mode

The boundary normalized inductor time constant $\tau_{L,B}$ can be defined as:

$$\tau_{L,B} = \frac{L_s f_{sw}}{R} \tag{18}$$

where R is low-side input equivalent resistance.

During boundary conduction mode (BCM), the input current BDC can be derived as:

$$I_L = \frac{4V_L}{L_s f_{sw}}(1 - D_d) \tag{19}$$

Substituting Equation (19) into (18), the boundary normalized time constant in charge state can be expressed as:

$$\tau_{Ld,B} = 4(1 - D_d) \tag{20}$$

Similarly, in discharge state, the input current of the studied BDC can be obtained as:

$$I_L = \frac{4V_L}{L_s f_{sw}} D_b \tag{21}$$

The boundary normalized time constant in discharge state can be expressed as:

$$\tau_{Lb,B} = 4D_b \tag{22}$$

Figure 13 shows the plots of boundary normalized inductor time constant curves $\tau_{Ld,B}$ and $\tau_{Lb,B}$ in charge and discharge states. The BDC in charge state operates in CCM when τ_{Ld} is designed to be higher than the boundary curve of $\tau_{Ld,B}$. The studied BDC in discharge state operates in discontinuous conduction mode (DCM) when τ_{Lb} is selected to be lower than the boundary curve of $\tau_{Lb,B}$.

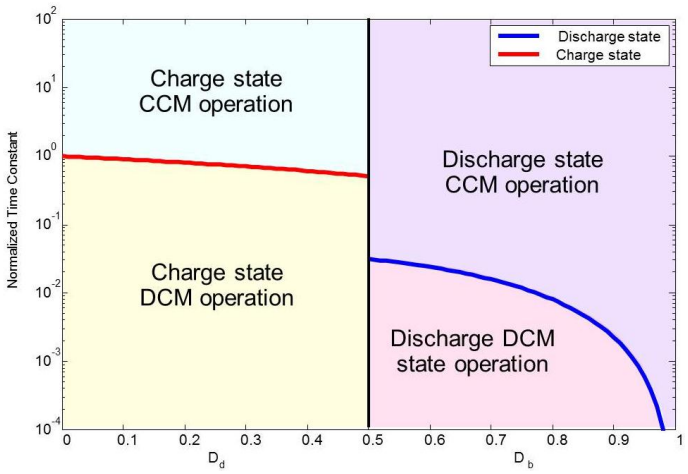

Figure 13. Normalized boundary inductances time constant in charge and discharge states.

Figure 14 shows the boundary inductances curve of the studied BDC in charge and discharge states. If the inductance is selected to be larger than the boundary inductance, the studied BDC will operate in CCM. The studied BDC can operate not only in charge state but also in discharge state, the boundary inductance can be derived as below from Equations (19) and (21), respectively.

$$L_{d,B} = \frac{4\,(1 - D_d)}{f_{sw}} \frac{V_L^2}{P_{out}} \tag{23}$$

$$L_{b,B} = \frac{4D_b}{f_{sw}} \frac{V_L^2}{P_{out}} \tag{24}$$

where P_{out} is the output power.

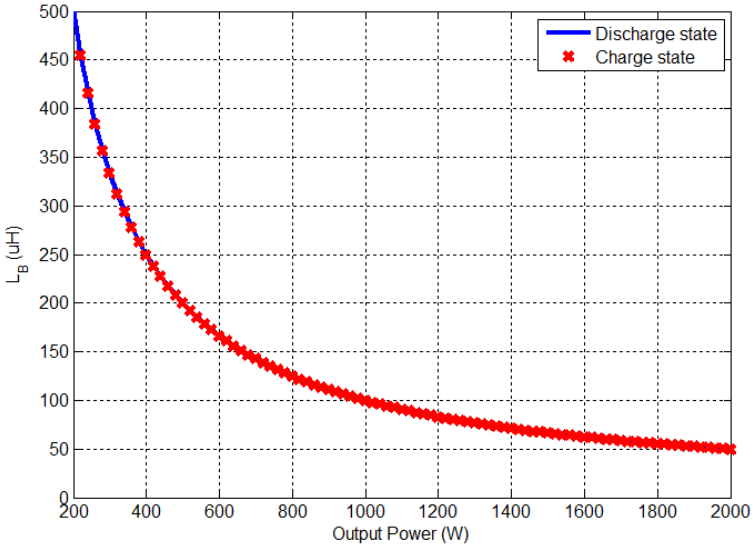

Figure 14. Boundary inductances in various power conditions.

3.5. Selection Considerations of Charge-Pump Capacitor

For the proposed BDC in charge state operation, the ripple voltage of the charge-pump capacitor C_B can be obtained as follows:

$$\Delta V_{CB} = \frac{1}{C_B}\int_{t_0}^{t_1} i_{CB}(t)dt = \frac{I_{Lt}D_d}{2C_B f_{sw}} \cong \frac{I_L D_d}{4C_B f_{sw}} \tag{25}$$

where:

$$i_{CB}(t) = \frac{I_L}{4} - \frac{\Delta i_{ripple}}{2} + \frac{0.5V_H - 2V_L}{L_s f_{sw}}(t - t_0) \tag{26}$$

$$\Delta i_{ripple} = \frac{0.5V_H - 2V_L}{L_s f_{sw}}(t_1 - t_0), t_1 = D_d T_{sw} + t_0 \tag{27}$$

From Equation (25), it is known that although a capacitor with low capacitance is used for charge-pump capacitor C_B, the voltage ripple can be reduced by increasing the switching frequency. The root mean square (RMS) value of the current through the charge-pump capacitor is

$$I_{CB(RMS)} = \sqrt{\frac{2}{f_{sw}}\int_{t_0}^{t_1} i_{CB}^2(t)dt} \cong \frac{I_L}{4}\sqrt{2D_d} \tag{28}$$

3.6. Summaries of Component Stress and Loss

For stress and loss analysis, it is assumed that the studied BDC operates with $D_d < 0.5$ and $D_b > 0.5$ for charge and discharge modes, respectively. The results of component stress can be summarized as in Table 1. Furthermore, equations for loss analysis can be summarized as in Table 2, where Q_g represents the MOSFET total gate charge; t_r is rise time, it's the period after the v_{GS} reaches threshold voltage $v_{GS(\text{th})}$ to complete the transient MOSFET gate charge; t_f is fall time, it's the time where the gate voltage reaches the threshold voltage $v_{GS(\text{th})}$ after MOSFET turn-off delay time [26].

Table 1. Stress analysis results at steady-state.

Items	Charge State	Discharge State
Voltage Stress of Q_1, Q_3, Q_4 (v_{Q1}, v_{Q3}, v_{Q4})	$0.5V_H$	$0.5V_H$
Voltage Stress of Q_2 (v_{Q2})	V_H	V_H
Voltage Stress of S_1~S_4 (v_{S1}~v_{S4})	V_L	V_L
RMS Current Stress of Q_1 (i_{Q1})	$I_{L2(\mathrm{RMS})}\sqrt{D_d}$	$I_{L2(\mathrm{RMS})}\sqrt{1-D_b}$
RMS Current Stress of Q_2 (i_{Q2})	$I_{L1(\mathrm{RMS})}\sqrt{D_d}$	$I_{L1(\mathrm{RMS})}\sqrt{1-D_b}$
RMS Current Stress of Q_3 (i_{Q3})	$I_{L1(\mathrm{RMS})}\sqrt{1-D_d}$	$I_{L1(\mathrm{RMS})}\sqrt{D_b}$
RMS Current Stress of Q_4 (i_{Q4})	$\sqrt{\begin{matrix}(I_{Lt(\mathrm{RMS})})^2(D_d)+\\(I_{L2(\mathrm{RMS})})^2(0.5-D_d)\end{matrix}}$	$\sqrt{\begin{matrix}(I_{Lt(\mathrm{RMS})})^2(1-D_b)+\\(I_{L2(\mathrm{RMS})})^2(D_b-0.5)\end{matrix}}$
RMS Current Stress of S_1~S_4 (i_{S1}~i_{S4})	$I_{Lt(RMS)}/\sqrt{2}$	$I_{Lt(RMS)}/\sqrt{2}$
RMS Current Stress of L_1 (i_{L1})	$\sqrt{{I_{L1}}^2+(\frac{\Delta i_{L1}}{2\sqrt{3}})}$	$\sqrt{{I_{L1}}^2+(\frac{\Delta i_{L1}}{2\sqrt{3}})}$
RMS Current Stress of L_2 (i_{L2})	$\sqrt{{I_{L2}}^2+(\frac{\Delta i_{L2}}{2\sqrt{3}})}$	$\sqrt{{I_{L2}}^2+(\frac{\Delta i_{L2}}{2\sqrt{3}})}$
RMS Current Stress of L_a (i_{L}a)	$\sqrt{{I_{La}}^2+(\frac{\Delta i_{La}}{2\sqrt{3}})}$	$\sqrt{{I_{La}}^2+(\frac{\Delta i_{La}}{2\sqrt{3}})}$
RMS Current Stress of L_b (i_{L}b)	$\sqrt{{I_{Lb}}^2+(\frac{\Delta i_{Lb}}{2\sqrt{3}})}$	$\sqrt{{I_{Lb}}^2+(\frac{\Delta i_{Lb}}{2\sqrt{3}})}$
RMS Current Stress of C_B (i_{CB})	$\left(I_L\sqrt{2D_d}\right)/4$	$\left(I_L\sqrt{2(1-D_b)}\right)/4$
RMS Current Stress of C_H (i_{CH})	$\sqrt{(I_{Q1(RMS)})^2-I_H}$	$\sqrt{(I_{Q1(RMS)})^2-I_H}$
RMS Current Stress of C_L (i_{CL})	$\sqrt{{I_L}^2-\frac{4\Delta i_{La}I_L}{\pi}+\frac{4{\Delta i_{La}}^2}{\pi^2}+\frac{{\Delta i_{La}}^2}{2}}$	$\sqrt{{I_L}^2-\frac{4\Delta i_{La}I_L}{\pi}+\frac{4{\Delta i_{La}}^2}{\pi^2}+\frac{{\Delta i_{La}}^2}{2}}$
RMS Current Stress of C_{M1}, C_{M2} (i_{CM1}, i_{CM2})	$\sqrt{{I_{Lt(RMS)}}^2-{I_{S1(RMS)}}^2}$	$\sqrt{{I_{Lt(RMS)}}^2-{I_{S2(RMS)}}^2}$

Table 2. Loss equations at steady-state.

Items	Equations
Conduction loss of Q_1~Q_4	$R_{DS(\mathrm{Q1})}\times[i_{Q1(RMS)}]^2$; $R_{DS(\mathrm{Q2})}\times[i_{Q2(RMS)}]^2$; $R_{DS(\mathrm{Q3})}\times[i_{Q3(RMS)}]^2$; $R_{DS(\mathrm{Q4})}\times[i_{Q4(RMS)}]^2$
Conduction loss of S_1~S_4	$R_{DS(\mathrm{S1})}\times[i_{S1(RMS)}]^2$; $R_{DS(\mathrm{S2})}\times[i_{S2(RMS)}]^2$; $R_{DS(\mathrm{S3})}\times[i_{S3(RMS)}]^2$; $R_{DS(\mathrm{S4})}\times[i_{S4(RMS)}]^2$
Switching loss of Q_1	$(V_{DS(\mathrm{Q1})}\times i_{Q1(ON)}\times T_r)/6T_{sw}$; $(V_{DS(\mathrm{Q1})}\times i_{Q1(OFF)}\times T_f)/6T_{sw}$
Switching loss of Q_2	$(V_{DS(\mathrm{Q2})}\times i_{Q2(ON)}\times T_r)/6T_{sw}$; $(V_{DS(\mathrm{Q2})}\times i_{Q2(OFF)}\times T_f)/6T_{sw}$
Switching loss of Q_3	$(V_{DS(\mathrm{Q3})}\times i_{Q3(ON)}\times T_r)/6T_{sw}$; $(V_{DS(\mathrm{Q3})}\times i_{Q3(OFF)}\times T_f)/6T_{sw}$
Switching loss of Q_4	$(V_{DS(\mathrm{Q4})}\times i_{Q4(ON)}\times T_r)/6T_{sw}$; $(V_{DS(\mathrm{Q4})}\times i_{Q4(OFF)}\times T_f)/6T_{sw}$
Switching loss of S_1	$\left(V_{DS(\mathrm{S1})}\times i_{S1(ON)}\times T_r\right)/6T_{sw}$; $(V_{DS(\mathrm{S1})}\times i_{S1(OFF)}\times T_f)/6T_{sw}$
Switching loss of S_2	$(V_{DS(\mathrm{S2})}\times i_{S2(ON)}\times T_r)/6T$; $\left(V_{DS(\mathrm{S2})}\times i_{S2(OFF)}\times T_f\right)/6T$
Switching loss of S_3	$(V_{DS(\mathrm{S3})}\times i_{S3(ON)}\times T_r)/6T_{sw}$; $(V_{DS(\mathrm{S3})}\times i_{S3(OFF)}\times T_f)/6T_{sw}$
Switching loss of S_4	$(V_{DS(\mathrm{S4})}\times i_{S4(ON)}\times T_r)/6T_{sw}$; $(V_{DS(\mathrm{S4})}\times i_{S4(OFF)}\times T_f)/6T_{sw}$
Conduction loss of L_1~L_2	$R_{L1}\times[i_{L1(RMS)}]^2$; $R_{L2}\times[i_{L2(RMS)}]^2$
Conduction loss of L_a~L_b	$R_{La}\times[i_{La(RMS)}]^2$; $R_{Lb}\times[i_{Lb(RMS)}]^2$
Conduction loss of C_B, C_H, C_L	$R_{CB}\times[i_{CB(RMS)}]^2$; $R_{CH}\times[i_{CH(RMS)}]^2$; $R_{CL}\times[i_{CL(RMS)}]^2$
Conduction loss of C_{M1}~ C_{M2}	$R_{CM1}\times[i_{CM1(RMS)}]^2$; $R_{CM2}\times[i_{CM2(RMS)}]^2$
Gate driving loss of Q_1~Q_4	$Q_{g(Q1\sim Q4)}\times V_{GS(Q1\sim Q4)}\times f_{sw}$
Gate driving loss of S_1~S_4	$Q_{g(S1\sim S4)}\times V_{GS(S1\sim S4)}\times f_{sw}$

4. Simulation and Experimental Results

In order to illustrate the performance of the studied BDC, a laboratory prototype circuit is simulated and experimented. To avoid all elements suffer from high-current stress at DCM operation, resulting in high conduction and core losses. The studied BDC operates at CCM, and its parameters and specifications of the constructed hardware prototype are given as below:

(1) high-side voltage V_H: 385 V;
(2) low-side voltage V_L: 48 V;
(3) rated power P_o: 500 W;

(4) switching frequency f_{sw}: 20 kHz;
(5) capacitors $C_H = C_L = 33$ μF, $C_{M1} = C_{M2} = 33$ μF, $C_B = 10$ μF; (ESR of C_H, $R_{CH} = 0.064$ Ω; ESR of C_L, $R_{CL} = 0.062$ Ω, ESR of C_{M1}, $R_{CM1} = 0.16$ Ω; ESR of C_{M2}, $R_{CM2} = 0.16$ Ω; ESR of C_B, $R_{CB} = 0.062$ Ω);
(6) inductors $L_1 = L_2 = L_s = 800$ μH; $L_a = L_b = 1.5$ μH (IHLP-6767GZ-A1); (ESR of L_1, $R_{L1} = 0.18$ Ω, ESR of L_2, $R_{L2} = 0.18$ Ω, ESR of L_a, $R_{La} = 13.6$ mΩ; ESR of L_b, $R_{Lb} = 13.6$ mΩ);
(7) power switches S_1~S_4: IXFH160N15T2, 150 V/160 A/$R_{DS(on)}$ = 9 mΩ, TO-247AC; Q_1, Q_3, Q_4: FDA59N30, 300 V/59 A/$R_{DS(on)}$ = 56 mΩ, TO-247AC; Q_2: W25NM60, 650 V/21 A/$R_{DS(on)}$ = 160 mΩ, TO-247AC.

Figure 15 show the simulated low-side filter currents (i_{La}, i_{Lb}), gate signals of active switches (Q_1, Q_2) and two-phase inductor currents (i_{L1}, i_{L2}) in charge state at full load condition. Also the corresponding experimental results are shown in Figure 16. One can observe that both results are in very close agreement as well. From Figures 15a and 16a, as can be seen, the low-side filter (L_a, L_b) can effectively limit the switching current spike and shape the current to a nearly rectified sinusoidal waveform. Also, from the figures it is observed that by interleaved controlling the duty cycles of 0.48 for the switches (Q_1, Q_2), the two-phase currents (i_{L1}, i_{L2}) are in complementary relation and in CCM.

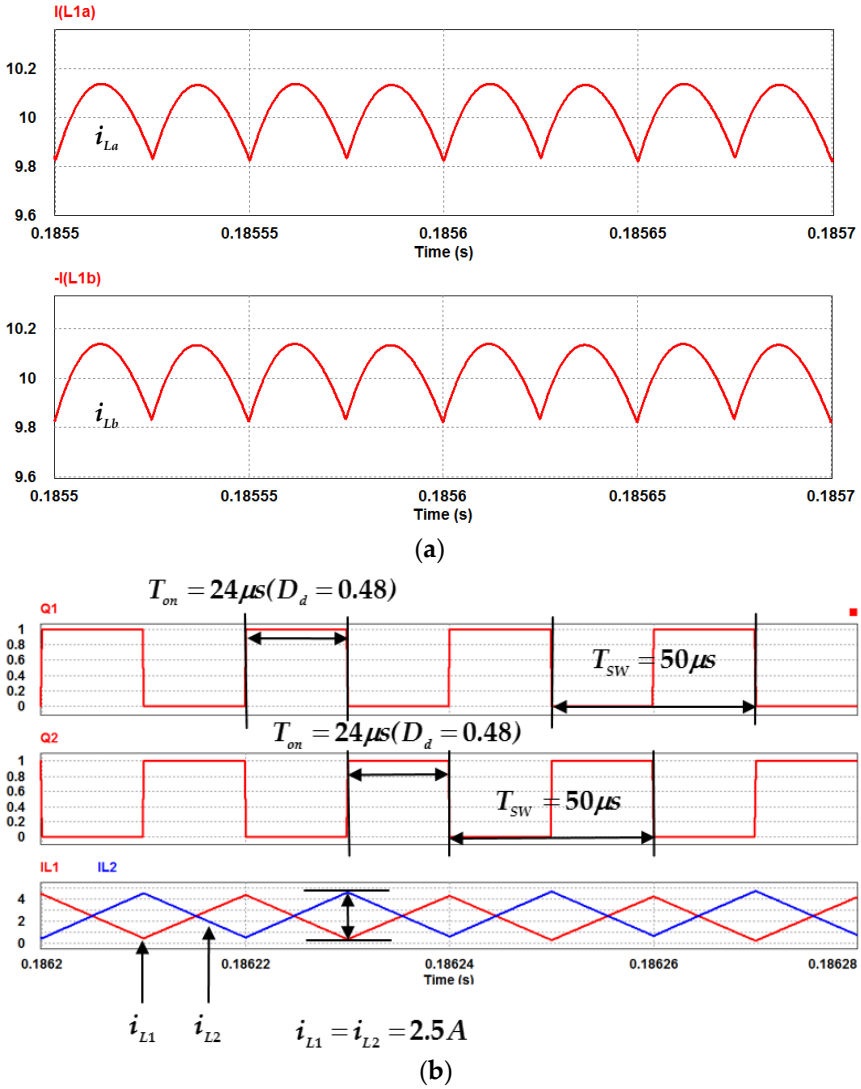

Figure 15. Simulated waveforms of the studied BDC in charge state at full load: (**a**) low-side filter currents i_{La}, i_{Lb}; (**b**) gate signals of Q_1, Q_2 and two-phase inductor currents i_{L1}, i_{L2}.

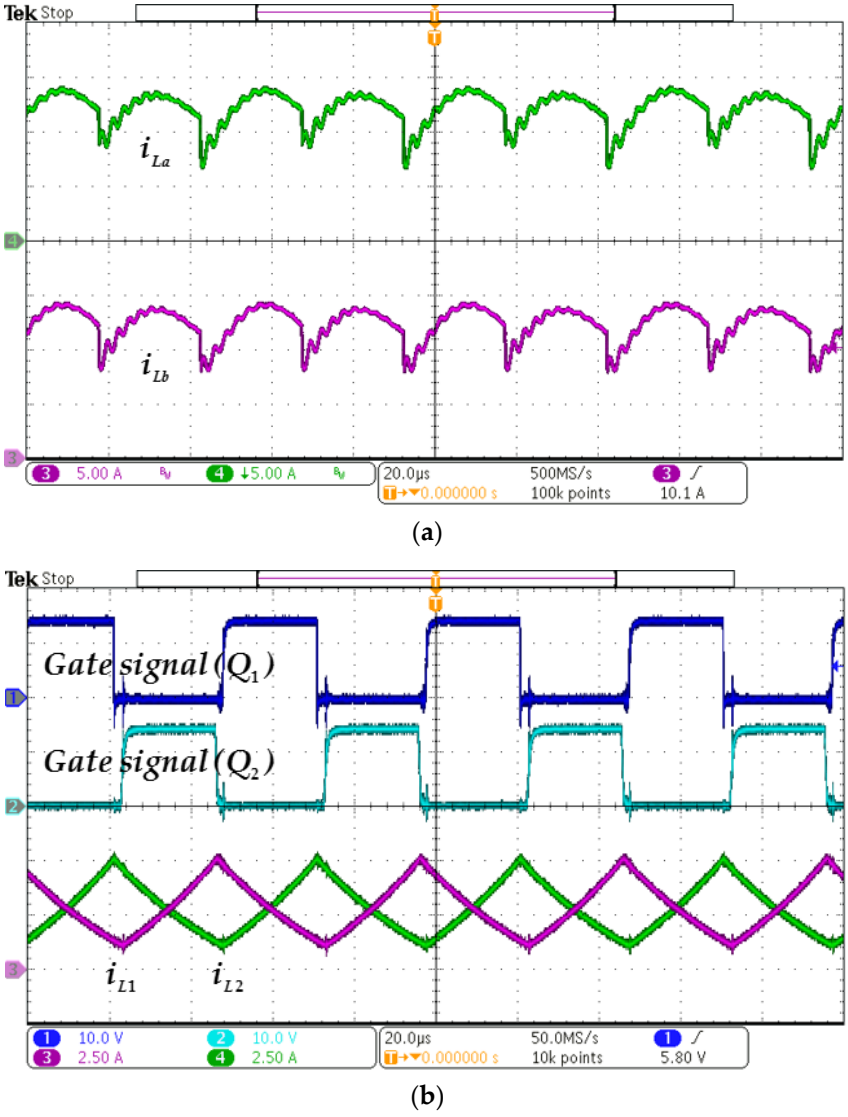

Figure 16. Measured waveforms of the studied BDC in charge state at full load: (**a**) low-side filter currents i_{La}, i_{Lb}; (**b**) gate signals of Q_1, Q_2 and two-phase inductor currents i_{L1}, i_{L2}.

Figures 17 and 18 show the simulated and measured waveforms of charge-pump capacitor voltage (V_{CB}), middle-link voltage (V_M), middle-link capacitor voltages (V_{M1}, V_{M2}), low-side voltage (V_L), and low-side switch voltages (V_{S1}, V_{S2}, V_{S3}, V_{S4}). From Figures 17 and 18 with the ULC of studied BDC, the low-voltage side (V_L) is well regulated at 48 V. The middle-link voltage is 96 V, it does quite reach twice of the regulated low-side voltage (V_L) of 48 V. The charge-pump capacitor voltage (V_{CB}) of 192 V can be achieved easily and indeed can share one-half of the high-side voltage to reduce the voltage stress of active switches. It is observed that the steady-state voltage stresses of low-side active switches (V_{S1}, V_{S2}, V_{S3}, V_{S4}) are only about 48 V, which means that lower on-resistance MOSFETs can be used to achieve the improved conversion efficiency. Also, both the simulated results are in close agreement with the corresponding experimental results.

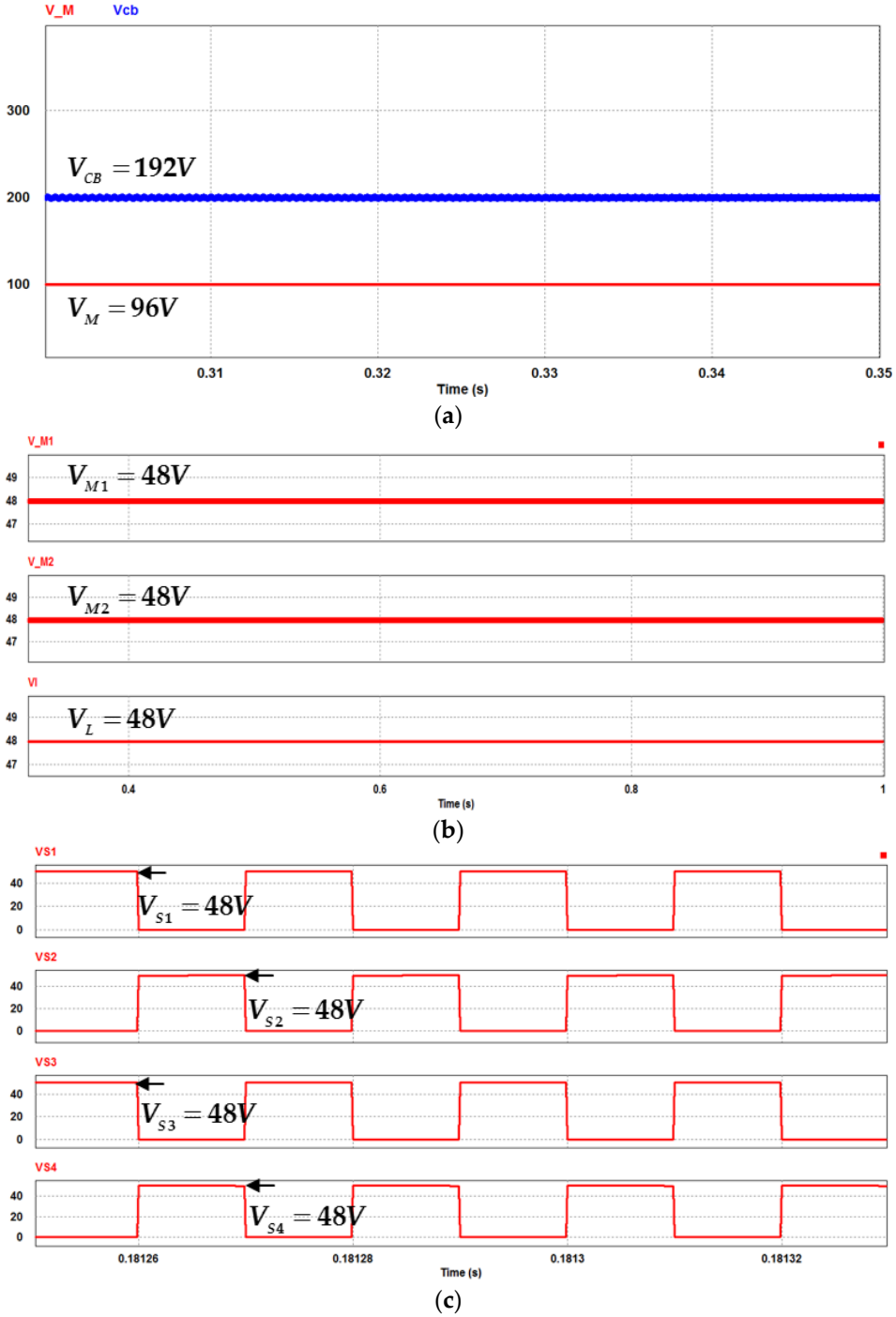

Figure 17. Simulated waveforms of the studied BDC in charge state at full load: (**a**) charge-pump capacitor voltage V_{CB}, middle-link voltage V_M; (**b**) middle-link capacitor voltages V_{M1}, V_{M2}, and low-side voltage V_L; (**c**) switch voltages of S_1, S_2, S_3, S_4.

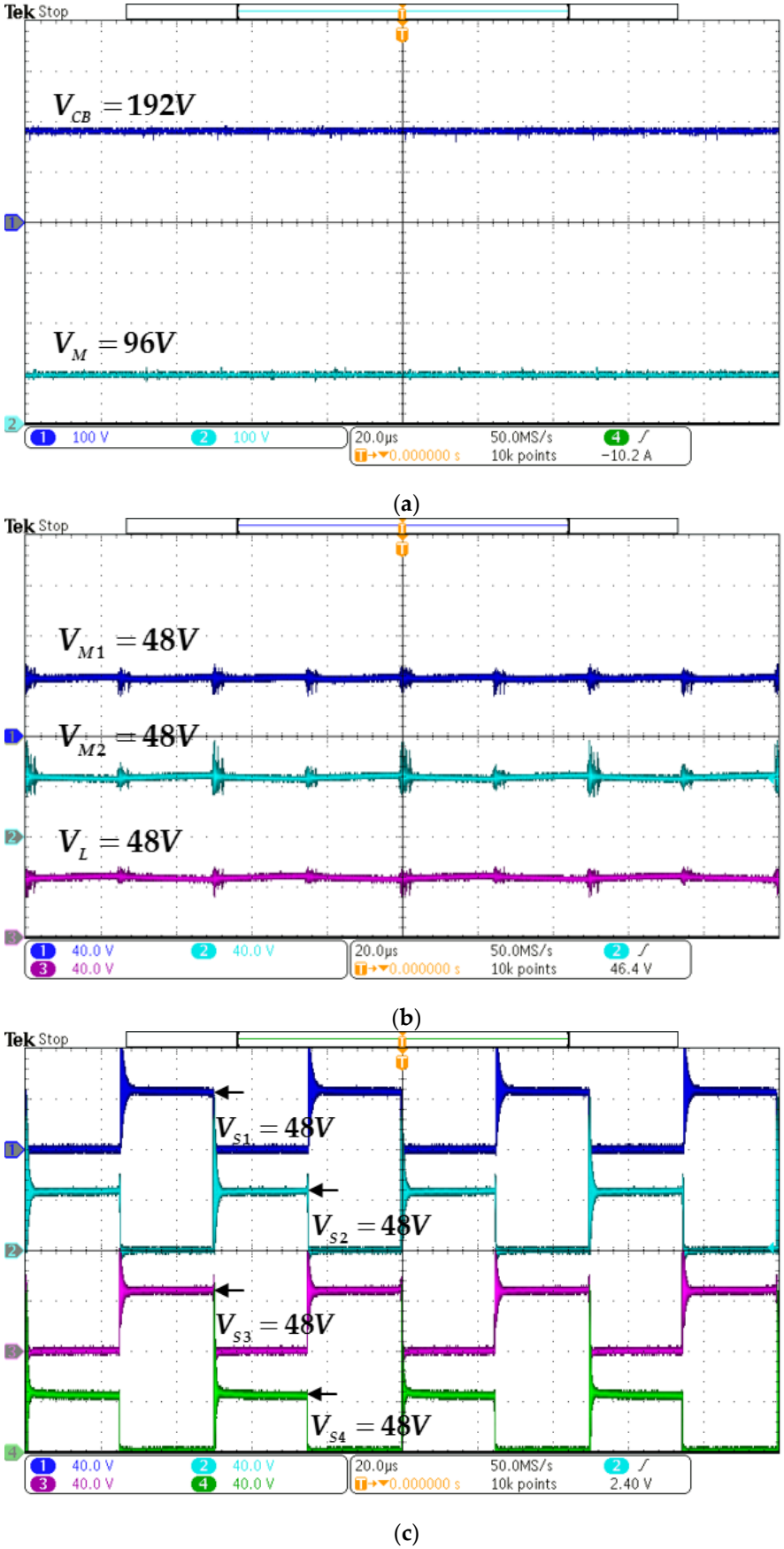

Figure 18. Measured waveforms of the studied BDC in charge state at full load: (**a**) charge-pump capacitor voltage V_{CB} and middle-link voltage V_M; (**b**) middle-link capacitor voltages V_{M1}, V_{M2}, and low-side voltage V_L; (**c**) switch voltages of S_1, S_2, S_3, S_4.

Figure 19 shows the simulated waveforms of gate signals of Q_3, Q_4, the two-phase inductor currents (i_{L1}, i_{L2}) and the switch voltages of (V_{Q3}, V_{Q4}) in charge state at full load condition. The corresponding experimental results are also shown in Figure 20. One can observe that both results are in very close agreement as well. From the figures it is observed that by interleaved controlling the duty cycles of 0.52 for the switches (Q_3, Q_4), the two-phase currents (i_{L1}, i_{L2}) are in complementary relation and in CCM. Also, from Figures 19b and 20b, the charge-pump capacitor voltage (V_{CB}) is about 192.5 V, it can clamp the switch voltages of active switches (Q_3, Q_4) to be nearly one-half of the regulated high-side voltage V_H of 385 V.

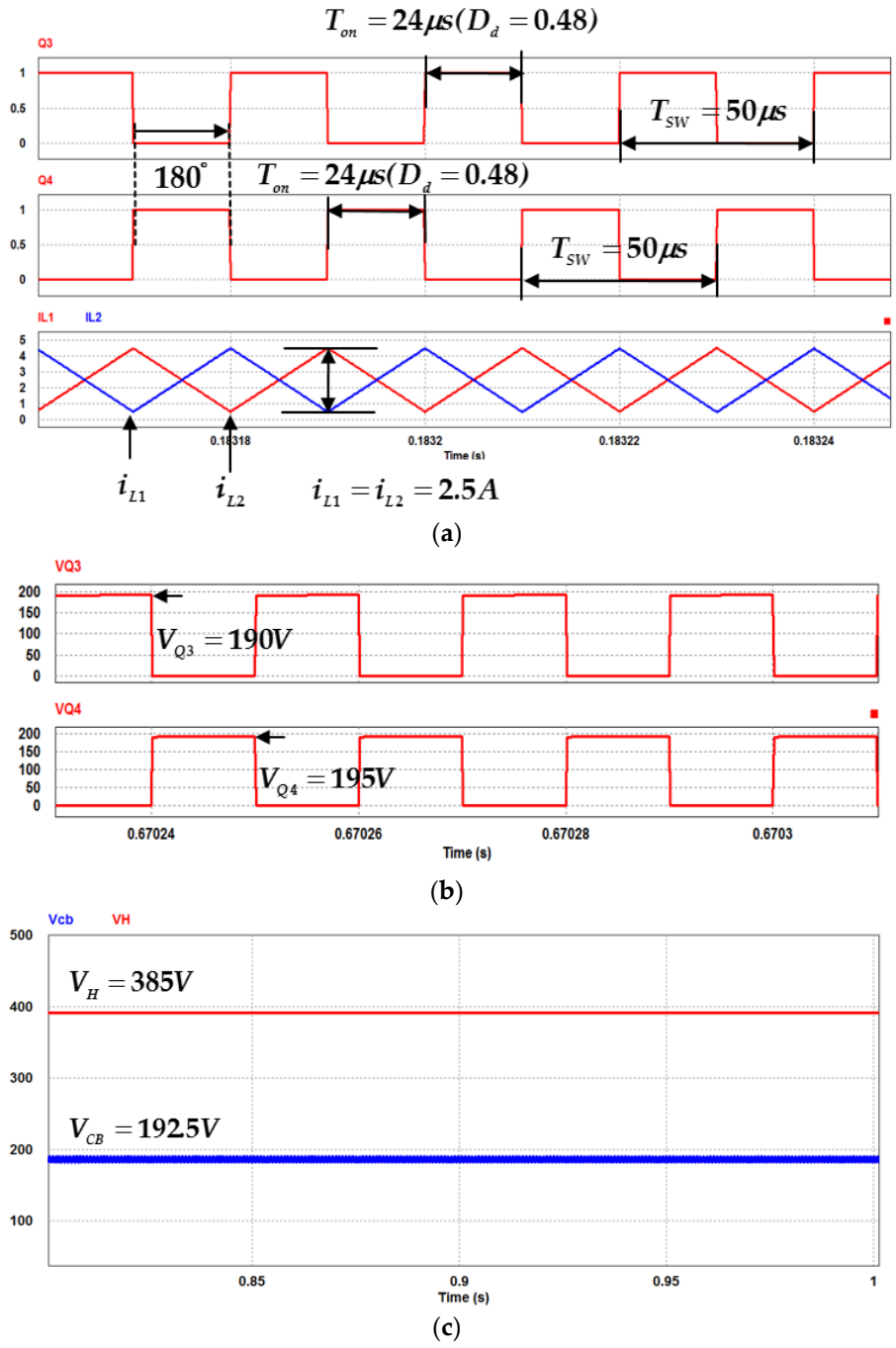

Figure 19. Simulated waveforms of the studied BDC in discharge state at full load: (**a**) gate signals of Q_3, Q_4, two-phase inductor currents i_{L1}, i_{L2}; (**b**) switch voltages of Q_3, Q_4; (**c**) charge-pump capacitor voltage V_{CB} and high-side voltage V_H.

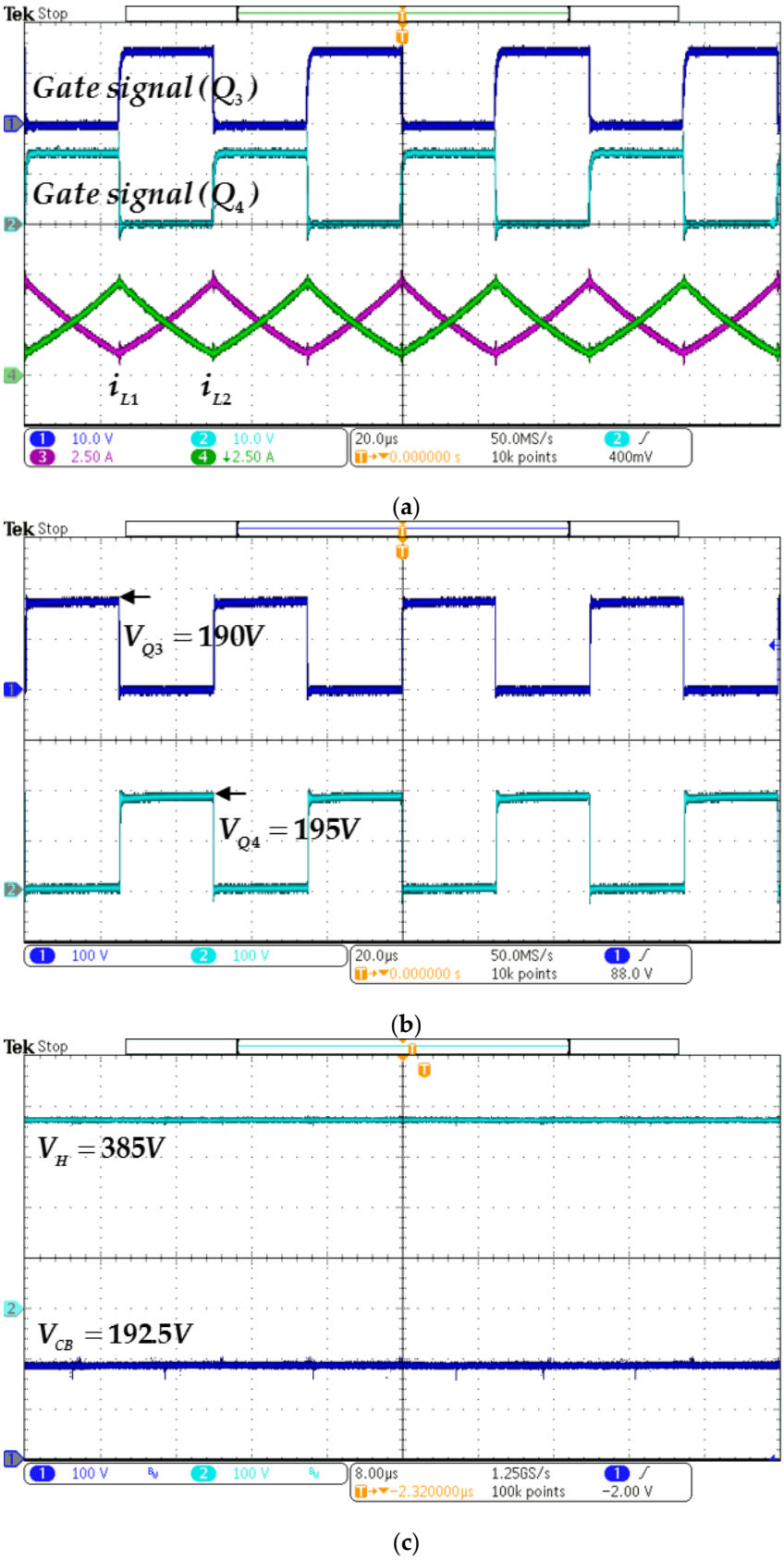

Figure 20. Measured waveforms of the studied BDC in discharge state at full load: (**a**) gate signals of Q_3, Q_4, two-phase inductor currents i_{L1}, i_{L2}; (**b**) switches voltages of Q_3, Q_4; (**c**) charge-pump capacitor voltage V_{CB} and high-side voltage V_H.

Figure 21 summarizes the measured conversion efficiency of the studied BDC in charge and discharge states. On the experimental porotype system, the conversion efficiency is measured via precise digital power meter WT310 equipment, manufactured by the Yokogawa Electric Corporation (Tokyo, Japan). The accuracy of the measured power is within +/−0.1%. It can be seen that from Figure 21, the measured highest conversion efficiency is 95% in discharge state and is around 96% in charge state. In order to clarify the actual measured conversion efficiency further, based on the equations in Table 2, the calculated power loss distribution at the rated load condition is listed in Table 3, and furthermore, the calculated losses breakdown diagrams of the studied BDC are depicted in Figure 22. From Table 3 and Figure 22, one can see that the power losses mainly occur in the copper loss of the inductors, switching loss and conduction loss of the MOSFETs. The total power losses in charge and discharge states are 28.5 W and 28.6 W, accounting for 5.70% and 5.73%, in rated load condition, respectively. These match well the measured conversion efficiency of the studied BDC in charge (94.29%) and discharge (94.25%) states.

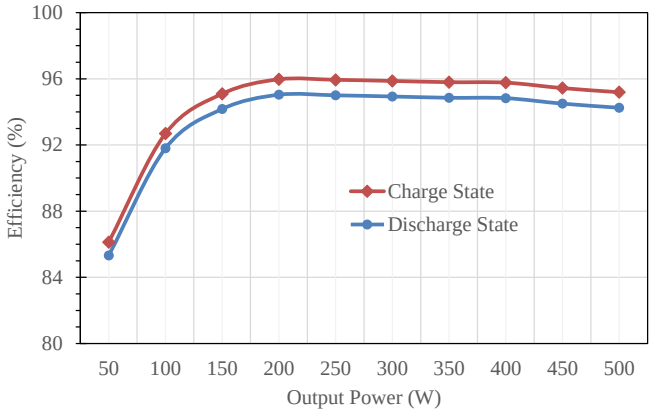

Figure 21. Measured conversion efficiency of the studied BDC for low-side voltage V_L = 48 V and high-side voltage V_H = 385 V under different loads.

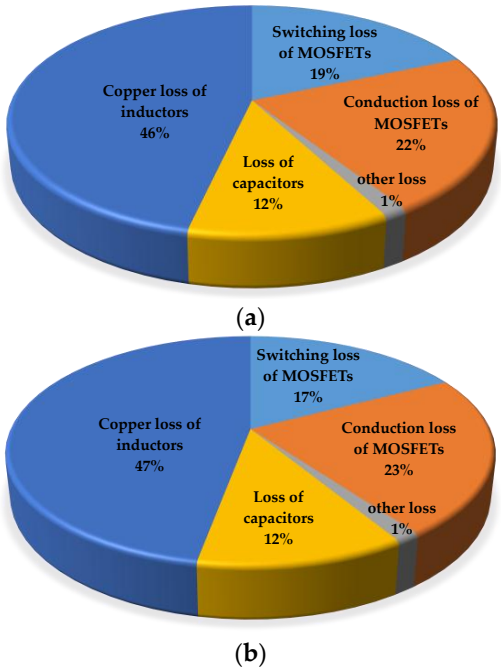

Figure 22. Calculated losses breakdown diagrams at rated load condition: (**a**) in charge state; (**b**) in discharge state.

Table 3. Power loss distribution (500 W rated load condition).

Items	Charge State	Discharge State
	Calculated Results	**Calculated Results**
Conduction loss of Q_1	0.62 W	0.62 W
Conduction loss of Q_2	1.58 W	1.58 W
Conduction loss of Q_3	0.67 W	0.67 W
Conduction loss of Q_4	1.29 W	1.29 W
Conduction loss of S_1	0.58 W	0.58 W
Conduction loss of S_2	0.58 W	0.58 W
Conduction loss of S_3	0.58 W	0.58 W
Conduction loss of S_4	0.58 W	0.58 W
Switching loss of Q_1 (turn on/off transition)	on: 0.09 W; off: 0.52 W	on: 0.10 W; off: 0.72 W
Switching loss of Q_2 (turn on/off transition)	on: 0.19 W; off: 1.01 W	on: 0.17 W; off: 0.87 W
Switching loss of Q_3 (turn on/off transition)	on: 0.09 W; off: 0.62 W	on: 0.09 W; off: 0.52 W
Switching loss of Q_4 (turn on/off transition)	on: 0.10 W; off: 0.69 W	on: 0.09 W; off: 0.54 W
Switching loss of S_1 (turn on/off transition)	on: 0.07 W; off: 0.44 W	on: 0.05 W; off: 0.55 W
Switching loss of S_2 (turn on/off transition)	on: 0.05 W; off: 0.60 W	on: 0.06 W; off: 0.35 W
Switching loss of S_3 (turn on/off transition)	on: 0.05 W; off: 0.47 W	on: 0.05 W; off: 0.29 W
Switching loss of S_4 (turn on/off transition)	on: 0.06 W; off: 0.34 W	on: 0.05 W; off: 0.46 W
Conduction loss of L_1	4.94 W	4.94 W
Conduction loss of L_2	4.94 W	4.94 W
Conduction loss of L_a	1.80 W	1.80 W
Conduction loss of L_b	1.80 W	1.80 W
Conduction loss of C_B	1.61 W	1.61 W
Conduction loss of C_H	1.67 W	1.67 W
Conduction loss of C_L	0.02 W	0.02 W
Conduction loss of C_{M1}	0.01 W	0.01 W
Conduction loss of C_{M2}	0.01 W	0.01 W
Gate driving loss of Q_1~Q_4	0.02 W	0.02 W
Gate driving loss of S_1~S_4	0.08 W	0.08 W
Total losses	28.5 W	28.64 W
% in rated load condition	5.70%	5.73%
Calculated Efficiency	94.30%	94.27%
Measured Efficiency	94.29%	94.25%

The performance comparisons between the studied BDC and a variety of published research results are summarized in Table 4. As can be seen from the comparative data, though the amounts of components in the proposed converter are more than the requirement in the other previous BDCs. The studied two-phase BDC indeed performs the higher conversion efficiency, bidirectional power flow, lower output ripples under 500 W power rating than other announced works [17,22,23]. Finally, the practical photograph of the realized BDC prototype and the test bench system are depicted in Figure 23.

Table 4. Performance comparisons with other published converters.

Items	Topology			
	This Work	**[17]**	**[22]**	**[23]**
Switching control structure	two-phase	single-phase	single-phase	single-phase
Output ripple	Low	High	Medium	Medium
Step-up conversion ratio	$4/(1-D_b)$	$n/(1-D_b)$	$2/(1-D_b)$	$1/(1-D_b)^2$
Step-down conversion ratio	$D_d/4$	$D_d/(1+n-nD_d)$	$D_d/2$	$(D_d)^2$
High-side voltage	385 V	400 V	200 V	62.5 V
Low-side voltage	48 V	48 V	24 V	10 V
Realized prototype power rating	500 W	200 W	200 W	100 W
Number of main switches	8	4	4	4
Number of storage components	7	5	5	5
Maximum efficiency (charge state)	96%	91.6%	94.8%	91.5%
Maximum efficiency (discharge state)	95%	94.3%	94.1%	92.5%

n: the turns ratio of coupled inductor [17].

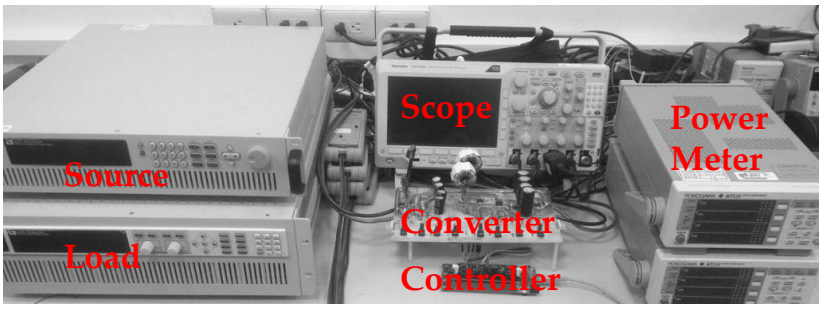

Figure 23. Photograph of the realized BDC prototype and the test bench system.

5. Conclusions

A novel BDC topology with high voltage conversion ratio is developed and a 500 W rating prototype system with 48 V battery input is constructed. Applying the developed BDC topology to the 48 V mini-hybrid powertrain system is also expected in the future [27]. In this study, thanks to the ULC located at the low-side stage, high power density and efficiency in all load range make the studied BDC a promising two-stage power architecture. Furthermore, the IBCPC located at the high-side stage can achieve a much higher voltage conversion ratio under a reasonable duty cycle. In summary, the proposed novel BDC offers the following improvements: (1) high voltage conversion ratio; (2) low ripple current; (3) it is simpler to design, implement and control. Finally, a 500 W rating low-power prototype system is given as an example for verifying the validity of the operation principle. Experimental results show that a highest efficiency of 96% and 95% can be achieved, respectively, in charge and discharge states. Certainly, by making a suitable printed circuit board (PCB) layout, and with good component placement and good heat dissipation transfer process, the novel BDC can be implemented for higher power conversion applications.

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