

## Article

# Modeling and Controller Design of PV Micro Inverter without Using Electrolytic Capacitors and Input Current Sensors

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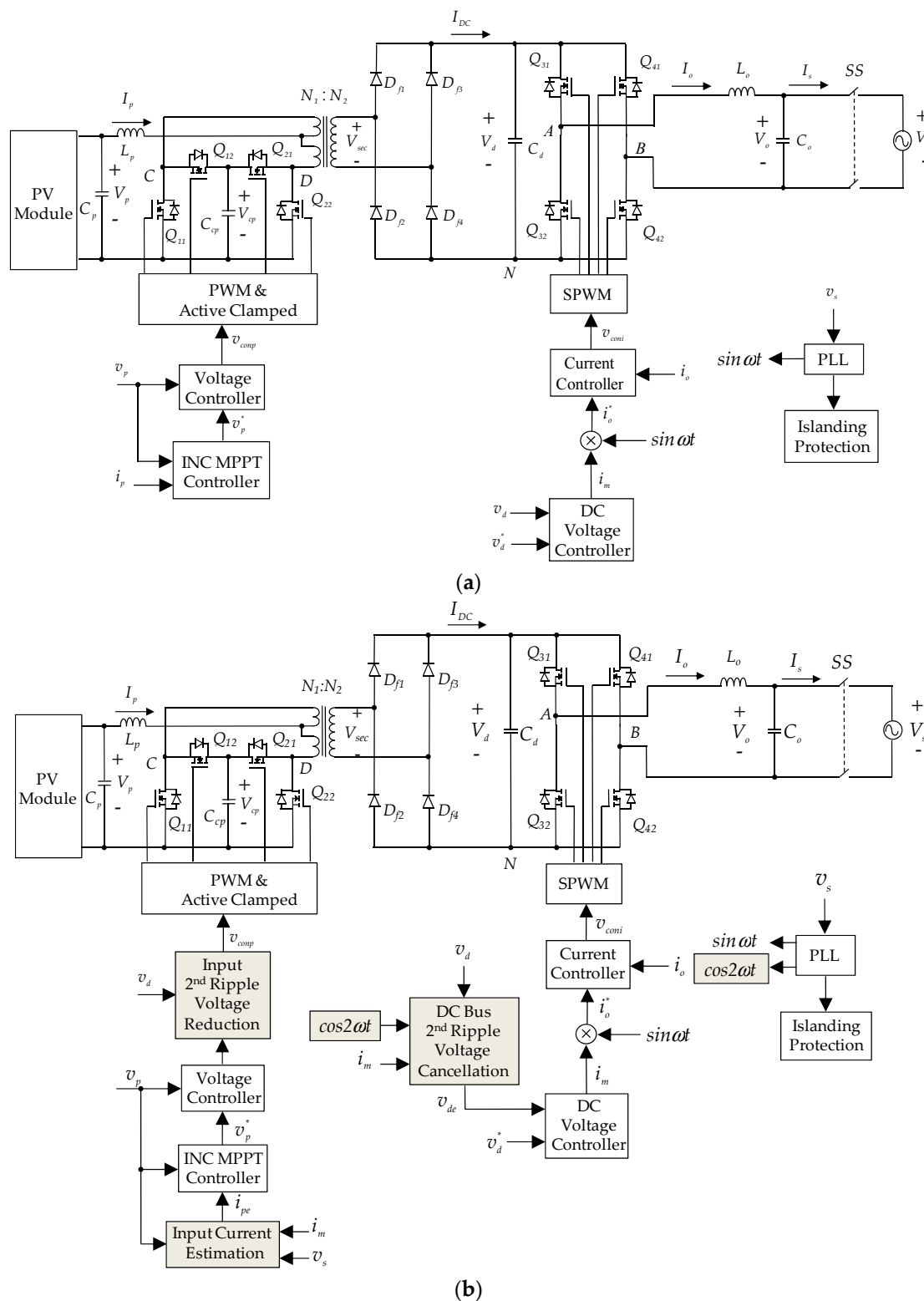
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**Abstract:** This paper outlines the modeling and controller design of a novel two-stage photovoltaic (PV) micro inverter (MI) that eliminates the need for an electrolytic capacitor (E-cap) and input current sensor. The proposed MI uses an active-clamped current-fed push-pull DC-DC converter, cascaded with a full-bridge inverter. Three strategies are proposed to cope with the inherent limitations of a two-stage PV MI: (i) high-speed DC bus voltage regulation using an integrator to deal with the 2nd harmonic voltage ripples found in single-phase systems; (ii) inclusion of a small film capacitor in the DC bus to achieve ripple-free PV voltage; (iii) improved incremental conductance (INC) maximum power point tracking (MPPT) without the need for current sensing by the PV module. Simulation and experimental results demonstrate the efficacy of the proposed system.

**Keywords:** ripple voltage cancellation technique; input current; sensorless; incremental conductance maximum power point tracking; active-clamped current-fed push-pull DC-DC converter

## 1. Introduction

Micro inverters (MIs) have a number of advantages over string inverters [1–4]: (i) they are free from the issue of shading; (ii) maximum power point tracking (MPPT) can be implemented for individual photovoltaic (PV) modules to maximize efficiency; (iii) installation and maintenance are simple and easy. In contrast, the two-stage inverter topology with an isolated DC-DC converter cascaded with an inverter requires a large electrolytic capacitor (E-cap) on the DC bus to absorb the reactive power at the 2nd harmonic frequency [5–7]. Nonetheless, the robustness and lifespan of MIs is an issue, which has prompted a move toward designs that avoid the use of relatively fragile E-caps [8,9]. Some devices include a decoupling circuit or ripple port circuit to absorb the reactive power [10,11]; however, this increases fabrication costs and results in switching losses that reduce the efficiency of the MI. As shown in Figure 1a [12–14], a film capacitor with a longer lifespan can be used as a substitute for an E-cap in typical single-phase two-stage MI systems [15]. However, the capacitance of a film capacitor is less than that of an E-cap with the same power rating, which increases voltage ripple at the 2nd harmonic frequency on the DC bus and can have three serious side-effects. First, voltage regulation on the DC bus must be limited to a narrow frequency bandwidth (usually 125.6 rad/s) in order to limit distortion of the grid current. Second, 2nd harmonic voltage ripple on the DC bus can cause 2nd harmonic voltage ripple of the PV voltage, which ultimately degrades the precision of MPPT due to the voltage oscillation around the maximum power point (MPP). Third, the fact that the PV voltage control loop and the input power calculation are limited by the 2nd harmonic frequency component means that the response speed of the MPPT is greatly constrained.



**Figure 1.** Two-stage MI with current-fed push-pull converter cascaded with full bridge inverter: (a) conventional; (b) proposed.

Feedforward control with a bandpass filter was adopted in [16] for the extraction of the 2nd harmonic frequency component in order to minimize distortion of the grid current. The 2nd harmonic frequency component is then subtracted from the feedback voltage to produce a feedback signal

without ripple. This ensures that the regulated signal generating the inverter current command is smooth and that the current command is low in distortion. This solves the current distortion problem; however, the DC bus voltage response is slowed by the inclusion of a bandpass filter. Some researchers have employed a notch filter or a combo filter augmented with an outer voltage controller in order for the 2nd harmonic frequency to attenuate the 2nd harmonic voltage ripple and thereby increase the crossover frequency of the outer voltage loop [12,13]. However, the maximum crossover frequency of the outer voltage loop is still limited and lower than double of the output frequency. A load current feedforward control scheme with high DC voltage response speed was presented in [17]; however, it is limited only to the applications in which the inverter supplies an isolated load, which means that it is unsuitable for a grid-connected system. On the DC-DC converter side, researchers have sought to increase MPPT efficiency by applying current mode control in the outer loop and voltage mode control in the inner loop of the MPPT control to reduce PV voltage ripple [13]. The inner loop was designed with high gain on the 2nd harmonic frequency to attenuate the propagation of 2nd harmonic voltage ripple from the DC bus into the PV input side. Despite the effectiveness of these methods, they all require input current sensing for the execution of MPPT. Various MPPT control methods have been proposed [18], and among these, incremental conductance (INC) MPPT has proven particularly with regard to stability, fast speed, and precision [19]. However, this method also requires the input current sensing in order to calculate conductance [20].

The three control methods in Figure 1b were developed to overcome the limitations of the two-stage topology in Figure 1a. We developed a novel 2nd ripple voltage cancellation technique to speed up voltage regulation on the DC bus. This method employs an integrator with a small time constant, instead of using a 2nd order filter, to achieve fast response. A feedforward 2nd ripple voltage reduction technique to reduce PV voltage ripple is also developed. Finally, an improved INC MPPT using the inverter parameters is developed in order to eliminate the need for an input current sensor and thereby reduce costs. A 240 W MI is implemented using the proposed control methods on a Texas instruments (TI) TMS320F28335 digital signal processing (DSP). Experiments are then conducted to demonstrate the effectiveness of the proposed control methods.

## 2. Modeling and Controller Design of Grid-Connected Inverter

The proposed two-stage PV MI is presented in Figure 1b, where  $V_o$  is the output voltage of the inverter;  $v_o = k_v V$ ,  $k_v$  is the voltage sensing factor;  $V_s$  is the grid voltage;  $v_s = k_v V_s$ ;  $I_s$  is the grid current;  $I_o$  is the output current of inverter;  $i_o = k_s I_o$ , and  $k_s$  is the current sensing factor;  $i_o^*$  is the current command of  $i_o$ ;  $V_d$  is the DC bus voltage;  $v_d = k_v V_d$ ;  $v_d^*$  is the DC bus voltage command;  $I_{DC}$  is the current generated by the DC-DC converter;  $V_p$  is the voltage of the PV module;  $v_p = k_v V_p$ ;  $v_p^*$  is the PV module voltage command;  $I_p$  is the input current of the DC-DC converter;  $i_m$  is the current amplitude of  $i_o^*$ ;  $v_{comp}$  is the pulse width modulation (PWM) control voltage ( $p = C, D$ );  $v_{coni}$  is the PWM control voltage ( $i = A, B$ );  $\sin\omega t$  is the synchronous sine-wave obtained from the phase-locked loop; and SS is the solid-state switch. The full-bridge inverter in Figure 1b can be described using the following state equation:

$$L_o \frac{dI_o}{dt} = V_{AN} - V_{BN} - V_o = S_A V_d - S_B V_d - V_o \quad (1)$$

where  $S_A$  and  $S_B$  are the switching functions of the A and B legs respectively, and:

$$S_i = \frac{1}{2} + \frac{v_{coni}}{2v_{tm}} \quad (i = A, B) \quad (2)$$

where  $v_{tm}$  is the amplitude of the PWM triangular signal. The use of unipolar voltage switching means that:

$$v_{conB} = -v_{conA} \quad (3)$$

One can derive the following equation by substituting (2) and (3) into (1), as follows:

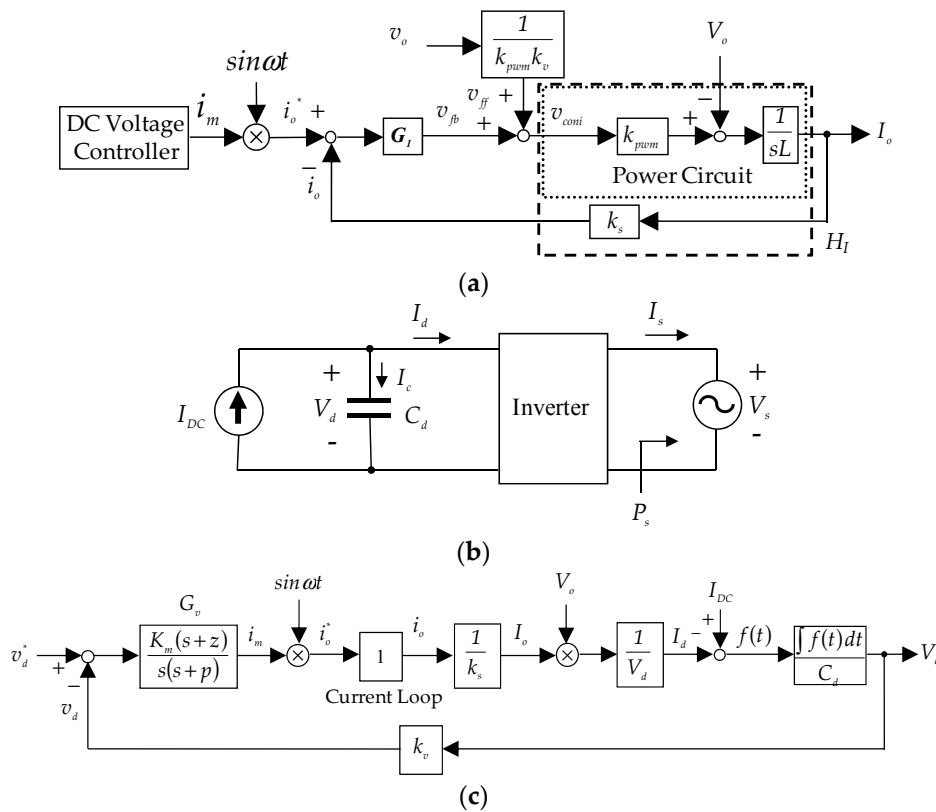
$$L_o \frac{dI_o}{dt} = \frac{v_{con}}{v_{tm}} V_d - V_o \quad (4)$$

Moreover, (4) can be represented as:

$$L_o \frac{dI_o}{dt} = k_{pwm} v_{con} - V_o \quad (5)$$

where  $k_{pwm} = \frac{V_d}{v_{tm}}$ .

The current control loop of the inverter in which  $i_o$  tracks  $i_o^*$  can be designed as shown in Figure 2a, where dash block  $H_I$  is plotted to represent (4). Current command  $i_o^*$  is generated by multiplying the synchronous  $\sin\omega t$  signal with regulated signal  $i_m$  from the outer DC voltage controller. Output voltage  $V_o$  is equivalent to a disturbance in the current loop. Feedforward control signal  $v_{ff}$  is used to cancel this disturbance directly via a signal  $v_{con}$ , and  $v_{fb}$  is a control signal for current feedback compensation.



**Figure 2.** Block diagram of inverter control loop: (a) Current control loop; (b) DC voltage equivalent circuit; (c) DC voltage control loop.

Many types of control, such as proportional (P), proportional-integral (PI), type 2 and proportional-resonant (PR) [21], can be used in the design of current controller  $G_I$ . In this study, a P control with gain  $k_1$  is adopted. The current tracking response can be derived as follows:

$$\frac{i_o}{i_o^*} = \frac{\frac{k_1 k_s k_{pwm}}{L_o}}{s + \frac{k_1 k_s k_{pwm}}{L_o}} = \frac{u_i}{s + u_i} \quad (6)$$

where pole  $u_i$  is equivalent to the bandwidth of the current control loop. The bandwidth of the current loop can be assigned to be  $f_s/8 \sim f_s/10$ , where  $f_s$  is the switching frequency. By assigning the value of  $u_i$ , the gain of the feedback controller  $k_1$  can be calculated as follows:

$$k_1 = \frac{u_i L_o}{k_s k_{pwm}} \quad (7)$$

The inverter can also be represented using the equivalent circuit in Figure 2b, where  $I_d$  is the DC bus current;  $I_c$  is the DC bus capacitance current of  $C_d$ ; and  $P_s$  is the output power of the inverter. The bandwidth of the current control loop is far higher than that of the DC voltage control loop; therefore, the current tracking response in (6) can be treated as ideal (i.e.,  $i_o/i_o^* = 1$ ) in the design of the DC voltage control loop. The DC voltage control loop is then represented as shown in Figure 2c. By disregarding the AC filter, capacitor current grid current  $I_s$  can be represented as follows:

$$I_s = I_o = \frac{i_o}{k_s} = \frac{i_o^*}{k_s} = \frac{i_m \sin \omega t}{k_s} = I_m \sin \omega t \quad (8)$$

where  $I_m$  is the amplitude of  $I_s$ . The output power of the inverter can be derived as:

$$\begin{aligned} P_s &= V_s I_s = V_m \sin \omega t I_m \sin \omega t = \frac{V_m I_m}{2} - \frac{V_m I_m}{2} \cos 2\omega t \\ &= \bar{P}_{ac} + \tilde{P}_{ac2} \end{aligned} \quad (9)$$

where  $V_m$  is the amplitude of  $V_s$ . The output power contains a DC component  $\bar{P}_{ac}$  and an 2nd harmonic AC component  $\tilde{P}_{ac2}$ . This 2nd harmonic component generates a 2nd harmonic current to charge and discharge the DC bus capacitor, resulting in 2nd harmonic voltage ripple. Disregarding the loss of the inverter, the DC input power of the inverter is equal to the output power of the inverter as follows:

$$\bar{P}_{ac} = P_{dc} \quad (10)$$

Thus:

$$\frac{V_m I_m}{2} = V_d I_d \quad (11)$$

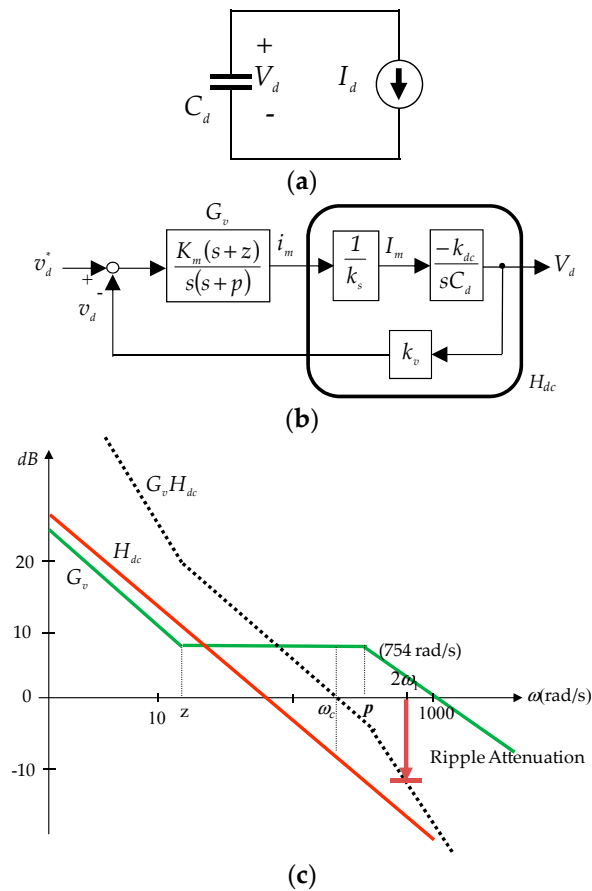
The DC input current of the inverter can be derived as:

$$I_d = \frac{V_m I_m}{2V_d} = k_{dc} I_m, \quad k_{dc} = \frac{V_m}{2V_d} \quad (12)$$

In the design of a conventional DC bus voltage controller, a small signal model of the inverter can be represented as current source  $I_d$  to discharge DC capacitor  $C_d$ , as shown in Figure 3a. The transfer function of the DC control model can be derived as:

$$\frac{V_d}{I_m} = \frac{-k_{dc}}{sC_d} \quad (13)$$

The small signal model of the voltage loop can be derived from Figure 2c and (13), as shown in Figure 3b. The design of voltage controller  $G_v$ , which is a 2nd order compensator with zero  $z$  and pole  $p$ , can be based on the voltage loop model  $H_{dc}$ , as shown Figure 3b. A Bode plot of the loop gain is presented in Figure 3c. When taking into account the 2nd harmonic voltage ripple on  $V_d$ , bandwidth  $\omega_c$  of loop gain  $G_v H_{dc}$  must be far lower than 2nd harmonic frequency  $2\omega_1$  in order to attenuate the voltage ripple in current amplitude command  $i_m$ . The bandwidth is usually located at 125.6 rad/s to minimize distortion of the inverter current command while providing voltage regulation of acceptable speed.

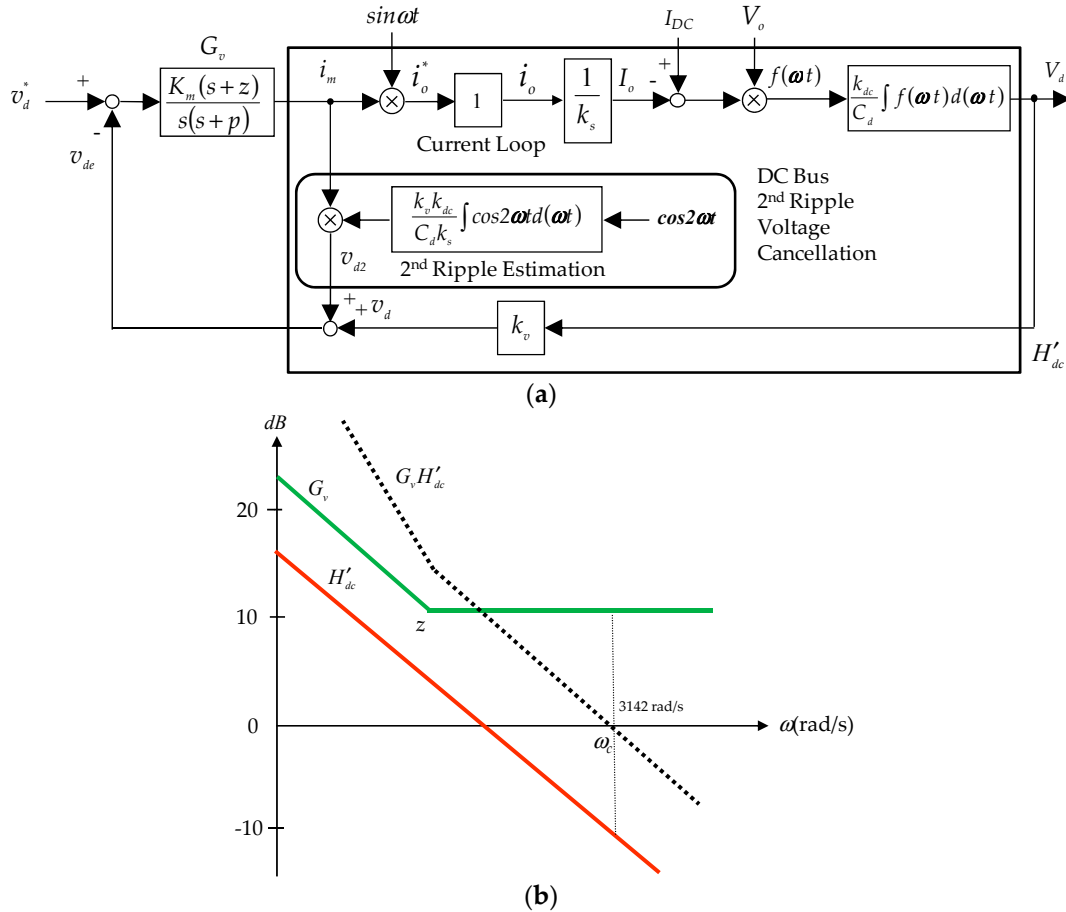


**Figure 3.** Conventional DC bus voltage controller for inverter: (a) small signal model of inverter viewed from the DC side; (b) DC bus voltage control loop; (c) bode plot of control loop transfer functions.

The above method is commonly used for the design of a general two-stage system with a large capacitance E-cap on the DC bus. However, the use of low capacitance of film capacitors as an alternative to E-cap topology results in greater DC bus voltage ripple, such that a bandwidth of 125.6 rad/s does not provide sufficient attenuation. Reducing the bandwidth to attenuate the ripple would lower the response speed and increase voltage disturbance when the generated power is changed. In contrast, employing a higher bandwidth to cope with voltage disturbance would lead to the distortion of grid current. As shown in Figure 4, a technique for the cancellation of 2nd ripple voltage on the DC bus is developed to overcome this difficulty, where  $H'_{dc}$  is the new voltage loop model. A 2nd ripple signal  $v_{d2}$ , which is equal to the 2nd ripple of feedback voltage  $v_d$ , is used to eliminate the 2nd ripple of feedback signal  $v_{de}$ . The voltage controller generates current amplitude command  $i_m$ , where  $i_m$  is the magnitude of command signal of  $i_o^*$ , which is sent to the DC bus voltage 2nd ripple voltage cancellation block. The fact that there is no 2nd ripple in  $v_{de}$  means that the bandwidth of the voltage loop gain can be made wider than the 2nd harmonic frequency, thereby ensuring a fast response, as shown in Figure 4b (bandwidth of 3141 rad/s). The proposed method for the cancellation of 2nd ripple voltage is based on the situation in which there is no 2nd ripple current in  $I_o$ . All of the 2nd reactive power is absorbed by the DC bus capacitor, which means that the DC bus capacitor is charged and discharged only by  $\tilde{P}_{ac2}$  in Equation (9). Thus, an integrator is used to calculate the 2nd harmonic voltage ripple as follows:

$$v_{d2} = k_v V_{d2} = \frac{k_v \int \frac{\tilde{P}_{ac2}}{V_d} dt}{C_d} = \frac{k_v \int \frac{V_m I_m}{2V_d} \cos 2\omega t d(\omega t)}{C_d} = \frac{k_v k_{dc} i_m \int \cos 2\omega t d(\omega t)}{k_s C_d} \quad (14)$$

To prevent the coupling of control loops in practical implementations, the  $i_m$  of the last sampling interval is adopted in (14). The use of an integrator enables the adoption of a digital integrator with small time constant, which means that the voltage dynamic response is not be limited by the 2nd ripple calculation.



**Figure 4.** Proposed method for cancellation of 2nd ripple voltage on the DC bus: (a) Control block diagram; (b) Bode plot of control loop transfer functions.

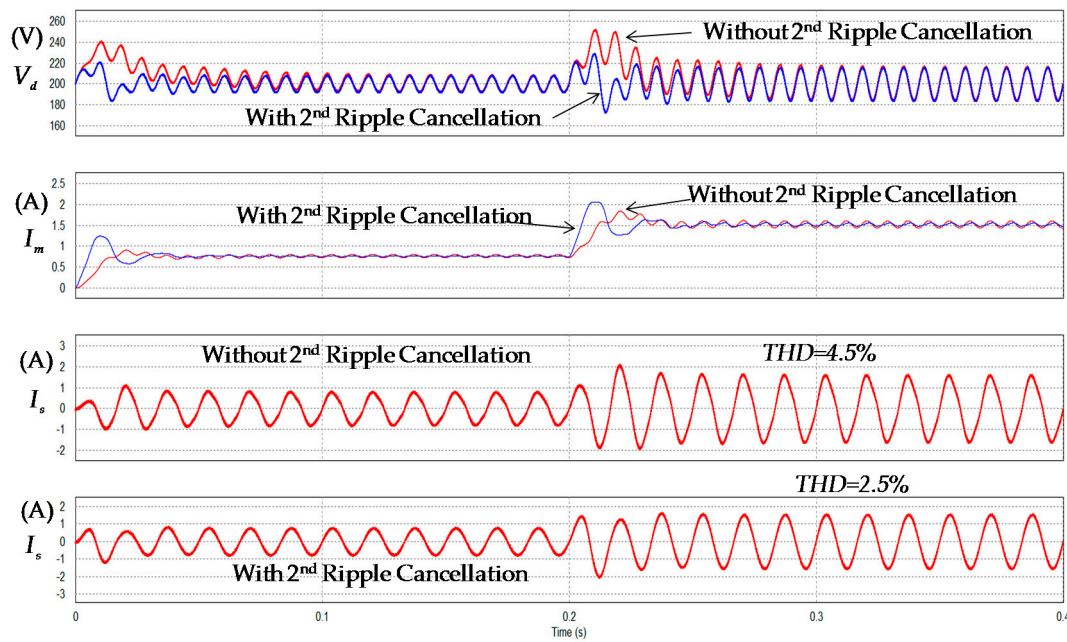
To verify the design of the proposed current and voltage controller and 2nd ripple voltage cancellation technique, a 240 W grid-connected inverter is designed using the parameters listed in Table 1. The  $k_1$  in (7) and the 2nd order compensator are designed as follows:

$$k_1 = 2.5, G_v = \frac{450(s+30)}{s(s+180)}. \quad (15)$$

Figure 5 presents the simulation results obtained with and without the application of the proposed 2nd ripple voltage cancellation technique to the inverter. The test condition involves changing the inverter input current at 0.2 s to vary the output power between 120 W and 240 W. Simulation results demonstrate that the proposed 2nd ripple voltage cancellation technique enables rapid DC bus voltage  $V_d$  response with reduced overvoltage. Moreover, applying the proposed 2nd ripple voltage cancellation technique reduces distortion in the amplitude command of the inverter output current  $I_m$ . Furthermore, the proposed 2nd ripple voltage cancellation technique reduces the total harmonic distortion (THD) in the inverter output current  $I_s$  from 4.5% to 2.5%.

**Table 1.** Parameters of grid-connected inverter.

Items	Values
Grid Voltage $V_s$	100 Vrms
Grid Frequency	60 Hz
Inverter Rated Power	240 W
Filter Inductor $L_o$	1.2 mH
Filter Capacitor $C_o$	1 $\mu$ F
Switching Frequency	20 kHz
DC Capacitor $C_d$	80 $\mu$ F
DC Bus Voltage $V_d$	200 V
Power MOSFET $Q_{3x} \sim Q_{4x}$	FDPF18N50

**Figure 5.** Simulation results of inverter with and without proposed 2nd voltage cancellation control.

### 3. Modeling and Controller Design of MPPT DC-DC Converter

The active-clamped current-fed push-pull converter can be operated using duty cycle  $d$  of each main switch  $Q_{11}$  and  $Q_{21}$  less or larger than 0.5. Clamped switches  $Q_{12}$  and  $Q_{22}$  are switched complementary to the main switch. One can derive the following state equation from Figure 1b [22]:

$$L_p \frac{dI_p}{dt} = V_p - 2(1-D) \frac{N_1}{N_2} V_d \quad (16)$$

The voltage conversion ratio at steady state can be derived from (16) as follows:

$$\frac{V_d}{V_p} = \frac{N_2}{N_1} \frac{1}{2(1-D)} \quad (17)$$

In (17), if one sets  $D = 0.5$  with  $V_d = \frac{N_2}{N_1} V_p$  being the nominal condition, then  $D < 0.5$  is in buck mode and  $D > 0.5$  is in boost mode.

Considering large 2nd harmonic voltage ripple in DC bus voltage  $V_d$ , then the following analysis could be used to express the bus voltage as  $V_d = V_{d0} + V_{d2}$ , where  $V_{d0}$  is the average value of  $V_d$ , and  $V_{d2}$  is the 2nd ripple voltage. Equation (16) can be rewritten as:



The design of the input for the 2nd ripple voltage reduction control scheme in Figure 6a is based on (24). A 2nd band-pass filter is used to extract  $V_{d2}$ , where signal  $v_{tm}$  is the amplitude of the PWM triangular waveform. Equation (24) is implemented using feedforward control signal  $v_{conf}$ , resulting in the following final duty:

$$D = D_0 + D_2 \quad (25)$$

where  $D = \frac{v_{comp}}{v_{tm}} = \frac{v_{cong} + v_{conf}}{v_{tm}}$ ,  $D_0 = \frac{v_{cong}}{v_{tm}}$ ,  $D_2 = \frac{v_{conf}}{v_{tm}}$  and  $v_{conf} = (v_{tm} - v_{cong}) \frac{v_{d2}}{v_{d0} + v_{d2}}$ . Once the 2nd ripple voltage  $V_{d2}$  has been eliminated, the small signal model of the PV voltage control loop can be obtained from Figure 6a, as shown in Figure 6b. The output used to control the transfer function can be derived as follows:

$$H_p(s) = \frac{v_p}{v_{comp}} = \frac{-\frac{2k_v V_d}{N v_{tm}}}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \quad (26)$$

where  $\omega_o = \frac{1}{\sqrt{L_p C_p}}$  and  $Q = \frac{R_{pv}}{\omega_o L_p}$ . The design of PV voltage controller  $G_p$ , which employs a pole-zero compensator, can be based on (26). Having eliminated the 2nd ripple voltage, the voltage loop can be given wider bandwidth to ensure fast MPPT response. The only concern is a possible lack of stability due to variations in parameter  $R_{pv}$  of the PV module in the model based on (26).

To verify the design of the above voltage controller for the DC-DC converter and the proposed 2nd ripple voltage reduction technique, a 240 W active-clamped current-fed push-pull DC-DC converter with the parameters listed in Table 2 is designed. Figure 7 presents the bode plots of various  $H_p(s)$  using the above parameters, while taking into consideration variations in  $R_{pv}$  from 0.5  $\Omega$  to 20  $\Omega$ . Figure 7 also presents the Bode plots of  $G_p$  and various  $G_p H_p$  values. Compensator  $G_p$  is designed using MPP for the case  $H_p$  ( $R_{pv} = 3.75 \Omega$ ) as the nominal operating point:

$$G_p = \frac{165(s + 10)}{s(s + 30)} \quad (27)$$

**Table 2.** Parameters of DC-DC converter.

Items	Values
PV Module Voltage $V_p$	25~42 V
DC Bus Voltage $V_d$	200 V
Converter Rated Power	280 W
Input Inductor $L_p$	25 $\mu$ H
Input Capacitor $C_p$	50 $\mu$ F
Clamp Capacitor $C_{cp}$	2.2 $\mu$ F
Switching Frequency	50 kHz
DC Capacitor $C_d$	80 $\mu$ F
Power MOSFET $Q_{1x} \sim Q_{2x}$	FDP075N15A
Diode $D_{f1} \sim D_{f4}$	F10L60U
PV Module Maximum Power	240 W
PV Module Maximum Power Voltage $V_m$	32 V
PV Module Maximum Power Current $I_m$	7.5 A
PV Module Open Circuit Voltage $V_{oc}$	40 V
PV Module Short Circuit Current $I_{sc}$	8.9 A
PV Module Internal Equivalent Resistance $R_{pv}$	0~20 $\Omega$

To consider all of the operating points when  $R_{pv}$  is changed, the crossover frequency of the loop gain  $G_p H_p$  is set to 15 kHz, which is far wider than the bandwidth of the MPPT control loop. The phase margin (PM) is also set to 95° to ensure sufficient PM for the stability at other operating points. According to the bode plots, a smaller  $R_{pv}$  results in a higher Q value, which increases the voltage gain and phase droop close to resonant frequency  $\omega_o$ . Thus, PM decreases with a reduction in the value of  $R_{pv}$ . Using the above  $G_p$ , the PM of  $G_p H_p$  is 70° at  $R_{pv} = 0.5 \Omega$ . Thus, a fair dynamic

response still can be achieved even in the worst case scenario. Figure 8 presents the voltage regulation response with and without the proposed input 2nd ripple voltage reduction controller with the PV module output power set to 240 W. This shows that the PV module voltage  $V_p$  and DC-DC converter input current  $I_p$  have nearly no ripple when the proposed 2nd ripple voltage reduction controller is applied, thereby increasing the power the PV module is able to generate.

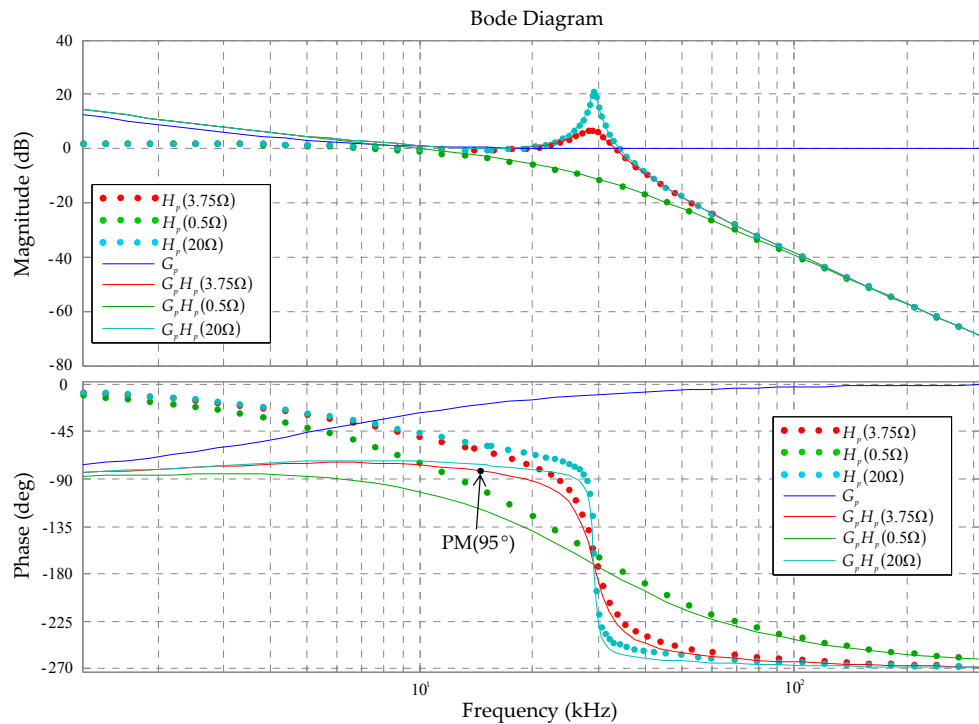


Figure 7. Bode plots for PV voltage loop control design.

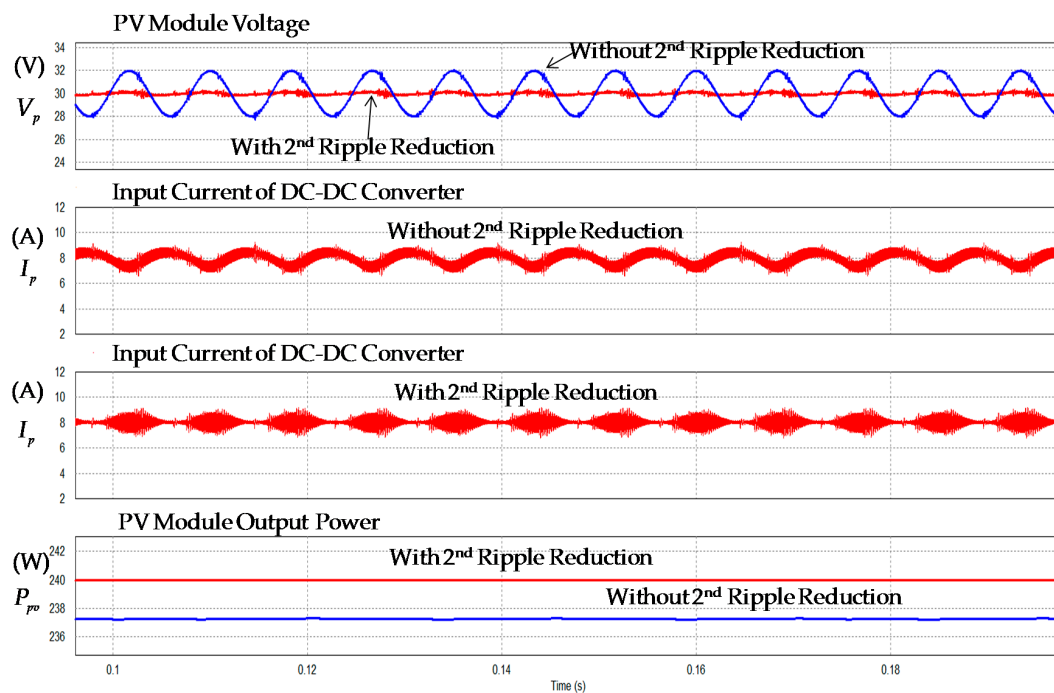


Figure 8. Voltage regulation response of PV module without and with proposed 2nd ripple voltage reduction control at input.

#### 4. MPPT Controller Design

Based on the proposed ripple-less PV voltage control system, an improved INC MPPT controller located on the outer loop of the voltage controller is developed with the aim of generating voltage commands in accordance with the operating conditions of the PV module. The INC method is adopted to track the MPP of the PV module. INC is based on the following equation that the PV module is at MPP:

$$\frac{dP_{pv}}{dV_p} = \frac{d(V_p I_p)}{dV_p} = V_p \frac{dI_p}{dV_p} + I_p = 0 \quad (28)$$

therefore:

$$-\frac{dV_p}{dI_p} = \frac{V_p}{I_p} \quad (29)$$

Equation (29) is equivalent to  $R_{pv} = R_L$ , i.e.,:

$$R_{pv} = -\frac{dV_p}{dI_p}, R_L = \frac{V_p}{I_p}. \quad (30)$$

where  $R_L$  is an impedance value equivalent to that of the DC/DC converter. It also is the MPP condition that the source  $V_{oc}$  supplied to the load  $R_L$ . However, calculation based on Equation (29) requires an input current sensor for  $I_p$ . The fast response characteristics of the inverter and DC-DC converter means that MPPT can be calculated using the inverter parameters, without taking into account the control delay. The improved INC MPPT uses the following equation to obtain  $I_p$ :

$$I_p = \frac{P_{pv}}{V_p} = \frac{P_{ac}}{V_p} = \frac{V_m I_m}{2V_p} \quad (31)$$

It can be obtained from the ripple-free control signal  $i_m$  shown in Figure 4. Figure 9 presents a control block diagram of the improved INC MPPT controller in which the estimated DC-DC converter input current  $I_p$  is obtained using Equation (31).  $R_{pv}$  and  $R_L$  are then calculated using Equation (30), which requires an absolute function to obtain  $R_{pv}$ . Resistance error  $dR$  is regulated by a PI controller to generate voltage correction signal  $V_{pr}$ , which is then added to the initial operating voltage  $V_{pinit}$  to generate the final voltage command  $v_p^*$  of the PV module.

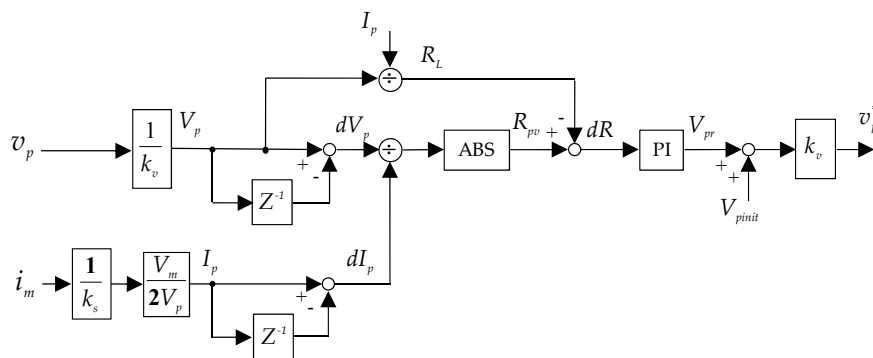
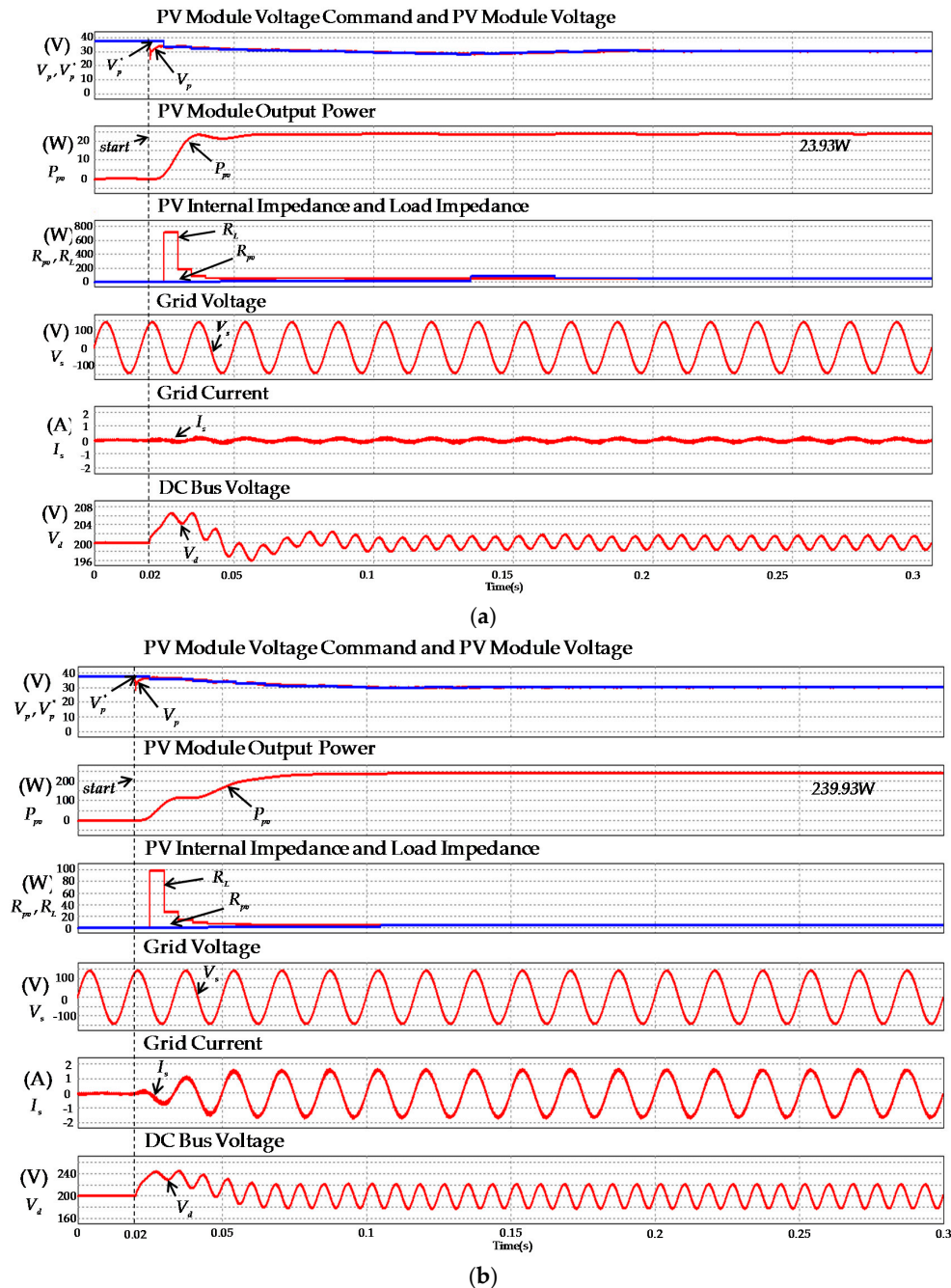


Figure 9. Improved INC MPPT controller without sensing the input current.

Figure 10a,b present simulation results obtained using the improved INC MPPT at 10% and 100% PV output power conditions respectively. The proportional and integral gains of the PI controller are set to 1 and 0.05 respectively. In the simulations, MI starts operating at 20 ms and peak power tracking is obtained within 120 ms under both test conditions. The proposed 2nd ripple voltage cancellation method helps to ensure that the inverter output current  $I_s$  is a perfect sine wave, under both test conditions. Moreover, absorption of all 2nd reactive power by the film capacitor on the DC bus resulted

in the appearance of an obvious 2nd ripple at DC bus voltage  $V_d$ . Furthermore, the DC-DC 2nd ripple voltage reduction method prevented the appearance of 2nd ripple voltage at PV module voltage  $V_p$ . This is a clear demonstration of the effectiveness of the proposed 2nd ripple voltage reduction technique in conjunction with the improved INC MPPT.



**Figure 10.** Simulation results obtained from improved INC MPPT: (a) 24 W (10%) PV output power; (b) 240 W (100%) PV output power.

## 5. Experimental Verification

Figure 11 presents the experimental setup of 240 W MI based on the above specifications and designs. The controller was realized using the TI TMS320F28335 DSP (Texas Instruments, Dallas,

TX, USA). The Chroma 62100H-600S with PV module emulating function as a DC power source is employed to facilitate the emulation of PV module characteristics.

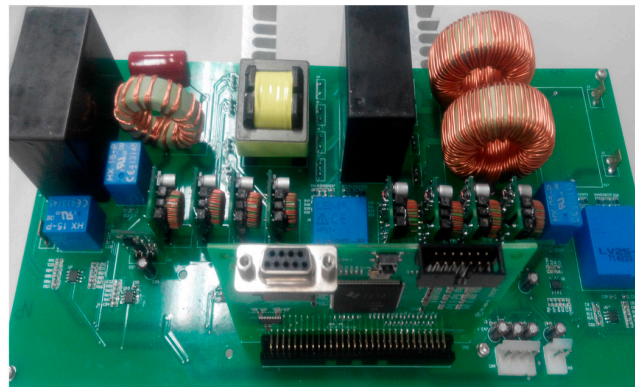


Figure 11. Experimental setup to assess proposed micro-inverter.

Figure 12a,c present the responses of DC bus voltage  $V_d$  and inverter output current  $I_s$  without and with DC bus 2nd ripple voltage cancellation controller, when the input power of the DC-DC converter changes from 120 W to 240 W. Measurement results demonstrate the fast DC bus voltage response of the proposed 2nd ripple voltage cancellation method. Figure 12b,d present the measured voltage  $V_p$  and current  $I_p$  of the PV module at 240 W output without and with input 2nd ripple voltage reduction controller. The measured waveforms demonstrate the effectiveness of the proposed 2nd ripple voltage reduction technique applied to the DC-DC converter in reducing PV side 2nd voltage and current ripple. Figure 12e,f present the measured waveforms of  $V_p$ ,  $V_d$ ,  $I_s$ , and grid voltage  $V_s$  using the improved INC MPPT at 10% and 100% PV output power respectively. These results demonstrate the speed and precision of the MPPT response under both PV output power test conditions. The experimental results in Figure 12e,f show that the power factor was not equal to 1 before initiating INC MPPT control, due to the fact that the power factor was equal to 1 when the MI began injecting actual current into the grid. All of the results obtained in experiments are in agreement with the simulation results in Figures 5, 8 and 10. These results further confirm the efficacy of the proposed designs.

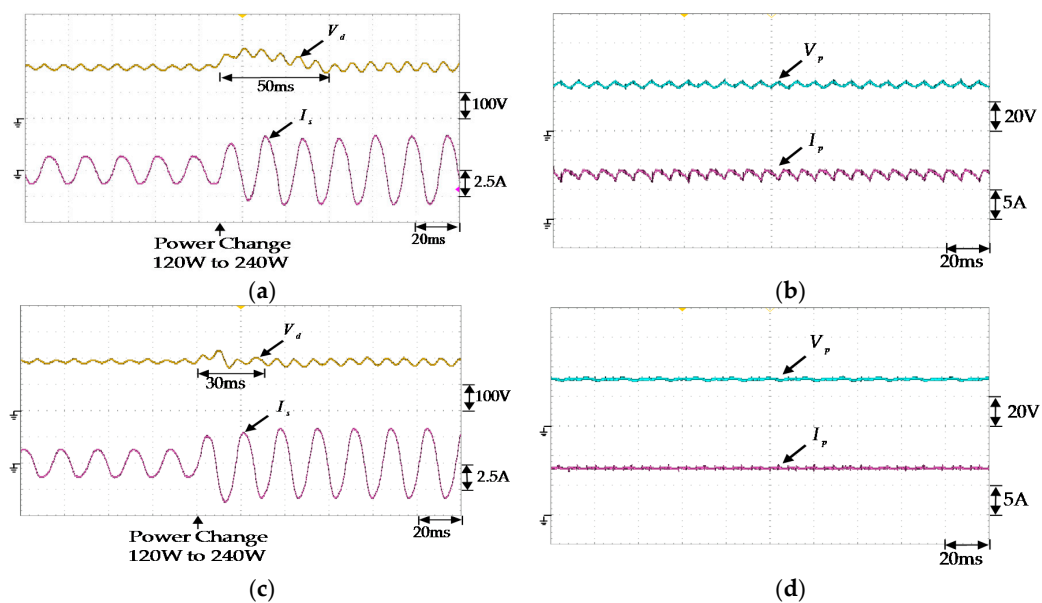
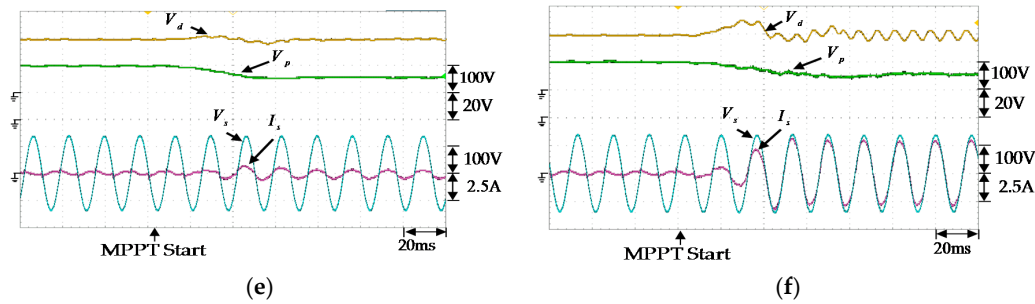
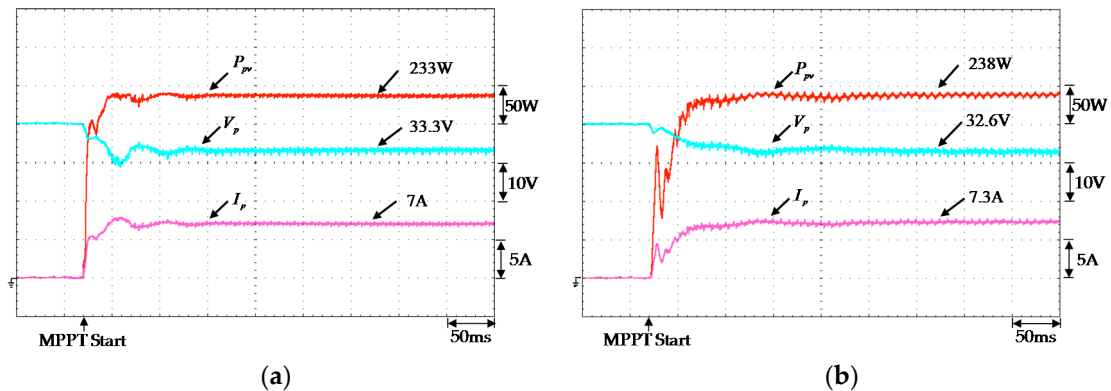


Figure 12. Cont.



**Figure 12.** Experiment results of proposed two-stage MI: (a) DC bus voltage and output current of inverter at step input power changing from 120 W to 240 W without 2nd ripple voltage cancellation controller; (b) Voltage and current of PV module at 240 W power output without input 2nd ripple voltage reduction controller; (c) DC bus voltage and output current of inverter at step input power changing from 120 W to 240 W with 2nd ripple voltage cancellation controller; (d) Voltage and current of PV module at 240 W power output with input 2nd ripple voltage reduction controller; (e) Improved INC MPPT at 24 W (10%) PV output power; (f) Improved INC MPPT at 240 W (100%) PV output power.

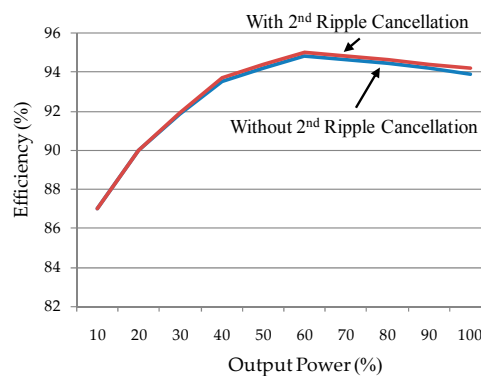
The perturb and observe (P & O) MPPT method [18] is employed to evaluate the performance of the improved INC MPPT algorithm. Figure 13 presents the experiment results showing a performance comparison of the P & O MPPT and the improved INC MPPT algorithms. For both algorithms, MI starts operating at 70 ms and peak power tracking begins within 200 ms. The application of the DC-DC 2nd ripple voltage reduction to the DC-DC converter can eliminate any 2nd ripple voltage at the PV module voltage  $V_p$ . The P & O MPPT algorithm obtains 233 W, whereas the improved INC MPPT algorithm obtains 238 W. This is a clear indication that the improved INC MPPT is able to achieve better MPPT results.



**Figure 13.** Performance comparison between MPPT algorithms: (a) P & O MPPT; (b) Improved INC MPPT.

Figure 14 presents the power conversion efficiency of the MI without and with 2nd ripple voltage cancellation control. Maximum efficiency is achieved at 60% load under both test conditions. The efficiency values of the MI without and with the proposed 2nd ripple voltage cancellation control are 94.8% and 95% respectively. Under full-load conditions, the efficiency values are 93.9% and 94.2% respectively. In accordance with the Energy Policy for Europe (EPE), the efficiency values of the MI without and with 2nd ripple voltage cancellation control are 92.5% and 92.6% respectively. This is a clear demonstration that the proposed 2nd ripple voltage cancellation control is able to improve the power conversion efficiency of the MI. In [23], a MI composed of an input partial power processing resonant converter and an interleaved DC-AC inverter stage was proposed. Its maximum efficiency is 96% at 50% rated load. Though the maximum efficiency is 1% higher in [23], the merits of the proposed

MI in this study are the formulation of an improved INC MPPT to eliminate the need for input current sensor and the development of a feedforward 2nd ripple voltage reduction technique to reduce the voltage ripple at the output of the PV module.



**Figure 14.** Power conversion efficiency of MI without and with proposed 2nd ripple voltage cancellation control.

## 6. Conclusions

This paper outlines the modeling and controller design of a two-stage MI without the use of an E-cap. Two different methods for the reduction of 2nd harmonic voltage ripple on the DC bus as well as on the PV side were developed. These two methods enhance the response speed in voltage regulation while maintaining very low distortion in the grid current. Moreover, an improved version of INC MPPT enables high-precision control without the need for an input current sensor was also developed. The major contributions of this study are as follows: (i) the development of a novel DC bus 2nd ripple voltage cancellation technique to speed up voltage regulation; (ii) the development of a feedforward 2nd ripple voltage reduction technique to reduce the voltage ripple at the PV module; (iii) the formulation of an improved INC MPPT to eliminate the need for input current sensors by using inverter parameters. The following two points are proposed as a guide for future research: (i) the proposed DC bus 2nd ripple voltage cancellation technique could be applied to control the power factor of single-phase AC/DC converters; (ii) the functions of harmonic and reactive power compensation could be developed for the proposed MI.

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