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Abstract: In this study, a novel, non-isolated, cascade-type, single-switch, high step-up DC/DC converter was developed for green energy systems. An integrated coupled inductor and voltage lift circuit were applied to simplify the converter structure and satisfy the requirements of high efficiency and high voltage gain ratios. In addition, the proposed structure is controllable with a single switch, which effectively reduces the circuit cost and simplifies the control circuit. With the leakage inductor energy recovery function and active voltage clamp characteristics being present, the circuit yields optimizable conversion efficiency and low component voltage stress. After the operating principles of the proposed structure and characteristics of a steady-state circuit were analyzed, a converter prototype with 450 W, 40 V of input voltage, 400 V of output voltage, and 95% operating efficiency was fabricated. The Renesas MCU RX62T was employed to control the circuits. Experimental results were analyzed to validate the feasibility and effectiveness of the proposed system.

Keywords: cascade structure; coupled inductor; green energy; high step-up converter

1. Introduction

In response to climate change and global warming induced by heavy use of fossil fuels, energy conservation and carbon reduction techniques, such as developing clean energies and increasing energy use efficiency, have become a global focus. Major countries across the globe have endeavored to develop low-carbon economies based on high performance and low emissions and have adjusted various industry, energy, technology, and transaction-related policies [1,2] to encourage green industry development. Moreover, because fossil fuel supplies are overly concentrated in areas with social instability, fuel prices are typically volatile and affected by human factors (e.g., political schemes and policies). Thus, fossil fuel energy supplies become restricted, resulting in increased geopolitical risks for investors and hindering energy production, transportation, and infrastructure construction and maintenance. Typically, such adversity indirectly leads to social instability and volatile political developments in developing countries. To address these problems, green energies have been developed as the primary method to propel contemporary progression.

The reusability of green energies is unaffected by conventional energy shortages. Numerous applications of green energies have been developed in recent years, such as photovoltaics (PV), wind power, biomass energy, and tidal energy production. However, these green energies are highly dependent on natural conditions and require high investment and maintenance costs, resulting in low power efficiency and high total power generation cost. In addition, the output voltage of reusable energies is low and unstable. Such energy must be converted using a first-stage step-up power converter.
converter before it can be used in households. The conversion process is shown in Figure 1. For instance, the input voltage ($V_{in}$) of photovoltaic ranges between 20 V and 45 V. To effectively feed the photovoltaic energy into the grid, the voltage must be increased to $380 \pm 20$ V to facilitate the grid connection for the rear inverter [3–5] or charge/discharge battery of an electric vehicle (EV) by a bidirectional DC/DC converter [6–8]. In the front-end structure, a boost converter is employed to generate a step-up ratio of at least 1:8. Thus, many high step-up converter structures have been recently researched and developed.

After previous studies have claimed that using a conventional, non-isolated boost converter to multiply voltage requires operating the system duty cycle at an extremely high ratio. Constrained by parasitic elements in the circuit, diodes have a reverse recovery time when equivalent series stray inductance and series impedance of the capacitor exist in the circuit or when switched between on and off transients. These factors restrain the step-up ratio and lower the conversion efficiency [9–11]. To achieve a high step-up ratio and conversion efficiency, while maintaining low development cost and compactness of electric power converters, many scholars have developed technical structures to improve boost converter-based step-up ratios. Applying a cascade type [12–14] boost converter can boost the voltage stepwise and raise the step-up ratio. However, in doing so, multistage cascade converters complicate the circuit and transmit energy indirectly through a capacitor [15,16], which causes unnecessary energy consumption. Therefore, scholars have proposed a voltage lift technique [17,18] to insert a voltage multiplier formed by a capacitor and diode in the boost pathway to substantially simplify the circuit compared with that of the cascade type. However, the voltage lift technique increases the size and cost of the circuit design and the voltage stress the switch bears remains overly high during high voltage output, thereby lowering the designers’ flexibility in selecting components. Consequently, a concept of integrating coupled inductors [4,19,20] and a coupled inductor cascade [21–23] has been proposed to achieve a design with high step-up ratios. This coupled structure couples inductors with a method similar to how a transformer turns a ratio to form a voltage multiplier; thus, the size and cost of circuit design can be reduced considerably. However, when the switched-off leakage of coupled inductors lacks a pathway to release energy, it resonates with the parasitic capacitor of cascade switches, increases the switching voltage stress, and causes increased switching losses, thereby degrading the overall circuit efficiency [24]. To avoid the conversion efficiency deterioration resulting from leakage, scholars have proposed improved circuit designs [19,23] to fabricate a clamping circuit that combines a capacitor and diode, while compromising slight cost and size increases. The clamping circuit can recover leakage energy or increase the control complexity to add a soft-switching converter with zero-current switching (ZCS) and zero-voltage switching (ZVS), to improve the conversion efficiency [25–27].

In the present study, a high step-up converter structure for green energy systems was developed. By using integrated voltage multipliers of three groups of coupled inductors, the proposed converter structure can boost voltage and combine a capacitor and diode to produce a boost converter.

<table>
<thead>
<tr>
<th>Energy source</th>
<th>High step-up Conversion</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Renewable Energy Source</td>
<td>DC to DC Converter</td>
<td>DC to AC Bi-directional Inverter</td>
</tr>
<tr>
<td>PV/Wind</td>
<td>Low input unsteadily</td>
<td>Utility AC Load</td>
</tr>
<tr>
<td></td>
<td>High input stability</td>
<td>DC to DC Bi-directional Converter</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Electric Vehicle Battery</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DC Load</td>
</tr>
</tbody>
</table>

**Figure 1.** Block diagram of application of vehicular green energy systems. PV: photovoltaics; and MPPT: maximum power point tracking.
Additionally, a freewheeling current path is provided to recover leakage energy, reduce the voltage stress on critical components, largely reduce the circuit size, and increase the overall conversion efficiency. The proposed design satisfies the requirements of a high voltage gain ratio, high conversion efficiency, low component voltage stress, and simple control in green energy circuit systems.

2. Operating Principles of the Main Circuit

Figure 2 shows the proposed novel, non-isolated, cascade-type single-switch high step-up DC/DC converter. The main circuit components are composed of a switch (S), the primary magnetizing inductance \( L_m \), magnetizing leakage inductance \( L_{k1} \), and coupled inductors (turns ratio \( N_1:N_2:N_3 \)). A voltage multiplier circuit is composed of diodes \( D_1 \) and \( D_2 \), capacitors \( C_1 \) and \( C_2 \), coupled inductor \( L_2 \), and coupled leakage inductance \( L_{k2} \). Another circuit cascaded with capacitor \( C_3 \) is composed of diodes \( D_4 \) and \( D_5 \), capacitors \( C_4 \) and \( C_5 \), coupled inductor \( L_3 \), and coupled leakage inductance \( L_{k3} \). A complete cycle of the circuits comprises five operating modes, which are analyzed as follows.

![Figure 2. The novel, cascade-type single-switch, high step-up converter with coupled inductors.](image)

To simplify the circuit analysis, the following assumptions were postulated:

1. The capacitance values of \( C_1, C_2, C_3, C_4 \) and \( C_5 \) are high enough to be regarded as constant power sources; and
2. The circuit is operated under the continuous conduction mode (CCM) and the magnetic inductance of each winding is substantially higher than the leakage.

In accordance with these assumptions, the steady-state waveform patterns of the primary operating signals of the converter were operated under the CCM and shown in Figure 3. Figure 4 shows the operating patterns of each mode.
Figure 3. Operating waveform patterns in the continuous conduction mode (CCM).

Figure 4. Mode operating under CCM: (a) Mode I; (b) Mode II; (c) Mode III; (d) Mode IV; and (e) Mode V.
2.1. Mode I ($t_0 \leq t < t_1$)

When $t = t_0$, the $S$, $D_1$ and $D_4$ are turned on, whereas $D_2$, $D_3$ and $D_5$ are turned off. The current pathway is depicted in Figure 4a. In this mode, the $V_{in}$ stores energy through $L_m$ and $L_{k1}$, yielding a linear rise of the inductive current. At the turn-on transient of $S$, $L_{k2}$, and $L_{k3}$ of $N_2$ and $N_3$ continuously release energy to $C_1$ and $C_4$ through $D_1$ and $D_4$, the cascade of $C_3$, $C_4$ and $C_5$ transmits energy to the output load ($R_L$) until the currents $i_{d1}$ and $i_{d4} = 0$. When $t = t_1$, this operating region ends and progresses into the next mode.

2.2. Mode II ($t_1 \leq t < t_2$)

In this operating region, the $S$, $D_2$ and $D_5$ are turned on continuously, whereas $D_1$, $D_3$ and $D_4$ are turned off. The current pathway is depicted in Figure 4b. In this mode, the $V_{in}$ stores energy through $L_m$ and $L_{k1}$, yielding a linear rise of the inductive current. Meanwhile, coupled inductors based on turns ratios $N_{21}$ and $N_{31}$ and through $D_2$ and $D_5$ release energy to $C_2$ and $C_3$ in a forward manner. The cascade of $C_3$, $C_4$ and $C_5$ transmits energy to the $R_L$. When $t = t_2$, this operating region ends and progresses into the next mode.

2.3. Mode III ($t_2 \leq t < t_3$)

In this operating region, when $t = t_2$, the $S$ is turned off transiently. Since the inductive voltage has a continuous current characteristic and cannot be changed instantaneously, $D_2$, $D_3$ and $D_5$ are turned on, whereas $D_1$ and $D_4$ are turned off. The current pathway is depicted in Figure 4c. In this mode, the $V_{in}$ is connected to $V_{C1}$ and $V_{C2}$ in series and transmits energy to $C_3$ through $D_3$. As $D_2$ and $D_5$ are switched on, the coupled inductors maintain leakage currents $i_{Lk2}$, $i_{Lk3}$, from which energy is continuously released to $C_2$ and $C_3$ as the means to recover leakage. The cascade of $C_3$, $C_4$ and $C_5$ transmits energy to the $R_L$. When the $t = t_3$, this operating region ends and enters the next mode.

2.4. Mode IV ($t_3 \leq t < t_4$)

When $t = t_3$, $S$ is permanently turned off and $D_1$, $D_3$ and $D_4$ are turned on, whereas $D_5$ is turned off. The current pathway is depicted in Figure 4d. In this mode, because the preceding mode releases energy continuously until currents $i_{Lk2}$ and $i_{Lk3}$ reach zero, the polarity of the coupled inductors is reversed. The energy at $N_1$ is transmitted through a flyback method and switched on through $D_1$ and $D_4$ to $C_1$ and $C_4$, thereby increasing $i_{d1}$ and $i_{d4}$. The $V_{in}$ is continuously connected to $V_{C1}$ and $V_{C2}$ in series to transmit energy to $C_3$ through $D_3$. At the output end, similarly, the cascade of $C_3$, $C_4$ and $C_5$ transmits energy to the $R_L$ until the $i_{Lk1}$ current reaches zero. When $t = t_4$, this operating region ends and progresses into the next mode.

2.5. Mode V ($t_4 \leq t < t_5$)

In this operating region, the $S$ is turned off permanently. The $V_{in}$ becomes an open circuit because of the zero $i_{Lk1}$ current. $D_1$ and $D_4$ are on, whereas $D_2$, $D_3$ and $D_5$ are off. The current pathway is depicted in Figure 4e. In this mode, the $L_m$ couples energy into $C_1$ and $C_4$ through the coupled inductors. Since the magnetizing inductance is the only source that supplies the required energy, the magnetizing inductance current $i_{Lm}$ and $i_{d1}$ and $i_{d2}$ continue to drop until $t = t_5$. Upon the conclusion of this operating region, a complete switching cycle $T_S$ is achieved.

3. Steady-State Analysis

In this section, discussion and analysis of the voltage gain ratio and switching stress of components are provided. The results are then compared with those of previous studies. To simplify the circuit analysis, the following assumptions were postulated:

1. The capacitance values of $C_1$, $C_2$, $C_3$, $C_4$ and $C_5$ are high enough to be regarded as constant power sources;
(2) The $S, D_1, D_2, D_3, D_4$ and $D_5$ are ideal circuit elements;
(3) The magnetizing inductance of each winding is substantially higher than the leakage, which can, thus, be ignored; and
(4) The converter is operated under the CCM.

3.1. Step-Up Conversion Ratio

With the $S$ turned on, the node voltage analysis based on Kirchhoff’s voltage law (KVL) applied to Mode II, shown in Figure 4b, yields the following equations of voltage stress of the inductance and capacitors:

\begin{align}
V_{in} - V_{L1} &= 0 \quad (1) \\
V_{C2} &= N_{21} \times V_{L1} \quad (2) \\
V_{C5} &= N_{31} \times V_{L1} \quad (3)
\end{align}

where $N_{21} = N_2:N_1$ and $N_{31} = N_3:N_1$.

When the $S$ is off, KVL applied to Mode VI, shown in Figure 4e, can be used to determine the voltage stress of the inductance and capacitors as expressed in the following equations:

\begin{align}
V_{C3} &= V_{in} + V_{C1} + V_{C2} - V_{L1} \quad (4) \\
V_{C1} &= N_2 \times V_{L1} \quad (5) \\
V_{C4} &= N_{31} \times V_{L1} \quad (6)
\end{align}

In accordance with a voltage-second balance principle between the on-off transients of each inductance, the following equations were derived:

\begin{align}
\int_0^{DTs} V_{L1}dt + \int_{DTs}^{Ts} V_{L1}dt &= 0 \quad (7) \\
V_{c1} &= \frac{N_{21} \times DV_{in}}{1 - D} \quad (8) \\
V_{c2} &= \frac{N_{21} \times V_{in}}{1 - D} \quad (9) \\
V_{c3} &= \frac{(1 + D + N_{21}) \times V_{in}}{1 - D} \quad (10) \\
V_{c4} &= \frac{N_{31} \times DV_{in}}{1 - D} \quad (11) \\
V_{c5} &= \frac{N_{31} \times V_{in}}{1 - D} \quad (12)
\end{align}

Since $V_O = V_{C3} + V_{C4} + V_{C5}$, substituting Equations (10)–(12) into the equation can render a voltage gain ratio of converters, as expressed in Equation (13):

\[
\frac{V_O}{V_{in}} = \frac{1 + D + (N_3/N_1) + (N_2/N_1)}{1 - D} \quad (13)
\]

The voltage gain ratio curve obtained from Equation (13) is shown in Figure 5. Under identical duty cycles, the proposed converter provided a higher step-up ratio than did conventional step-up converters at a turns ratio of $n = 1$. 
3.2. Component Voltage Stress

By using the on-off transients, the voltage stress on circuit elements can be calculated. The switch on-off state of Mode II in Figure 4b can be applied to calculate the voltage stress on the $S$ and $D_1$, $D_3$, and $D_4$. The corresponding equations are expressed as follows:

$$V_{\text{switch}} = \frac{1}{1-D} V_{in}$$  \hspace{1cm} (14)

$$V_{D1} = V_{C1} + V_{L2} = \frac{N_2}{1-D} \times V_{in}$$  \hspace{1cm} (15)

$$V_{D3} = V_{C3} - V_{C2} - V_{C1} = \frac{1+D}{1-D} \times V_{in}$$  \hspace{1cm} (16)

$$V_{D4} = V_{C4} + V_{L3} = \frac{N_3}{1-D} \times V_{in}$$  \hspace{1cm} (17)

When the $S$ of Mode VI in Figure 4d is off, the voltage stress on $D_2$ and $D_5$ are calculated using Equations (18) and (19), as follows:

$$V_{D5} = V_{C4} + V_{CS} = \frac{N_3}{1-D} \times V_{in}$$  \hspace{1cm} (18)

$$V_{D2} = V_{C1} + V_{C2} = \frac{N_2}{1-D} \times V_{in}$$  \hspace{1cm} (19)

3.3. Loss Analysis

Performing a loss analysis is a critical step in circuit design. By performing reasonable calculations and evaluations of the power loss characteristics of circuit elements, designers can efficiently design circuits without wasting time on wrong design directions. Loss analysis is discussed in two sections of this paper, separated into loss analysis of individual elements during operation and the estimated conversion efficiency of the entire system.

3.3.1. Switch Element ($S$)

The loss of the $S$ primarily depends on conduction loss and switching loss, which involves driver loss, turn-on, and turn-off transient loss. The loss value is determined by summing Equations (20)–(23), where $T_r$ represents the rise time of the switch and $T_f$ represents the fall time of the switch.

$$P_{\text{conduction-loss}} = I_{\text{fwd}}^2 \times R_{DS(on)}$$  \hspace{1cm} (20)

$$P_{\text{driver-loss}} = \frac{16}{3} \times C_{gs} \times V_{in} \times f_{sw}$$  \hspace{1cm} (21)
\[ P_{\text{turn-on-loss}} = \frac{1}{2} \times T_r \times I_{\text{load}} \times V_{\text{in}} \times f_{\text{sw}} \] (22)

\[ P_{\text{turn-off-loss}} = \frac{1}{2} \times T_f \times I_{\text{load}} \times V_{\text{in}} \times f_{\text{sw}} \] (23)

3.3.2. Magnetic Energy Storage Element (L)

This element comprises copper and core losses. The copper losses refer to losses caused by current \( I \) flowing through wire equivalent impedance \( R \) on a transformer or inductor winding, as expressed in Equation (24). The core losses, or iron losses, can be categorized into hysteresis losses and eddy-current losses. Affected by varying magnetic fields, hysteresis losses cause partial energy losses inside the iron core through thermal dissipation. Eddy-current losses involve the cyclic current (i.e., eddy current) generated within a conductor caused by varying induction of the magnetic field. The energy of eddy currents dissipates through heat transference when passing through the resistance of iron core materials. The eddy-current loss and area of current cycle are positively correlated.

\[ P_{\text{copper-loss}} = I_{\text{load}}^2 \times R \] (24)

3.3.3. Capacitor (C)

The capacitor presents two major loss factors, namely, equivalent series resistance (ESR) and leakage current. When aluminum electrolytic capacitors are operated, leakage current definitely occurs. When the leakage current flows through the internal resistance \( R_c \) in the capacitor, losses are generated. The leakage current should be minimized. The equation to calculate leakage currents is expressed in Equation (25):

\[ I_{\text{leakage}} = K \times C \times V \] (25)

where \( I \) is the leakage current (µA) and \( K \) is the constant set for production.

3.3.4. Diode (D)

Although diodes are unidirectional conducted elements, power losses occur in forward conduction and reverse-bias blocking. In forward conduction, a junction potential barrier \( V_f \) occurs to lower the voltage; when current \( I_{\text{load}} \) flows through the potential barrier, power losses occur, as expressed in Equation (26):

\[ P_{\text{forward-loss}} = V_f \times I_{\text{load}} \times D \] (26)

where \( D \) represents a duty cycle. In addition, parasitic series resistance \( R_d \) exists in the diodes and can cause power losses when the \( I_{\text{load}} \) flows through it. The equation is expressed in Equation (27):

\[ P_{R_d\text{-loss}} = I_{\text{load}}^2 \times R_d \times D \] (27)

When the diodes are in the reverse-bias blocking state, they may have a reverse recovery that prevents the currents from returning to zero transiently during cut off; instead, the current maintains a reverse flow for a certain period before returning to zero. Such current is called reverse recover current \( I_{\text{rm}} \) and the period during which it occurs is called the reverse recovery time \( T_{rr} \). The area resembling an inverse triangle formed by \( I_{\text{rm}} \) and the \( T_{rr} \) is called the reverse storage charge \( Q_{rr} \). Without appropriate recycling mechanisms, the energy accumulates and cause losses, as expressed in Equation (28):

\[ P_{drr\text{-loss}} = \frac{1}{2} T_{rr} \times I_{nn} \times V_R \times f_{\text{sw}} \] (28)

where \( f_{\text{sw}} \) is the switching frequency and \( V_R \) is the reverse-bias voltage of the diode.

In the proposed structure, reverse recovery losses are absent because the capacitors in the circuit recycle and store the energy. Table 1 lists the expected loss assessment of components under a power loading of 450 W. The values were calculated without considering eddy-current losses, \( R_d \), and capacitor losses. The total impedance of the winding was set to 60 mΩ, resistance of switching
conduction $R_{DS(on)}$ as 10 mΩ, diode $V_f$ as 0.55 V, and $f_c$ as 50 kHz for calculation. In this paper, the measurement device was limited, so component power losses were roughly estimated. We neglected some difficult evaluation parameters (for example, eddy-current, capacitance ESR, print circuit board (PCB) (parasitic impedance losses, and capacitance impedance losses, etc.), and the full load efficiency estimation compared with measurement can meet within ±1%. The total component power losses of the system were much smaller than the system power.

### Table 1. Assessment of component power losses under 450 W power loading.

<table>
<thead>
<tr>
<th>Component</th>
<th>Loss Calculation</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch Conduction Loss</td>
<td>2.166</td>
<td>W</td>
</tr>
<tr>
<td>Switch Switching Loss</td>
<td>1.726</td>
<td>W</td>
</tr>
<tr>
<td>Inductor Copper Loss</td>
<td>12.612</td>
<td>W</td>
</tr>
<tr>
<td>Inductor Iron Loss</td>
<td>0.28</td>
<td>W</td>
</tr>
<tr>
<td>Total Diode Loss</td>
<td>7.324</td>
<td>W</td>
</tr>
<tr>
<td>Total</td>
<td>24.108</td>
<td>W</td>
</tr>
<tr>
<td>Calculated Efficiency</td>
<td>94.642%</td>
<td>-</td>
</tr>
<tr>
<td>Measured Efficiency</td>
<td>93.159%</td>
<td>-</td>
</tr>
</tbody>
</table>

#### 3.3.5. Estimated Conversion Efficiency Analysis

In the analysis presented in this subsection, diode $T_n$, coupled coefficient losses and leakage of coupled inductance, and equivalent series inductance of electrolytic capacitors were ignored. The parasitic effects of elements that were considered were the parasitic internal resistance of coupled inductance ($r_{L1}$, $r_{L2}$ and $r_{L3}$), the forward conduction voltage drop of diodes ($V_{D1}$, $V_{D2}$, $V_{D3}$, $V_{D4}$ and $V_{DS}$), the series internal resistance of diodes ($r_{D1}$, $r_{D2}$, $r_{D3}$, $r_{D4}$ and $r_{DS}$), the ESR of capacitors ($r_{C1}$, $r_{C2}$, $r_{C3}$, $r_{C4}$ and $r_{C5}$), and the internal $R_{DS}$, as depicted in Figure 6.

![Figure 6. Equivalent model circuit of efficiency analysis.](image)

To simplify the analysis, temporary recycle pathways caused by leakage and equivalent resistance of capacitors were ignored. Only the on and off states of the switch were considered. Subsequently, the voltage-second balance, small-ripple approximation, and capacitor-charge balance principles were applied to calculate the circuit conversion efficiency, as expressed in Equation (29). The efficiency was the ratio of the output power ($P_o$) to the input power, as expressed in Equation (30):

$$\eta = \frac{V_o}{V_{in}} = \frac{\left( n_2 D + \frac{2-v_{D}D+D}{1-D} \right) - \frac{(V_{D1}+V_{D2}+V_{D3}+V_{D4}+V_{D5})}{1}}{1 + \left( \frac{A}{R_L \times (1-D)^2} \right) + \left( \frac{B}{R_L \times (1-D)} \right) + \left( \frac{C}{R_L} \right) + \left( \frac{D}{R_L} \right)}$$
\[ A = (1 + n_2 D) r_{D3} + r_{C3} (1 + D) + (r_{C1} + r_{C5}) D + (1 - D) (r_{C2} + r_{C4}) \]
\[ B = n_2 (1 - D) r_{L3} + (r_{D1} + r_{D3}) D + (1 - D) \]
\[ C = (1 + n_2) D \times r_{L2} + (r_{D2} + r_{D4}) (1 - D) \]
\[ D = (1 + n_2 + n_3) \times (r_{D5} + r_{L1}) \]
\[ \eta = \frac{1 - D}{2 - n_2 D + D} \frac{1}{1 + \left(\frac{\Delta}{n_2} (1 - D)\right)} \frac{\Delta}{n_2} + \frac{1}{n_2} \left( 1 - D \right) + \frac{1}{n_2} \left( 1 - D \right) \]

where the values of \( r_{L1} \cdots r_{L3} \) are assumed to be 50 m\( \Omega \), \( r_{D1} \cdots r_{D3} \) as 20 m\( \Omega \), \( R_{DS} \) as 10 m\( \Omega \), \( r_{C1} \cdots r_{C5} \) as 20 m\( \Omega \), diode conduction voltage drop as 0.55 V, \( V_{in} \) as 40 V, output voltage as 400 V, and \( R_L \) as 355.56 \( \Omega \). The relationship among efficiency, gain ratio, and duty cycle is shown in Figure 7.

\[ \text{Figure 7. Relationship between efficiency and voltage gain vs. duty cycle.} \]

A desirable step-up ratio was approximately 1:10. The curves in Figure 7 reveal that the turns ratio of \( n = 1:2.2 \) should be applied in consideration of optimal circuit design points. At this ratio, the duty cycle of the \( S \) is approximately 0.5, rendering an efficiency of 95% or higher.

### 3.4. Comparison of the Proposed Structure with Extant Structures

The aforementioned characteristics of the single-switch high step-up converter of the proposed structure were compared with those in [9,16,21], as tabulated in Table 2. In Table 2, \( n_2 \) represents the ratio of coils \( N_2 \) to \( N_1 \); \( n_3 \) represents the ratio of \( N_3 \) to \( N_1 \); and \( D \) represents the operating duty cycle ratio. The voltage gain comparison in Table 2 is depicted in Figure 5, where the turns ratio is \( N_1:N_2:N_3 = 1:2:2 \).

<table>
<thead>
<tr>
<th>Comparison of Studies</th>
<th>Voltage Gain Ratio</th>
<th>Switch Voltage Stress</th>
<th>Diode Voltage Stress</th>
<th>Number of Capacitors</th>
<th>Number of Inductors</th>
<th>Number of Diodes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed structure</td>
<td>( \frac{1+D+n_2+n_3}{1-D/n_2} )</td>
<td>( \frac{V_{in}}{1-D/n_2} )</td>
<td>( n_2 \times \frac{V_{in}}{1-D/n_2} )</td>
<td>5</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>Reference [9]</td>
<td>( \frac{2+n_2+n_3}{1-D/n_2} )</td>
<td>( \frac{V_{in}}{1-D/n_2} )</td>
<td>( (1+n_3) V_{in} )</td>
<td>4</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Reference [16]</td>
<td>( \frac{1+n_2+n_3}{1-D/n_2} )</td>
<td>( \frac{V_{in}}{1-D/n_2} )</td>
<td>( V_{in} + n_3 V_{in} )</td>
<td>3</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>Reference [21]</td>
<td>( \frac{1+n_2+n_3}{1-D/n_2} )</td>
<td>( \frac{V_{in}}{1-D/n_2} )</td>
<td>( n_2 V_{in} )</td>
<td>3</td>
<td>2</td>
<td>4</td>
</tr>
</tbody>
</table>

Figure 8 reveals that the systems of [9,16,21], and the proposed structure renders more than a 10-fold increase of voltage at \( D = 0.5 \cdots 0.6 \). Although the step-up ratio of [9] exhibited an exponential increase with the increase in the control cycle, the cascade structure was unsuitable for overly high duty cycle ratios because of efficiency problems.
4. Experiment Results

Figure 9 shows the comparison of switch voltage stresses of structures listed in Table 2. At $D = 0.75$ or lower, the proposed structure has lower switch voltage stresses compared with the other three structures.

Figure 10 depicts the comparison of diode voltage stresses. At $D = 0.8$ or lower, the proposed structure has lower voltage stress than do the other three structures.

Figure 11 reveals a block diagram of system hardware and software planning. A microcontroller RX62T (Renesas, Santa Clara, CA, USA) was employed as the basis of system control. Through
digitized control, the problems of an overly complex hardware circuit and difficulty in designing the control circuit caused by the massive use of analog circuits can be avoided.

**Figure 10.** Comparison of diode voltage stresses (N\(_1\):N\(_2\):N\(_3\) = 1:1:1).

4. Experiment Results

Figure 11 reveals a block diagram of system hardware and software planning. A microcontroller RX62T (Renesas, Santa Clara, CA, USA) was employed as the basis of system control. Through digitized control, the problems of an overly complex hardware circuit and difficulty in designing the control circuit caused by the massive use of analog circuits can be avoided.

**Figure 11.** Block diagram of system hardware and software planning.

Figure 12 shows the picture of the experimental prototype circuit.

**Figure 12.** Picture of the experimental prototype circuit.

The electrical specification and element parameters of the circuit are tabulated in Table 3.

**Table 3.** Electrical specification and components of the experimental circuit.

<table>
<thead>
<tr>
<th>Component</th>
<th>Model</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input DC Voltage (V_{in})</td>
<td>36–48 V</td>
<td></td>
</tr>
<tr>
<td>Output DC Voltage (V_O)</td>
<td>400 V</td>
<td></td>
</tr>
<tr>
<td>Max output power (P_o)</td>
<td>450 W</td>
<td></td>
</tr>
<tr>
<td>Switching frequency (f_s)</td>
<td>50 kHz</td>
<td></td>
</tr>
<tr>
<td>Coupled inductors turns ratio</td>
<td>(N_1:N_2:N_3 = 1:2:2)</td>
<td></td>
</tr>
<tr>
<td>(S_1)</td>
<td>IRFP4110</td>
<td>100 V, 120 A</td>
</tr>
<tr>
<td>(D_1, D_2, D_4, D_5)</td>
<td>MBR20200</td>
<td>200 V/20 A</td>
</tr>
<tr>
<td>(D_3)</td>
<td>NF020</td>
<td>200 V/40 A</td>
</tr>
<tr>
<td>(L)</td>
<td>MPPRing core</td>
<td>125 (\mu)H</td>
</tr>
<tr>
<td>(C_1, C_2)</td>
<td>MPP Film Capacitor</td>
<td>10 (\mu)F/100 V</td>
</tr>
<tr>
<td>(C_3)</td>
<td>Electrolytic Capacitor</td>
<td>300 (\mu)F/400 V</td>
</tr>
<tr>
<td>(C_4, C_5)</td>
<td>MPP Film Capacitor</td>
<td>22 (\mu)F/100 V</td>
</tr>
</tbody>
</table>
Figure 13 reveals the operating waveforms of each element measured under the power loading of 450 W: (a) $V_s$ waveform and inductive current waveform; (b) $D_1$–$D_3$ voltage waveform; (c) $D_4$ and $D_5$ voltage waveform; (d) $D_1$–$D_3$ current waveform; (e) $D_4$ and $D_5$ current waveform; and (f) voltage waveform of $C_1$, $C_3$, $C_4$, and output. From the experimental waveforms of Figure 13 compared with the steady-state analysis before, the proposed converter had been proved that the component voltage stress of the active switch and diodes are less than 100 V, and was consistent with the results of steady-state analysis.

![Operating waveforms of each element](image)

**Figure 13.** The operating waveforms of each element measured under the power loading of 450 W, (a) $V_{gs}$: 10 V/div, $V_{ds}$: 50 V/div, $I_{LK1}$: 25 A/div, $I_{ds}$: 25 A/div, time: 5 $\mu$s/div; (b) $V_{gs}$: 10 V/div, $V_{D1}$: 100 V/div, $V_{D2}$: 100 V/div, $V_{D3}$: 50 V/div, time: 5 $\mu$s/div; (c) $V_{gs}$: 10 V/div, $V_{D4}$: 100 V/div, $V_{D5}$: 100 V/div, time: 5 $\mu$s/div; (d) $V_{gs}$: 20 V/div, $I_{D1}$: 5 A/div, $I_{D2}$: 5 A/div, $I_{D3}$: 25 A/div, time: 5 $\mu$s/div; (e) $V_{gs}$: 20 V/div, $I_{D4}$: 5 A/div, $I_{D5}$: 5 A/div, time: 5 $\mu$s/div; and (f) $V_{C1}$: 50 V/div, $V_{C3}$: 250 V/div, $V_{C4}$: 50 V/div, $V_{C5}$: 200 V/div, time: 25 $\mu$s/div.

Figure 14 shows the comparison of efficiency curves of the proposed converter and those presented in previous studies. The $V_{in}$, output voltage, and output power for the proposed converter were 40 V, 400 V and 450 W, respectively. The output power of [9,16,21] were only 200, 400 and 300 W, respectively. These curves were measured under a distinct $P_o$. Under a light-load $P_o$ of 50 W, the proposed structure yielded a 94.511% efficiency. Under a full-load $P_o$ of 450 W, the efficiency became 93.2%. The optimal efficiency (95.346%) was reached under a $P_o$ of 250 W. The efficiency under all power conditions was higher than 93%.
Table 4 shows the weight efficiency of the proposed converter based on California Energy Commission (CEC) standard [28], the results show the converter reached 94.6% weight efficiency at the nominal input voltage.

Table 4. The weight efficiency of proposed converter.

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>10%</th>
<th>20%</th>
<th>30%</th>
<th>50%</th>
<th>75%</th>
<th>100%</th>
<th>Weight Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>36 V</td>
<td>94.018</td>
<td>94.287</td>
<td>94.441</td>
<td>94.608</td>
<td>93.983</td>
<td>92.648</td>
<td>94.119</td>
</tr>
<tr>
<td>40 V</td>
<td>94.447</td>
<td>94.768</td>
<td>95.086</td>
<td>95.268</td>
<td>94.375</td>
<td>93.159</td>
<td>94.610</td>
</tr>
<tr>
<td>48 V</td>
<td>94.836</td>
<td>95.322</td>
<td>95.462</td>
<td>95.712</td>
<td>94.898</td>
<td>93.541</td>
<td>95.090</td>
</tr>
<tr>
<td>-</td>
<td>4%</td>
<td>5%</td>
<td>12%</td>
<td>21%</td>
<td>53%</td>
<td>5%</td>
<td>-</td>
</tr>
</tbody>
</table>

5. Conclusions

In the present study, a high step-up DC/DC converter with coupled inductance and voltage multipliers was developed. Through operating principles, steady-state analysis, and final test results, the effectiveness and feasibility of the proposed converter were validated. Applying the design of a single switch and coupled inductance with an integrated common core can substantially simplify the control circuit and reduce costs, while maintaining the effect of high step-up ratios. In addition, the proposed converter can recycle leakage, thereby minimizing the reverse voltage stress of the switch and diodes. Consequently, the switching losses can be reduced. Meanwhile, low-conduction loss elements can be flexibly selected to lower the conduction losses and improve the converter efficiency. In accordance with the experiment results, the converter efficiency reached 93.16% and 95.35% under the output power conditions of 450 W and 250 W, respectively. Obviously the proposed converter is advantageous for integrating high efficiency, simple structure, and high voltage gain ratios.

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Author Contributions: These authors contributed equally to this work.

Conflicts of Interest: The authors declare no conflict of interest.

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